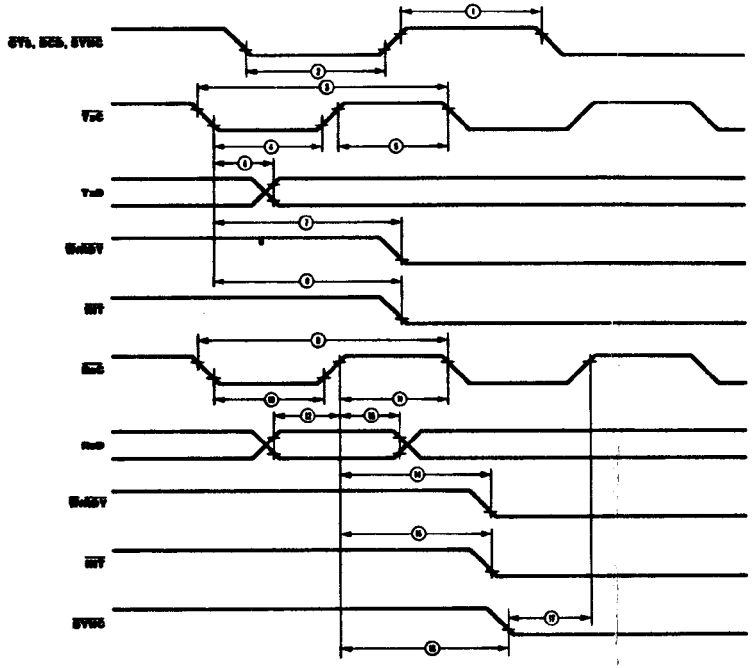
AC CHARACTERISTICS TIMING (Continued)



AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	Z80-4 SIO Min	Z80-4 SIO Max	Z80-6 SIO Min	Z80-6 SIO Max	Notes*
1	TwPh	Pulse Width (High)	200[c]		200[c]		2
2	TwPl	Pulse Width (Low)	200[c]		200[c]		2
3	TcTxC	$\overline{TxC}$ Cycle Time	400[c]	∞[c]	330[c]	∞[c]	2
4	TwTxCl	$\overline{TxC}$ Width (Low)	180[c]	∞[c]	100[c]	∞[c]	2
5	TwTxCh	$\overline{TxC}$ Width (High)	180[c]	∞[c]	100[c]	∞[c]	2
6	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD Delay (x1 Mode)		300[a]		220[a]	2
7	TdTxC(W/RRt)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	5[c]	9[c]	5[c]	9[c]	1
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5[c]	9[c]	5[c]	9[c]	1
9	TcRxC	$\overline{RxC}$ Cycle Time	400[c]	∞[c]	330[c]	∞[c]	2
10	TwRxCl	$\overline{RxC}$ Width (Low)	180[c]	∞[c]	100[c]	∞[c]	2
11	TwRxCh	$\overline{RxC}$ Width (High)	180[c]	∞[c]	100[c]	∞[c]	2
12	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ Setup Time (x1 Mode)	0[c]		0[c]		2
13	ThRxD(RxC)	$\overline{RxC}$ ↑ to RxD Hold Time (x1 Mode)	140[c]		100[c]		2
14	TdRxC(W/RRt)	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	10[c]	13[c]	10[c]	13[c]	1
15	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ Delay	10[c]	13[c]	10[c]	13[c]	1
16	TdRxC(SYNC)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ ↓ Delay (Output Modes)	4[c]	7[c]	4[c]	7[c]	1
17	TsSYNC(RxC)	$\overline{SYNC}$ ↓ to $\overline{RxC}$ ↑ Setup (External Sync Modes)	-100[c]		-100[c]		2

* In all modes, the System Clock rate must be at least five times the maximum data rate. $\overline{RESET}$ must be active a minimum of one complete clock cycle
1. Units equal to System Clock Periods.
2. Units in nanoseconds (ns)

* Clock-cycle time-dependent characteristics. See Footnotes to AC Characteristics.
+ Timings are preliminary and subject to change. Units in nanoseconds.
a Tested
b Guaranteed by Design
c Guaranteed by Characterization

Zilog

Z08440/1/2/4 Customer Procurement Spec (CPS)

GENERAL DESCRIPTION

The Z80 SIO Serial Input/Output Controller is a dual-channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications.

The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs, and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on two fully-independent channels, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast, or slow, peripheral devices. While designed primarily as a member of the Z80 family, its versatility makes it well suited to many other CPUs.

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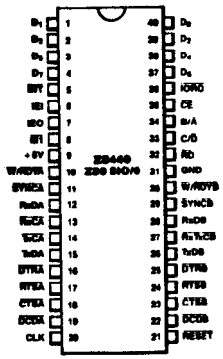
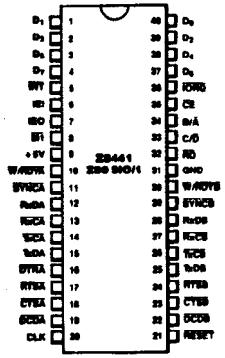
(MARCOM) DC2833 DOCUMENT CONTROL MASTER

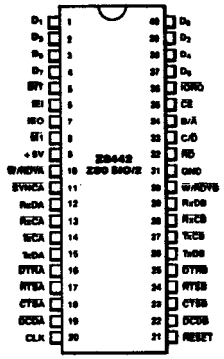
00-2833-02



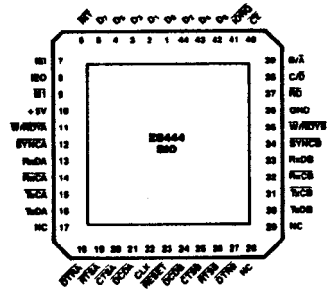
40-pin Dual-In-Line Package (DIP), Pin Assignments



40-pin Dual-In-Line Package (DIP), Pin Assignments



40-pin Dual-In-Line Package (DIP), Pin Assignments



44-pin Chip Carrier, Pin Assignments

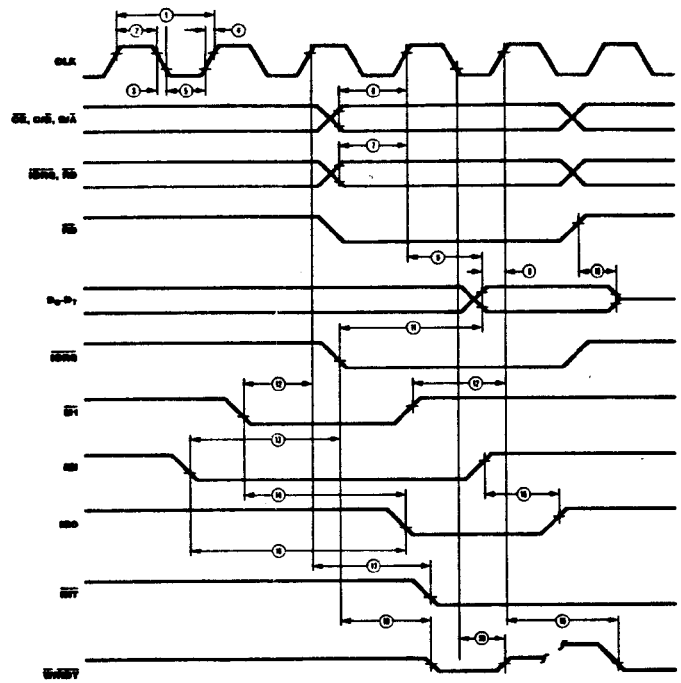
DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3[c]	+0.45[a]	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−0.6[a]	V_{CC}+0.3[a]	V	
V_{IL}	Input Low Voltage	−0.3[c]	+0.8[a]	V	
V_{IH}	Input High Voltage	+2.0[a]	V_{CC}[a]	V	
V_{OL}	Output Low Voltage		+0.4[a]	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.4[a]		V	I_{OH} = −250 μA
I_{LI}	Input Leakage Current		±10[a]	μA	V_{IN} = 0 to V_{CC}
I_{OL}	3-State Output Leakage Current in Float		±10[a]	μA	V_{OUT} = 0.4V to V_{CC}
$I_{L(SY)}$	$\overline{SYNC}$ Pin Leakage Current		+10/−40[a]	μA	0 < V_{IN} < V_{CC}
I_{CC}	Power Supply Current		100[a]	mA	

Over specified temperature and voltage range.

a Tested
b Guaranteed by Design
c Guaranteed by Characterization

AC CHARACTERISTICS TIMING



AC CHARACTERISTICS*

Number	Symbol	Parameter	Z80-4 SIO Min	Z80-4 SIO Max	Z80-6 SIO Min	Z80-6 SIO Max
1	TcC	Clock Cycle Time	250[a]	4000[c]	165[c]	4000[c]
2	TwCh	Clock Width (High)	105[c]	2000[c]	70[c]	2000[c]
3	TfC	Clock Fall Time		30[c]		15[c]
4	TrC	Clock Rise Time		30[c]		15[c]
5	TwCl	Clock Width (Low)	105[c]	2000[c]	70[c]	2000[c]
6	TsAD(C)	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to Clock ↑ Setup Time	145[a]		80[a]	
7	TsCS(C)	$\overline{IORQ}$, $\overline{RD}$ to Clock ↑ Setup Time	115[a]		80[a]	
8	TdC(DO)	Clock ↑ to Data Out Delay		220[a]		150[a]
9	TsDI(C)	Data In to Clock ↑ Setup (Write or $\overline{M1}$ Cycle)	50[a]		30[a]	
10	TdRD(DOz)	$\overline{RD}$ ↑ to Data Out Float Delay		110[c]		90[c]
11	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTACK Cycle)		160[c]		120[c]
12	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	90[a]		75[a]	
13	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time (INTACK Cycle)	140[c]	[+]	120[c]	
14	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (interrupt before $\overline{M1}$)		190[c]		150[c]
15	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED decode)		100[c]		70[c]
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		100[a]		70[a]
17	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		200[a]		150[a]
18	TdIO(W/RWf)	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Wait Mode)		210[c]		175[c]
19	TdC(W/RRf)	Clock ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)		120[a]		100[c]
20	TdC(W/RWz)	Clock ↓ to $\overline{W/RDY}$ Float Delay (Wait Mode)		130[c]		110[c]
21	Th	Any unspecified Hold when Setup is specified	0[c]		0[c]	

*Clock-cycle time-dependent characteristics. See Footnotes to AC Characteristics.
+ Timings are preliminary and subject to change. Units in nanoseconds.
a Tested b Guaranteed by Design c Guaranteed by Characterization*