XR-2207

Voltage-Controlled Oscillator

June 1997–3

FEATURES

- Excellent Temperature Stability (20ppm/°C)
- Linear Frequency Sweep
- Adjustable Duty Cycle (0.1% to 99.9%)
- Two or Four Level FSK Capability
- Wide Sweep Range (1000:1 Minimum)
- Logic Compatible Input and Output Levels
- Wide Supply Voltage Range (±4V to ±13V)
- Low Supply Sensitivity (0.1% /V)
- Wide Frequency Range (0.01Hz to 1MHz)
- Simultaneous Triangle and Squarewave Outputs

APPLICATIONS

- FSK Generation
- Voltage and Current-to-Frequency Conversion
- Stable Phase-Locked Loop
- Waveform Generation
  - Triangle, Sawtooth, Pulse, Squarewave
- FM and Sweep Generation

GENERAL DESCRIPTION

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01Hz to 1MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

The XR-2207 has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2207M	14 Lead 300 Mil CDIP	-55°C to +125°C
XR-2207CP	14 Lead 300 Mil PDIP	0°C to +70°C
XR-2207D	16 Lead 300 Mil JEDEC SOIC	0°C to +70°C
XR-2207ID	16 Lead 300 Mil JEDEC SOIC	-40°C to +85°C

BLOCK DIAGRAM

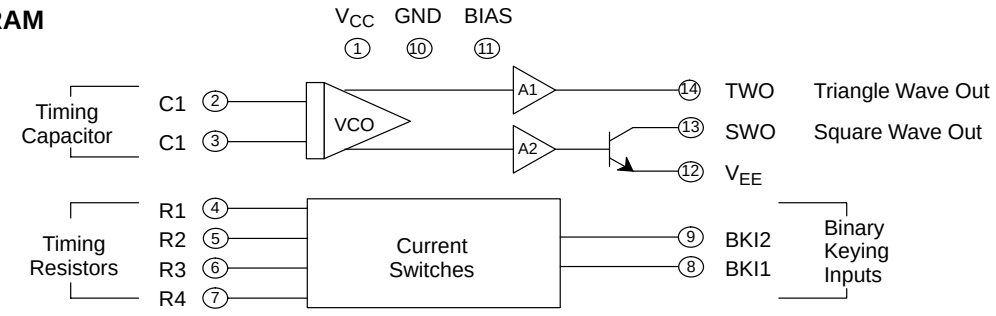
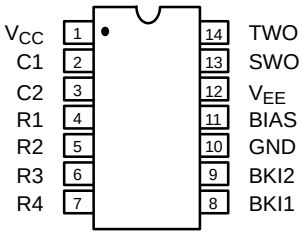


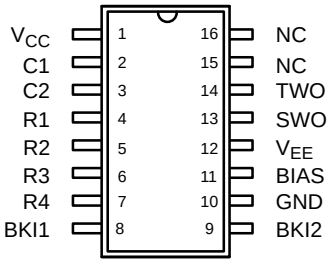
Figure 1. Block Diagram

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

PIN CONFIGURATION



14 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	V_{CC}		Positive Power Supply.
2	C1	I	Timing Capacitor Input.
3	C2	I	Timing Capacitor Input.
4	R1	I	Timing Resistor 1 Input.
5	R2	I	Timing Resistor 2 Input.
6	R3	I	Timing Resistor 3 Input.
7	R4	I	Timing Resistor 4 Input.
8	BKI1	I	Binary Keying 1 Timing Resistor Select Input.
9	BKI2	I	Binary Keying 2 Timing Resistor Select Input.
10	GND		Ground Pin.
11	BIAS	I	Bias Input for Single Supply Operation.
12	V_{EE}		Negative Power Supply.
13	SWO	O	Square Wave Output Signal.
14	TWO	O	Triangle Wave Output Signal.
15, 16	NC		Only SOIC-16 Package.

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of *Figure 3* and *Figure 4*, $V_{CC} = V_{EE} = 6V$, $T_A = +25°C$, C = 5000pF, $R_1 = R_2 = R_3 = R_4 = 20k\Omega$, RL = 4.7kΩ, Binary Inputs Grounded, S_1 and S_2 Closed Unless Otherwise Specified

Parameters	XR-2207ID/XR-2207M			XR-2207CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
General Characteristics								
Supply Voltage								
Single Supply	8		26	8		26	V	See *Figure 3*
Split Supplies	±4		±13	±4		±13	V	See *Figure 4*
Supply Current								See *Figure 3*
Single Supply		5	7		5	8	mA	Measure at Pin 1, S_1, S_2 Open
Split Supply								See *Figure 4*
Positive		5	**7**		5	**8**	mA	Measure at Pin 1, S_1, S_2 Open
Negative		4	**6**		4	**7**	mA	Measured at Pin 12, S_1, S_2 Open
Oscillator Section - Frequency Characteristics								
Upper Frequency Limit	**0.5**	1.0		**0.5**	1.0		MHz	C =500pF, $R_3 = 2k\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	C =50µF, $R_3 = 2M\Omega$
Frequency Accuracy		±1	±**3**		±1	±**5**	% of f_O	
Frequency Matching		**0.5**			**0.5**		% of f_O	
Frequency Stability								
Temperature		20	50		30		ppm/°C	0°C < T_A< 70°C
Power Supply		0.15			0.15		%V	
Sweep Range	**1000:1**	3000:1			**1000:1**		f_H/f_L	R3 = 1.5kΩ for f_{H1} R3 = 2MΩ for f_L
Sweep Linearity							%	C =5000pF
10:1 Sweep		1	**2**		1.5			f_H=10kHz, f_L= 1kHz
1000:1 Sweep		**5**			**5**			f_H=100kHz, f_L= 100Hz
FM Distortion		0.1			0.1		%	±10% FM Deviation
Recommended Range of Timing Resistors	**1.5**		**2000**	**1.5**		**2000**	kΩ	See Characteristic Curves
Impedance at Timing Pins		75			75		Ω	Measured at Pins 4, 5, 6, or 7
DC Level at Timing Terminals		10			10		mV	
Binary Keying Inputs								
Switching Threshold	1.4	2.2	2.8	1.4	2.2	2.8	V	Measured at Pins 8 and 9, Referenced to Pin 10
Input Impedance		5			5		kΩ	

Notes
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2207ID/XR-2207M			XR-2207CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Output Characteristics								
Triangle Output								Measured at Pin 13
Amplitude	**4**	6		**4**	6		V_{PP}	
Impedance		10			10		Ω	
DC Level		+100			+100		mV	Referenced to Pin 10
Linearity		0.1			0.1		%	From 10% to 90% to Swing
Squarewave Output								Measured at Pin 13, S_2 Closed
Amplitude	**11**	12		**11**	12		Vpp	
Saturation Voltage		0.2	**0.4**		0.2	**0.4**	V	Referenced to Pin 12
Rise Time		200			200		nsec	$C_L \leq 10pF$
Fall Time		20			20		nsec	$C_L \leq 10pF$

Notes
Bold face parameters *are covered by production test and guaranteed over operating temperature range.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 26V
Storage Temperature Range . . . . . -65°C to +150°C
Power Dissipation (package limitation)
Ceramic package 750mW
Derate above +25°C . . . . . 6mW/°C
Plastic package 625mW
Derate above +25°C . . . . . 5mW/°C
SOIC package 500mW
Derate above +25°C . . . . . 4mW/°C

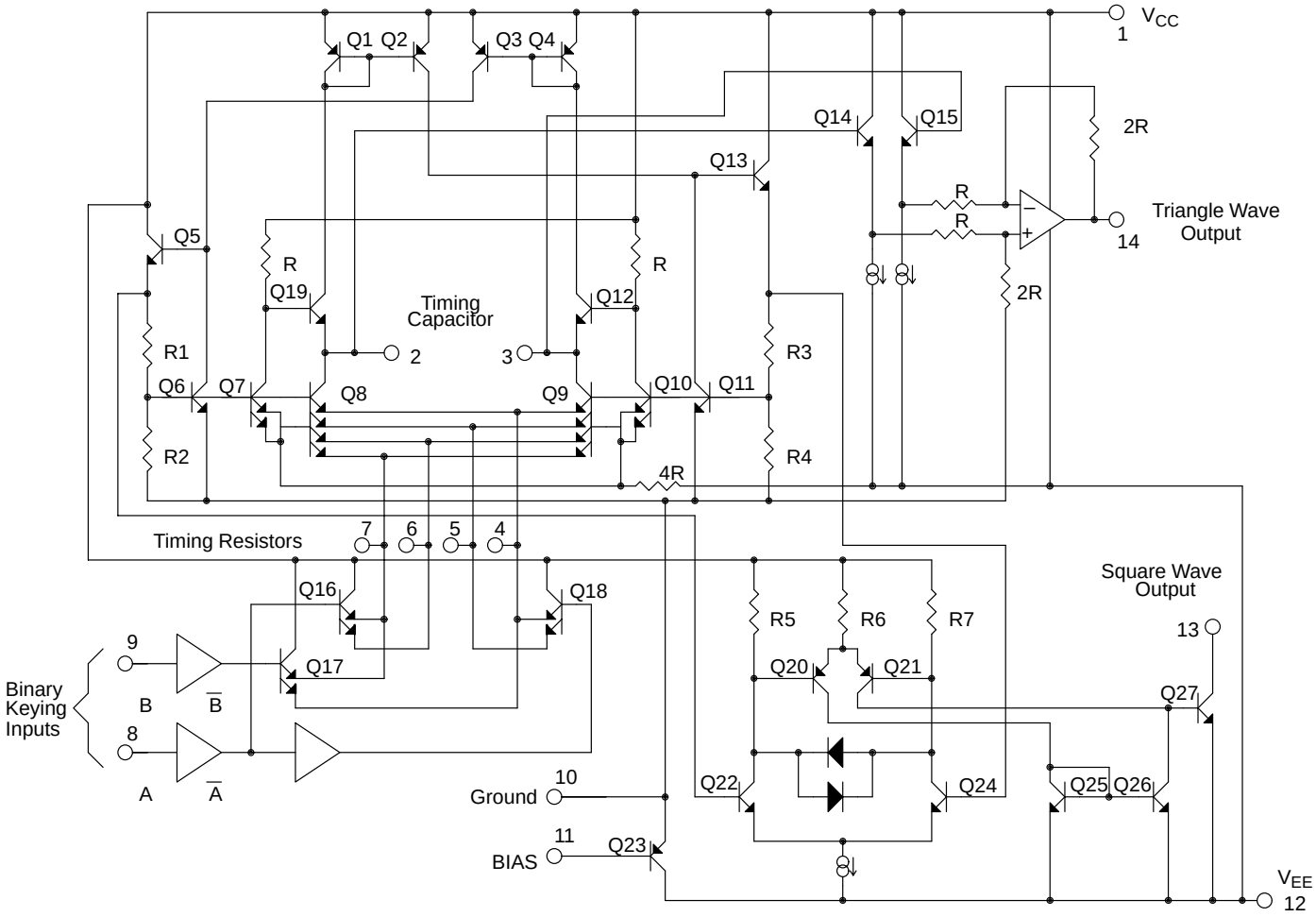


Figure 2. Equivalent Schematic Diagram

PRECAUTIONS

The following precautions should be observed when operating the XR-2207 family of integrated circuits:

1. Pulling excessive current from the timing terminals will adversely affect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the total current drawn from pins 4, 5, 6, and 7 be limited to $\leq$ 6mA. In addition, permanent damage to the device may occur if the total timing current exceeds 10mA.
2. Terminals 2, 3, 4, 5, 6 , and 7 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltage.
3. The keying logic pulse amplitude should not exceed the supply voltage.

SYSTEM DESCRIPTION

The XR-2207 functional blocks are shown in the block diagram given in *Figure 1*. They are a voltage controlled oscillator (VCO), four current switches which are controlled by binary keying inputs, and two buffer amplifiers for triangle and squarewave outputs. *Figure 2* is a simplified XR-2207 schematic diagram that shows the circuit in greater detail.

The VCO is a modified emitter-coupled current controlled multivibrator. Its oscillation is inversely proportional to the value of the timing capacitor connected to pins 2 and 3, and directly proportional to the total timing current I_T. This current is determined by the resistors that are connected from the four timing terminals (pins 4, 5, 6 and 7) to ground, and by the logic levels that are applied to the two binary keying input terminals (pins 8 and 9). Four different oscillation frequencies are possible since I_T can have four different values.

The triangle output buffer has a low impedance output (10Ω TYP) while the squarewave is an open-collector type. An external bias input allows the XR-2207 to be used in either single or split supply applications.

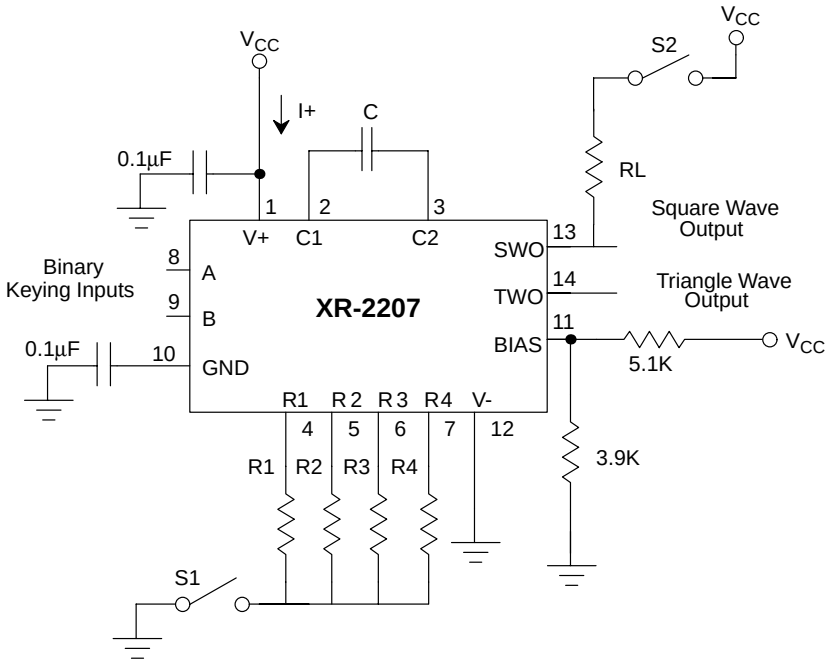


Figure 3. Test Circuit for Single Supply Operation

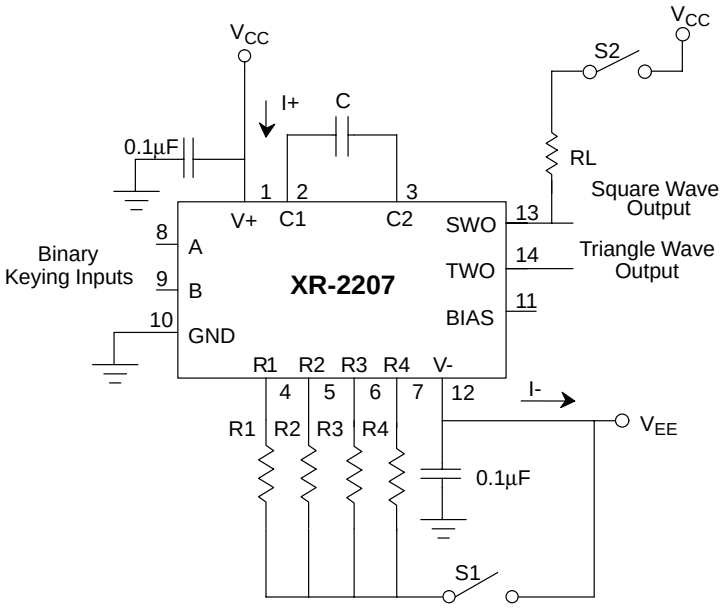


Figure 4. Test Circuit for Split Supply Operation

OPERATING CONSIDERATIONS

Supply Voltage (Pins 1 and 12)

The XR-2207 is designed to operate over a power supply range of ±4V to ±13V for split supplies, or 8V to 26V for single supplies. *Figure 5* shows the permissible supply voltage for operation with unequal split supply voltages. *Figure 6* and *Figure 7* show supply current versus supply voltage Performance is optimum for ±6V split supply, or 12V single supply operation. At higher supply voltages, the frequency sweep range is reduced.

Ground (Pin 10)

For split supply operation, this pin serves as circuit ground. For single supply operation, pin 10 should be AC grounded through a 1µF bypass capacitor. During split supply operation, a ground current of $2I_T$ flows out of this terminal, where I_T is the total timing current.

Bias for Single Supply (Pin 11)

For single supply operation, pin 11 should be externally biased to a potential between $V^+/3$ and $V^+/2V$ (see *Figure 3*). The bias current at pin 11 is nominally 5% of the total oscillation timing current, I_T.

Bypass Capacitors

The recommended value for bypass capacitors is 1µF although larger values are required for very low frequency operation.

Timing Resistors (Pins 4, 5, 6, and 7)

The timing resistors determine the total timing current, I_T, available to charge the timing capacitor. Values for timing resistors can range from 2kΩ to 2MΩ; however, for optimum temperature and power supply stability, recommended values are 4kΩ to 200kΩ (see *Figure 8*, *Figure 9*, *Figure 10* and *Figure 11*). To avoid parasitic pick up, timing resistor leads should be kept as short as possible. For noisy environments, unused or deactivated timing terminals should be bypassed to ground through 0.1µF capacitors.

Timing Capacitor (Pins 2 and 3)

The oscillator frequency is inversely proportional to the timing capacitor, C. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100pF to 100µF. The capacitor should be non-polarized.

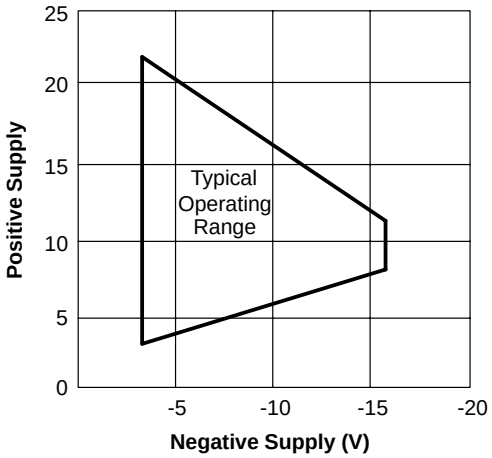


Figure 5. Operating Range for Unequal Split Supply Voltages

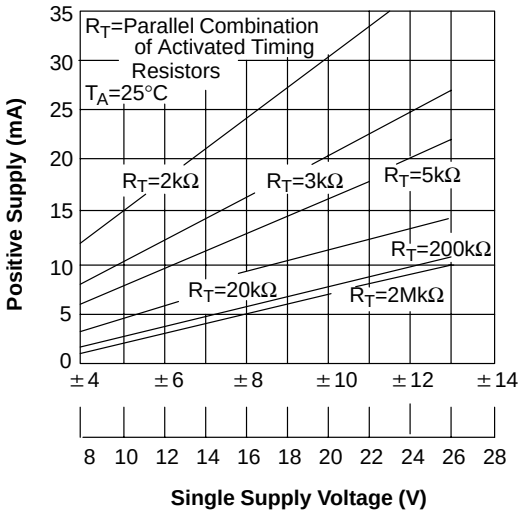


Figure 6. Positive Supply Current, I^+ (Measured at Pin 1) vs. Supply Voltage

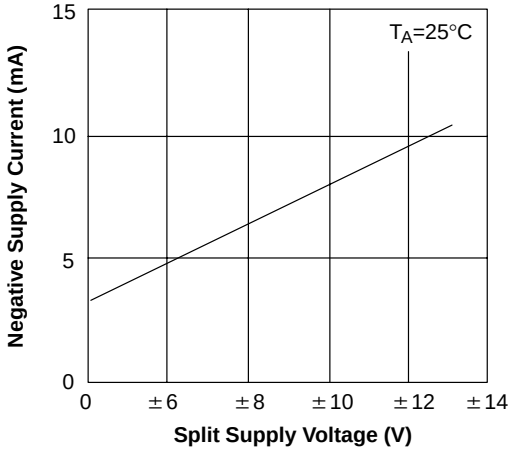


Figure 7. Negative Supply Current, I^- (Measured at Pin 12) vs. Supply Voltage

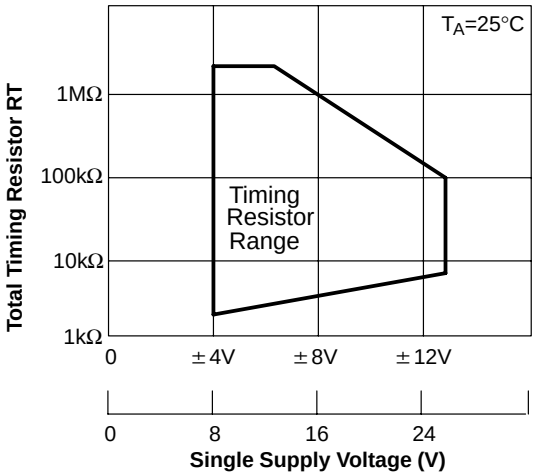


Figure 8. Recommended Timing Resistor Value vs. Power Supply Voltage

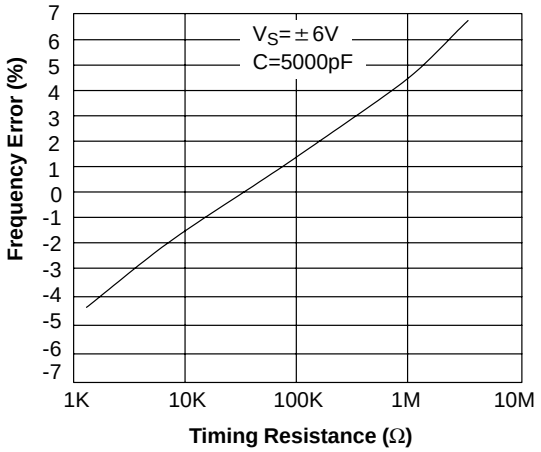


Figure 9. Frequency Accuracy vs. Timing Resistance

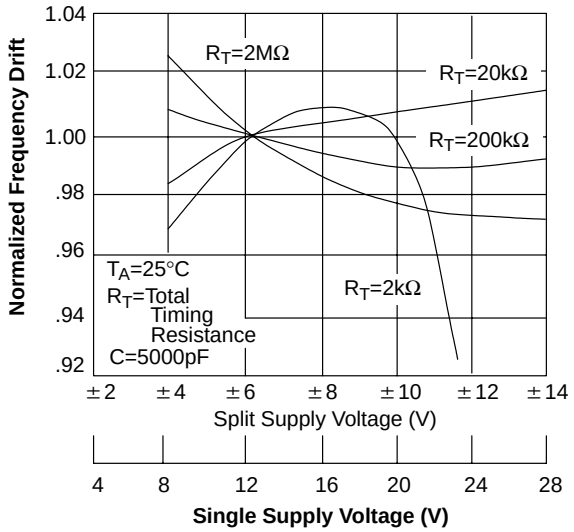


Figure 10. Frequency Drift vs. Supply Voltage

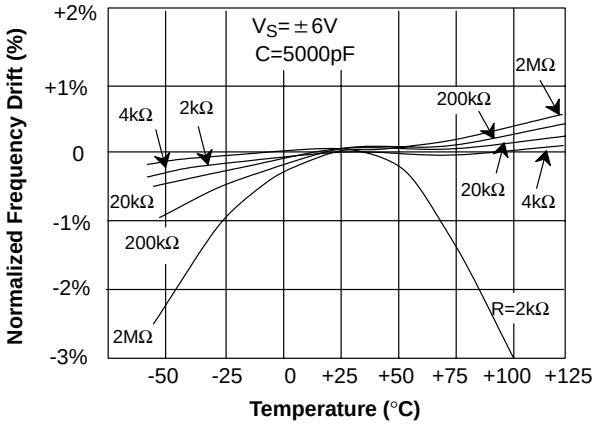


Figure 11. Normalized Frequency Drift with Temperature

Binary Keying Inputs (Pins 8 and 9)

The logic levels applied to the two binary keying inputs allow the selection of four different oscillator frequencies. The internal impedance at these pins is approximately 5kΩ. Keying voltages, which are referenced to pin 10, are < 1.4 V for "zero" and > 3V for "one" logic levels. *Table 1* relates binary keying input logic levels, and selected timing pins to oscillator output frequency for each of the four possible cases.

Figure 12 shows the oscillator control mechanism in greater detail. Timing pins 4, 5, 6 and 7 correspond to the emitters of switching transistor pairs T1, T2, T3, and T4 respectively, which are internal to the integrated circuit. The current switches, and corresponding timing terminals, are activated by external logic signals applied to pins 8 and 9.

Logic Level		Selected Timing Pins	Frequency
Pin 8	Pin 9		
0	0	6	f_1
0	1	6 and 7	$f_1 + \Delta f_1$
1	0	5	f_2
1	1	4 and 5	$f_2 + \Delta f_2$

Table 1. Logic Table for Binary Keying Controls

Definitions:

$$f_1 = \frac{1}{R_3C} \quad \Delta f_1 = \frac{1}{R_4C} \quad \Delta f_2 = \frac{1}{R_2C} \quad \Delta f_2 = \frac{1}{R_1C}$$

Logic Levels: 0 = Ground, 1 $\geq$ 3V

Note

For single supply operation, logic levels are referenced to voltage at pin 10

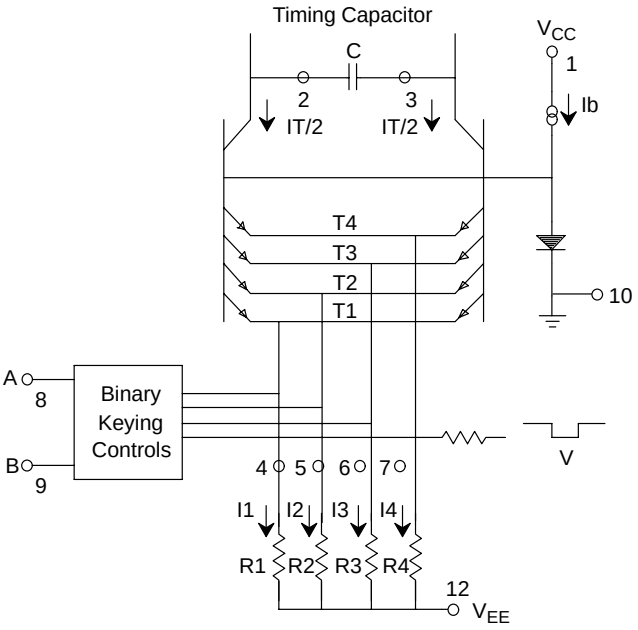


Figure 12. Simplified Schematic of Frequency Control Mechanism

Squarewave Output (Pin 13)

The squarewave output at pin 13 is an "open-collector" stage capable of sinking up to 20mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1kΩ to 100kΩ.

Triangle Output (Pin 14)

The output at pin 14 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 14 has a 10Ω output impedance and is internally protected against short circuits.

MODES OF OPERATION

Split Supply Operation

Figure 13 is the recommended configuration for split supply operation. The circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs with ±6V supplies. For operation with unequal supply voltages, see *Figure 5*.

With the generalized circuit of *Figure 13A*, the frequency of operation is determined by the timing capacitor, C, and the activated timing resistors (R_1 through R_4). The timing resistors are activated by the logic signals at the binary

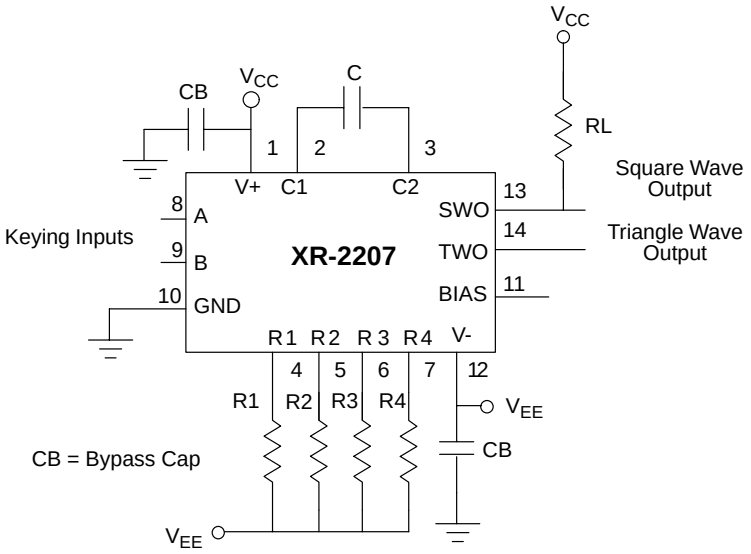
keying inputs (pins 8 and 9), as shown in the logic table (*Table 1*). If a single timing resistor is activated, the frequency is 1/RC. Otherwise, the frequency is either $1/(R_1||R_2)C$ or $1/(R_3||R_4)C$.

Figure 13B shows a fixed frequency application using a single timing resistor that is selected by grounding the binary keying inputs. The oscillator frequency is $1/R_3C$.

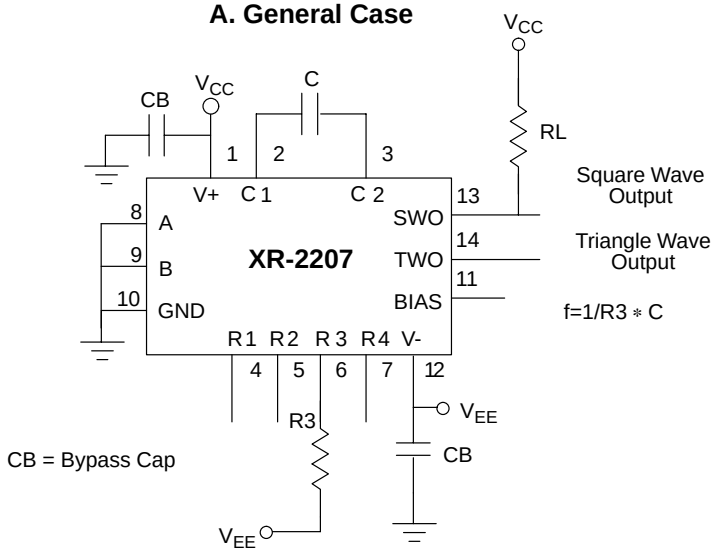
The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5kΩ) to the positive supply. The triangle waveform obtained at pin 14 is centered about ground and has a peak amplitude of $V^+/2$.

Note

For Single-Supply Operation, Logic Levels are referenced to voltage at Pin 10.



A. General Case



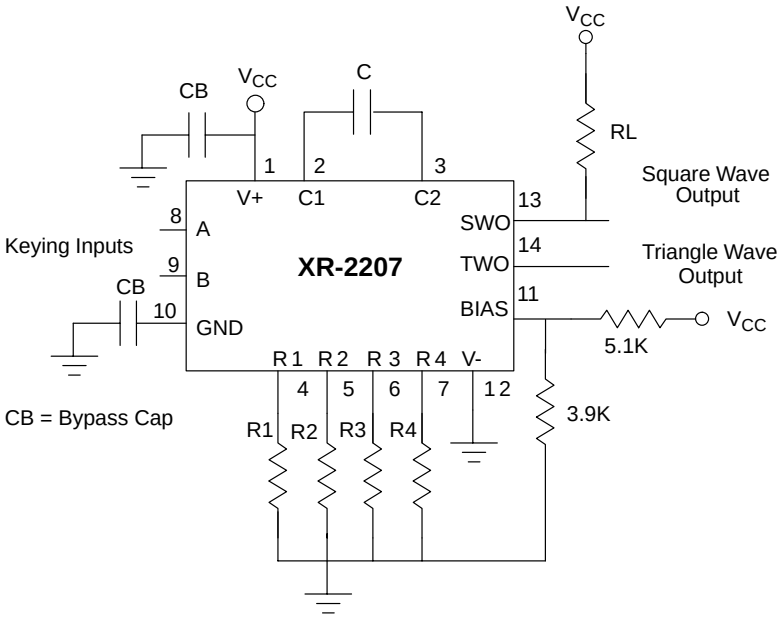
B. Fixed Frequency Case

Figure 13. Split-Supply Operation

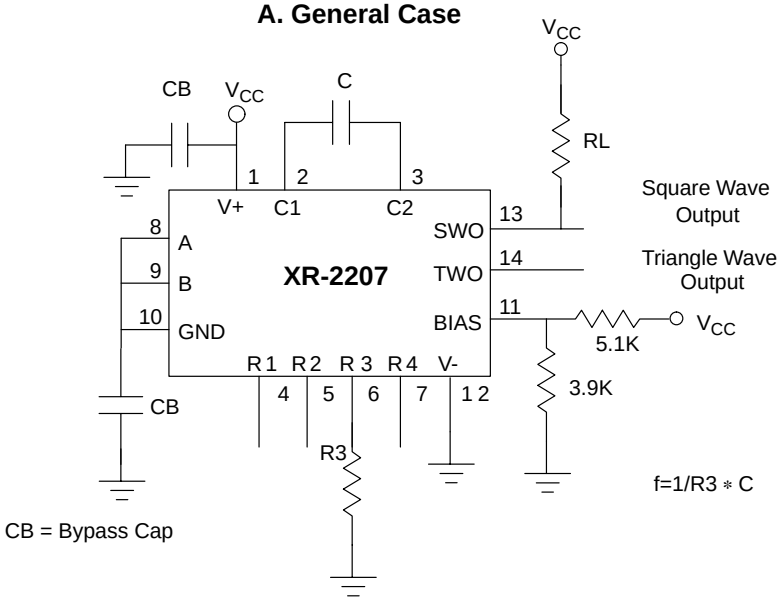
Single Supply Operation

The circuit should be interconnected as shown in *Figure 14A* or *Figure 14B* for single supply operation. Pin 12 should be grounded, and pin 11 biased from V_{CC} through a resistive divider to a value of bias voltage between $V^+/3$ and $V^+/2$. Pin 10 is bypassed to ground through a 1µF capacitor.

For single supply operation, the DC voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately 0.6V above V_B, the bias voltage at pin 11. The logic levels at the binary keying terminals are referenced to the voltage at pin 10.



A. General Case



B. Single Frequency

Figure 14. Single Supply Operation

Frequency Control (Sweep and FM)

The frequency of operation is controlled by varying the total timing current, I_T, drawn from the activated timing pins 4, 5, 6, or 7. The timing current can be modulated by applying a control voltage, V_C, to the activated timing pin through a series resistor R_C. As the control voltage becomes more negative, both the total timing current, I_T, and the oscillation frequency increase.

The circuits given in *Figure 15* and *Figure 16* show two different frequency sweep methods for split supply operation.

Both binary keying inputs are grounded for the circuit in *Figure 15*. Therefore, only timing pin 6 is activated.

The frequency of operation, normally $f = \frac{1}{R_3 C}$ is now proportional to the control voltage, V_C, and determined as:

$$f = \frac{1}{R_3 C}\left[1 - \frac{V_C R_3}{R_C V^-}\right] Hz$$

If R_3 = 2MΩ, R_C = 2kΩ, C = 5000pF, then a 1000:1 frequency sweep would result for a negative sweep voltage $V_C \approx V^-$.

The voltage to frequency conversion gain, K, is controlled by the series resistance RC and can be expressed as:

$$K = \frac{\Delta f}{\Delta V_C} = \frac{1}{R_C C V^-} \; Hz/V$$

The circuit of *Figure 15* can operate both with positive and negative values of control voltage. However, for positive values of V_C with small (R_C/R_3) ratio, the direction of the timing current I_T is reversed and the oscillations will stop.

Figure 16 shows an alternate circuit for frequency control where two timing pins, 6 and 7, are activated. The frequency and the conversion gain expressions are the same as before, except that the circuit will operate only with negative values of V_C. For $V_C > 0$, pin 7 becomes deactivated and the frequency is fixed at:

$$f = \frac{1}{R_3}$$

The circuit given in *Figure 17* shows the frequency sweep method for single supply operation. Here, the oscillation frequency is given as:

$$f = \frac{1}{R_3 C}\left[1 + \frac{R_3}{R_C}\left(1 - \frac{V_C}{V_T}\right)\right]$$

where VT = Vbias + 0.7V.

This equation is valid from VC = 0V (RC is in parallel with R3) to

$$V_C = V_T\left(1 + \frac{R_C}{R_3}\right)$$

Caution
Total timing current I_T must be less than 6mA over the frequency control range.

$$f = \frac{1}{CR_3}\left[1 - \frac{V_C R_3}{R_C V^-}\right]$$

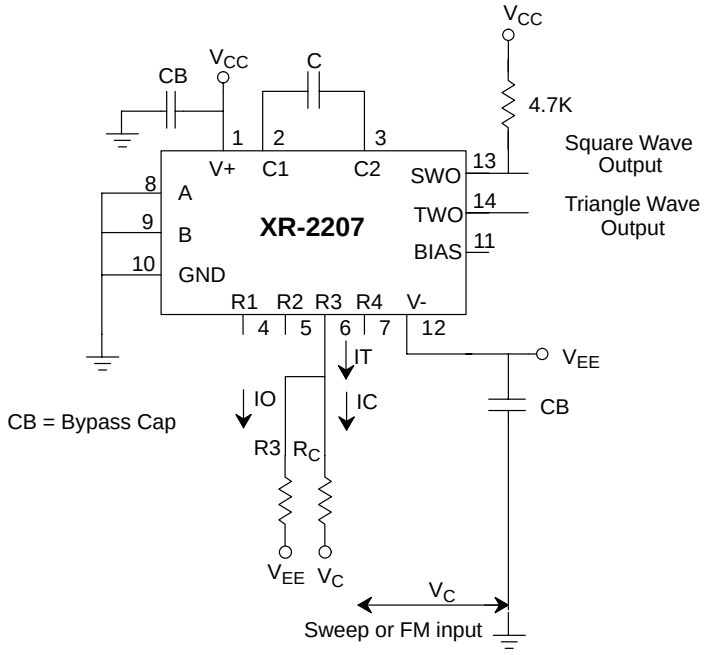


Figure 15. Frequency Sweep Operation, Split Supply

$$f = \frac{1}{CR_3}\left[1 - \frac{V_C R_3}{R_C V^-}\right]$$

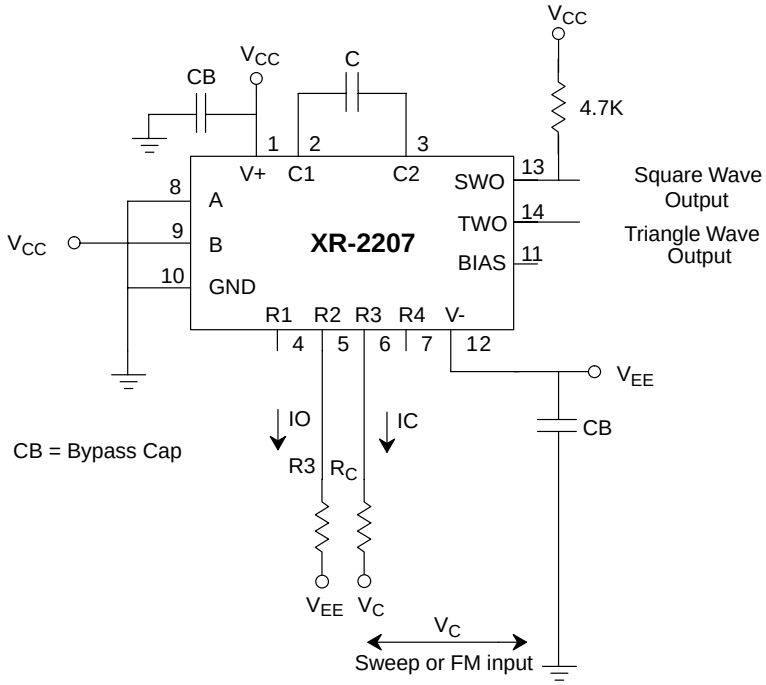


Figure 16. Alternate Frequency Sweep Operation, Split Supply

$$f = \frac{1}{CR_3}\left[1 + \frac{R_3}{R_C}\left(1 - \frac{V_C}{V_T}\right)\right]$$

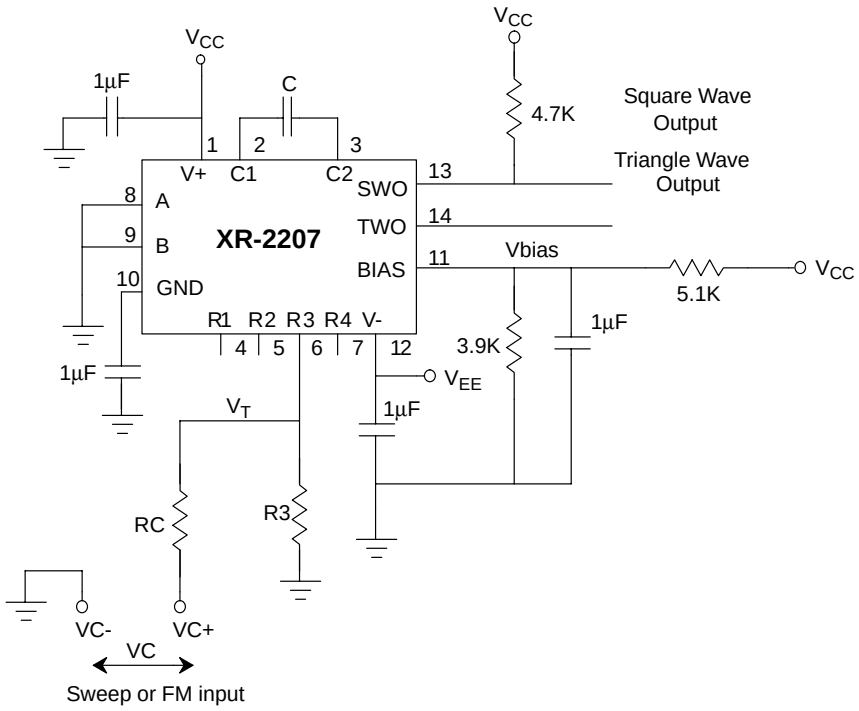


Figure 17. Frequency Sweep Operation, Single Supply

Duty Cycle Control

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pins 8 or 9) to the squarewave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveforms.

Figure 18 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the "0,0" and the "1,0" logic states given in *Table 1*. Timing pin 5 is activated when the output is "high," and the timing pin is activated when the squarewave output goes to a low state.

The duty cycle of the output waveforms is given as:

$$Duty\ Cycle = \frac{R_2}{R_2 + R_3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f, is given as:

$$f = \frac{2}{C}\left[\frac{1}{R_2 + R_3}\right]$$

The frequency can be modulated or swept without changing the duty cycle by connecting R_2 and R_3 to a common control voltage V_C, instead of V_{EE} (see *Figure 15*). The sawtooth and the pulse output waveforms are shown in *Figure 19*.

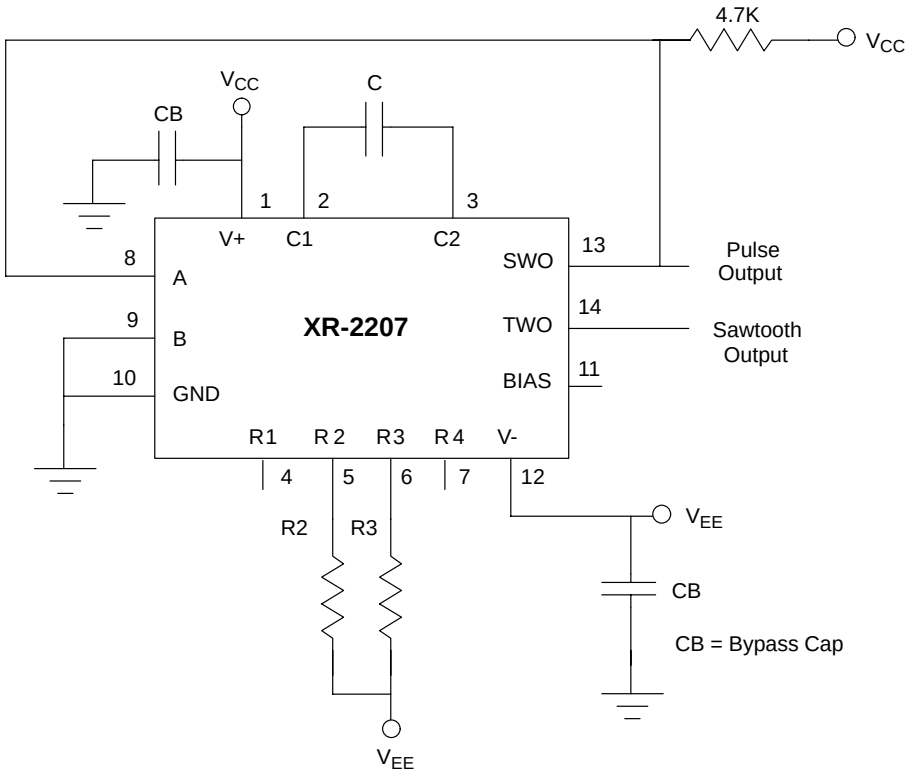
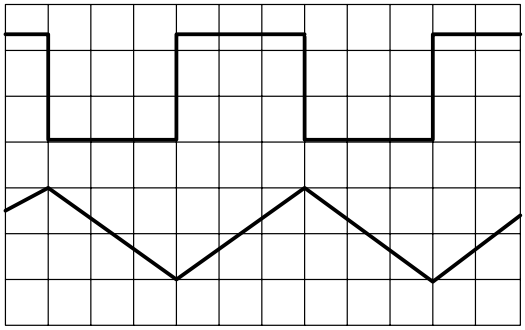
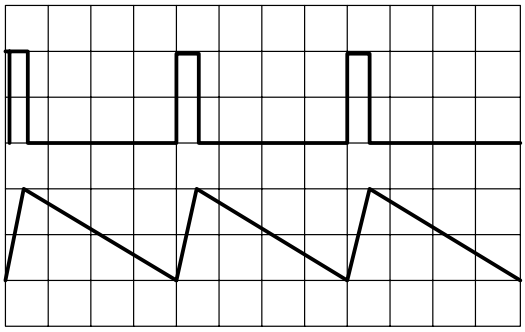


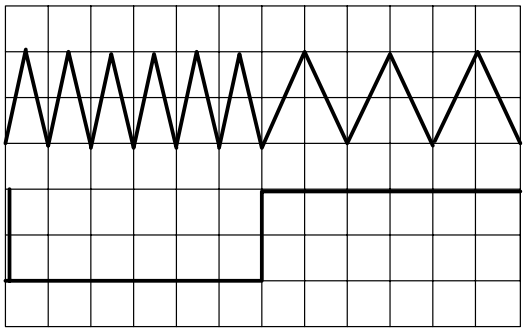
Figure 18. Duty Cycle Control



A. Squarewave and Triangle Outputs



B. Pulse and Sawtooth Outputs



C. Frequency Shift Keyed Outputs

Figure 19. Output Waveforms

On-Off Keying

The XR-2207 can be keyed on and off by simply activating an open circuited timing pin. Under certain conditions, the circuit may exhibit very low frequency (<1Hz) residual oscillations in the "off" state due to internal bias currents. If this effect is undesirable, it can be eliminated by connecting a 10MΩ resistor from pin 3 to V_{CC}.

Two-Channel FSK Generator (Modem Transmitter)

The multi-level frequency shift-keying capability of XR-2207 makes it ideally suited for two-channel FSK generation. A recommended circuit connection for this application is shown in *Figure 20*.

For two-channel FSK generation, the "mark" and "space" frequencies of the respective channels are determined by the timing resistor pairs (R_1, R_2) and (R_3, R_4). Pin 8 is the "channel-select" control in accord with *Figure 11*. For a "high" logic level at pin 8, the timing resistors R_1 and R_2 are activated. Similarly, for a "low" logic level, timing resistors R_3 and R_4 are enabled.

The "high" and "low" logic levels at pin 9 determine the respective high and low frequencies within the selected FSK channel. When only a single FSK channel is used, the remaining channel can be deactivated by connecting pin 8 to either V_{CC} or ground. In this case, the unused timing resistors can also be omitted from the circuit.

The low and high frequencies, f_1 and f_2, for a given FSK channel can be fine tuned using potentiometers connected in series with respective timing resistors. In fine tuning the frequencies, f_1 should be set first with the logic level at pin 9 in a "low" level.

Typical frequency drift of the circuit for 0°C to 75°C operation is ±0.2%. Since the frequency stability is directly related to the external timing components, care must be taken to use timing components with low temperature coefficients.

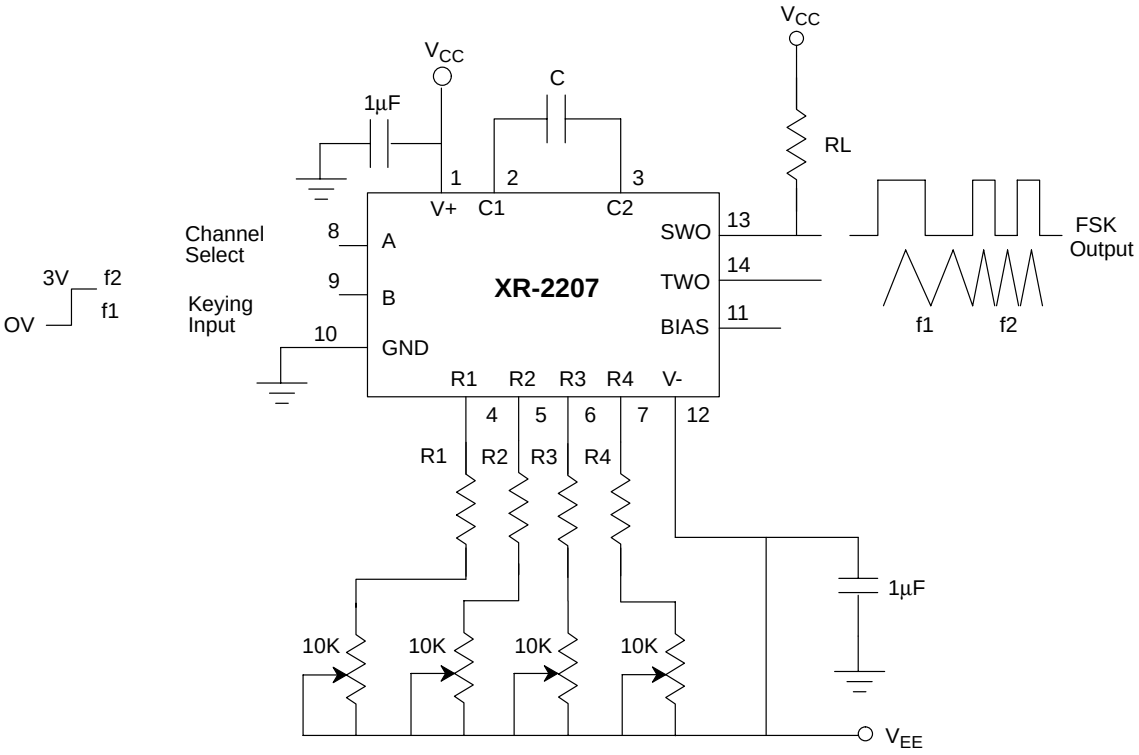
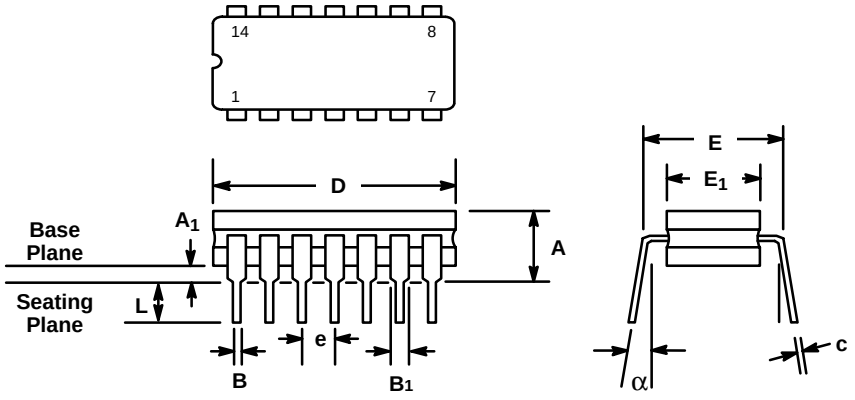


Figure 20. Multi-Channel FSK Generation

14 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

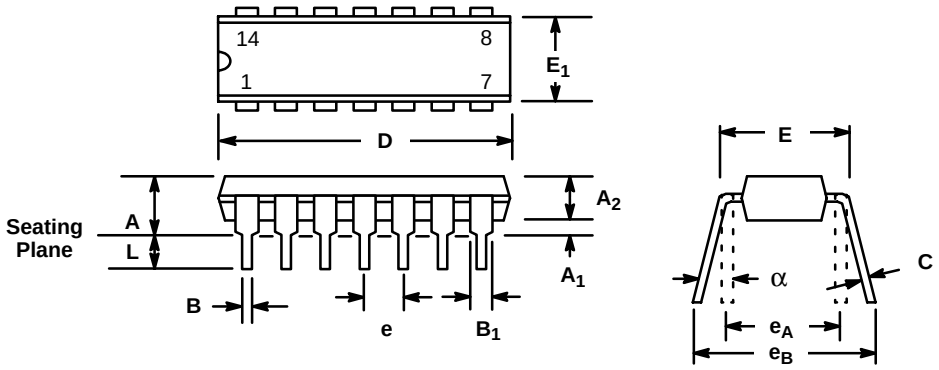


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.685	0.785	17.40	19.94
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

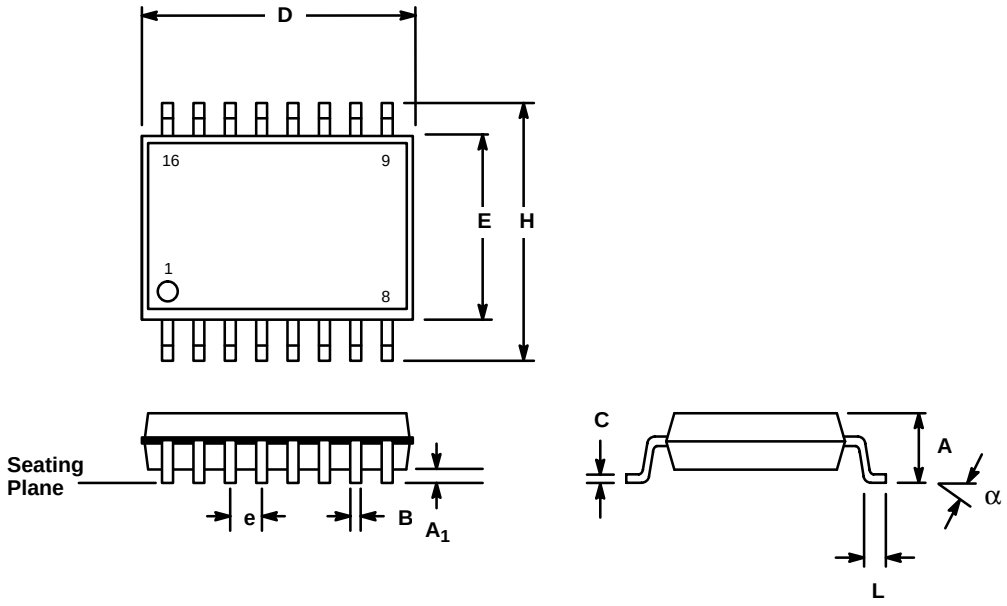


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.725	0.795	18.42	20.19
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

16 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

Notes

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Datasheet June 1997