

# DATA SHEET

# NEC

## MOS INTEGRATED CIRCUIT

# μPD4264805, 42S65805, 4265805

### 64 M-BIT DYNAMIC RAM 8 M-WORD BY 8-BIT, EDO

#### Description

The μPD4264805, 42S65805, 4265805 are 8,388,608 words by 8 bits CMOS dynamic RAMs with optional EDO. EDO is a kind of the page mode and is useful for the read operation. Besides, the μPD42S65805 can execute  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh. These are packaged in 32-pin plastic TSOP (II) and 32-pin plastic SOJ.

#### Features

- EDO (Hyper page mode)
- 8,388,608 words by 8 bits organization
- Single +3.3 V ±0.3 V power supply
- Fast access and cycle time

★

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	EDO (Hyper page mode) cycle time (MIN.)
μPD4264805-A50	378 mW	50 ns	84 ns	20 ns
μPD42S65805-A50, 4265805-A50	486 mW			
μPD4264805-A60	342 mW	60 ns	104 ns	25 ns
μPD42S65805-A60, 4265805-A60	414 mW			

★

- The μPD42S65805 can execute  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh.

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S65805	4,096 cycles/128 ms	$\overline{\text{RAS}}$ only refresh, Normal read/write, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh	0.72 mW (CMOS level input)
μPD4264805	8,192 cycles/64 ms	$\overline{\text{RAS}}$ only refresh, Normal read/write	1.8 mW (CMOS level input)
	4,096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh	
μPD4265805	4,096 cycles/64 ms	$\overline{\text{RAS}}$ only refresh, Normal read/write, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh	

The information in this document is subject to change without notice.

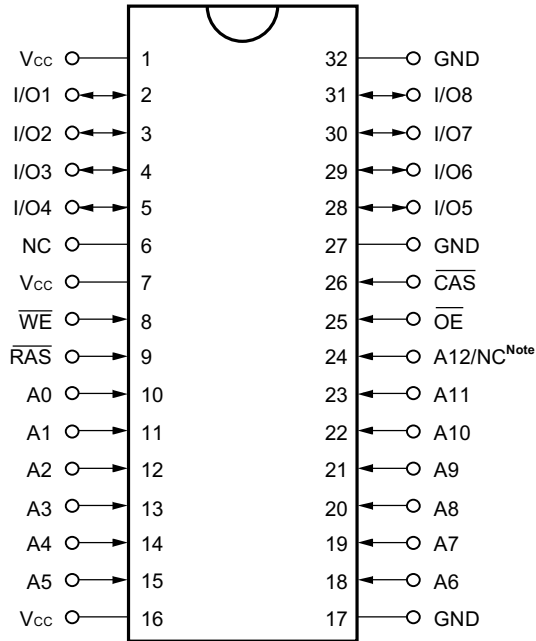
★ Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S65805G5-A50-7JD	50 ns	32-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S65805G5-A60-7JD	60 ns		
μPD42S65805LE-A50	50 ns	32-pin plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S65805LE-A60	60 ns		
μPD4264805G5-A50-7JD	50 ns	32-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD4264805G5-A60-7JD	60 ns		
μPD4265805G5-A50-7JD	50 ns		
μPD4265805G5-A60-7JD	60 ns		
μPD4264805LE-A50	50 ns	32-pin plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD4264805LE-A60	60 ns		
μPD4265805LE-A50	50 ns		
μPD4265805LE-A60	60 ns		

★ Pin Configurations (Marking Side)

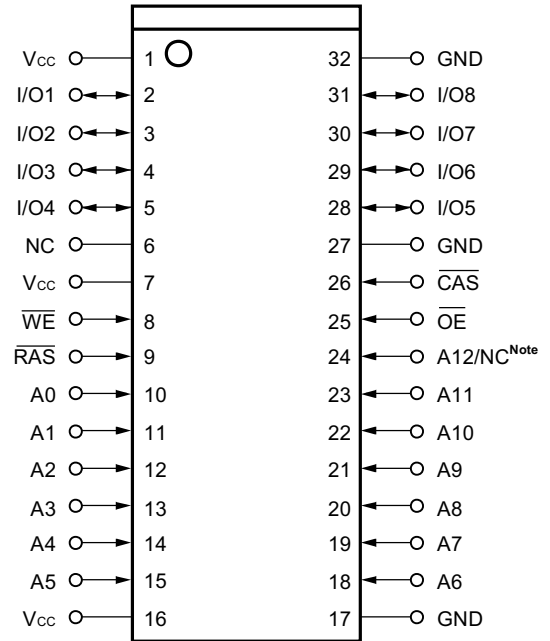
32-pin Plastic TSOP (II) (400 mil)

μPD4264805G5-7JD  
 μPD42S65805G5-7JD  
 μPD4265805G5-7JD



32-pin Plastic SOJ (400 mil)

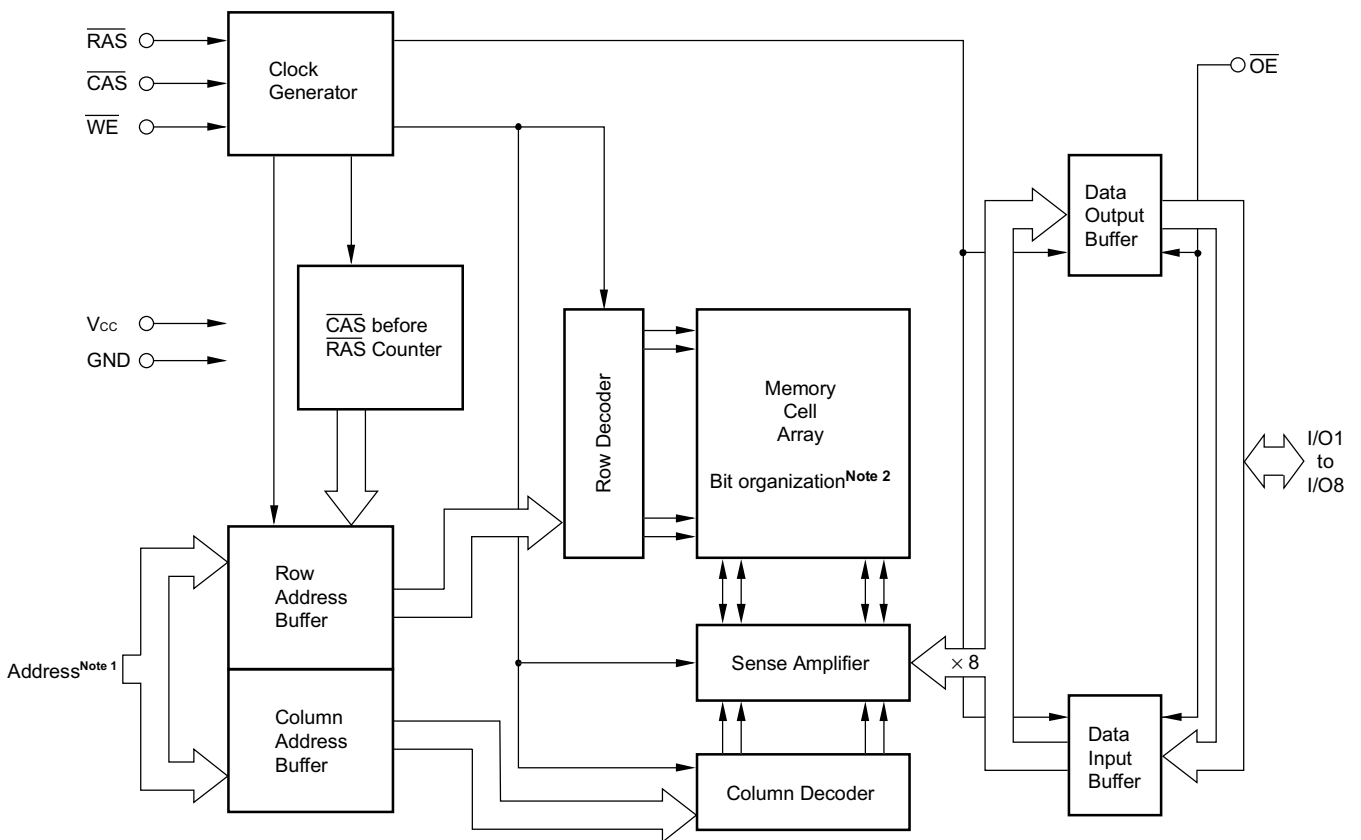
μPD4264805LE  
 μPD42S65805LE  
 μPD4265805LE



**Note** A12 ... μPD4264805  
 NC ... μPD42S65805, 4265805

- A0 to A12 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



★ Notes 1.

Part number	Row address	Column address
μPD4264805	A0 – A12	A0 – A9
μPD42S65805, 4265805	A0 – A11	A0 – A10

2. 4,096 x 2,048 x 8

**Input/Output Pin Functions**

The μPD4264805, 42S65805, 4265805 have input pins  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{OE}$ , Address<sup>Note</sup> and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A <sub>x</sub> <sup>Note</sup> (Address inputs)	Input	Address bus. Input total 23-bit of address signal, upper bits and lower bits <sup>Note</sup> in sequence (address multiplex method). Therefore, one word is selected from 8,388,608-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$ . Then, switch the address bus to column address and activate $\overline{CAS}$ . Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time ( $t_{ASR}$ , $t_{ASC}$ ) and hold time ( $t_{RAH}$ , $t_{CAH}$ ) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$ .
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ .
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{OE}$ . If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

★

**Note**

Part number	Address inputs	Upper bits	Lower bits
μPD4264805	A0 - A12	13	10
μPD42S65805, 4265805	A0 - A11	12	12

**Hyper Page Mode (EDO)**

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

**1. Data output time is extended.**

In the hyper page mode (EDO), the output data is held to the next  $\overline{\text{CAS}}$  cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the  $\overline{\text{CAS}}$  cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the  $\overline{\text{CAS}}$  cycle time becomes shorter.

**2. The  $\overline{\text{CAS}}$  cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.**

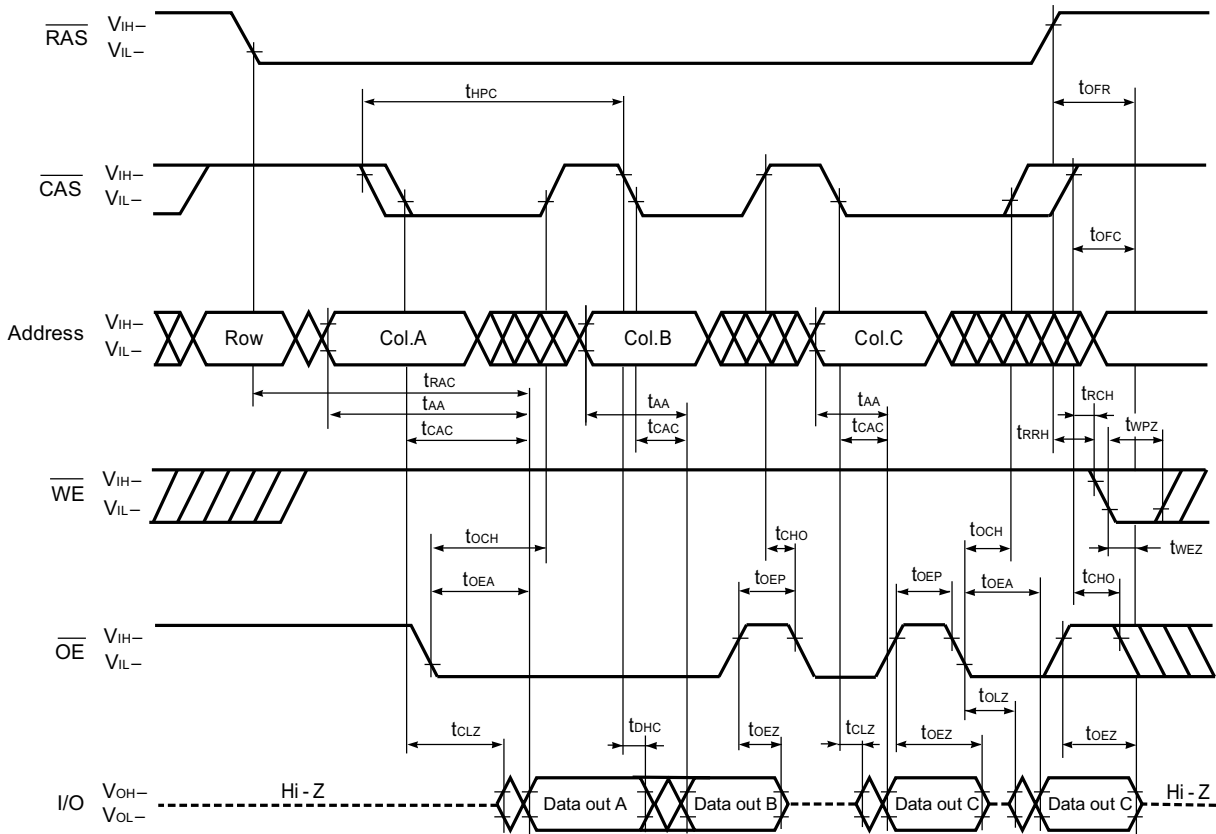
In the hyper page mode (EDO), due to the data extend function, the  $\overline{\text{CAS}}$  cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose  $t_{\text{RAC}}$  is 60 ns as an example, the  $\overline{\text{CAS}}$  cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one  $\overline{\text{RAS}}$  cycle. The hyper page mode (EDO) allows both read and write operations during one cycle.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

**Hyper Page Mode (EDO) Read Cycle**



**Cautions when using the hyper page mode (EDO)**

1.  $\overline{\text{CAS}}$  access should be used to operate  $t_{\text{HPC}}$  at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  as follows. The effective specification depends on the state of each signal.
  - (1) Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are inactive (at the end of read cycle)
    - $\overline{\text{WE}}$ : inactive,  $\overline{\text{OE}}$ : active
    - $t_{\text{OFC}}$  is effective when  $\overline{\text{RAS}}$  is inactivated before  $\overline{\text{CAS}}$  is inactivated.
    - $t_{\text{OFR}}$  is effective when  $\overline{\text{CAS}}$  is inactivated before  $\overline{\text{RAS}}$  is inactivated.
    - The slower of  $t_{\text{OFC}}$  and  $t_{\text{OFR}}$  becomes effective.
  - (2) Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are active or either  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  is active (in read cycle)
    - $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : inactive  $\cdots$   $t_{\text{OEZ}}$  is effective.
    - Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are inactive or  $\overline{\text{RAS}}$  is active and  $\overline{\text{CAS}}$  is inactive (at the end of read cycle)
      - $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : active and either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be met  $\cdots$   $t_{\text{WEZ}}$  and  $t_{\text{WPZ}}$  are effective.
      - The faster of  $t_{\text{OEZ}}$  and  $t_{\text{WEZ}}$  becomes effective.

The faster of (1) and (2) becomes effective.
3. In read cycle, the effective specification depends on the state of  $\overline{\text{CAS}}$  signal when controlling data output with the  $\overline{\text{OE}}$  signal.
  - (1)  $\overline{\text{CAS}}$ : inactive,  $\overline{\text{OE}}$ : active  $\cdots$   $t_{\text{CHO}}$  is effective.
  - (2)  $\overline{\text{CAS}}$ ,  $\overline{\text{OE}}$ : active  $\cdots$   $t_{\text{OCH}}$  is effective.

**Electrical Specifications**

- All voltages are referenced to GND.
- After power up ( $V_{CC} \geq V_{CC(MIN.)}$ ), wait more than 100 μs ( $\overline{RAS}$ ,  $\overline{CAS}$  inactive) and then, execute eight  $\overline{CAS}$  before  $\overline{RAS}$  or  $\overline{RAS}$  only refresh cycles as dummy cycles to initialize internal circuit.

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	$V_T$		-0.5 to +4.6	V
Supply voltage	$V_{CC}$		-0.5 to +4.6	V
Output current	$I_O$		50	mA
Power dissipation	$P_D$		1	W
Operating ambient temperature	$T_A$		0 to +70	°C
Storage temperature	$T_{stg}$		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	$V_{CC}$		3.0	3.3	3.6	V
High level input voltage	$V_{IH}$		2.0		$V_{CC} + 0.3$	V
Low level input voltage	$V_{IL}$		-0.3		+0.8	V
Operating ambient temperature	$T_A$		0		70	°C

**Capacitance ( $T_A = 25\text{ °C}$ ,  $f = 1\text{ MHz}$ )**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{I1}$	Address			5	pF
	$C_{I2}$	$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

★ DC Characteristics (Recommended operating conditions unless otherwise noted)

[μPD4264805]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I <sub>CC1</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling		105	mA	1, 2, 3
		$t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	95		
Standby current	I <sub>CC2</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$		1.0	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$		0.5		
$\overline{\text{RAS}}$ only refresh current	I <sub>CC3</sub>	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}$		105	mA	1, 2, 3, 4
		$t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	95		
Operating current (Hyper page mode (EDO))	I <sub>CC4</sub>	$\overline{\text{RAS}} \leq V_{\text{IL (MAX.)}}, \overline{\text{CAS}}$ cycling		105	mA	1, 2, 5
		$t_{\text{HPC}} = t_{\text{HPC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	95		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I <sub>CC5</sub>	$\overline{\text{RAS}}$ cycling		135	mA	1, 2
		$t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	115		
Input leakage current	I <sub>I (L)</sub>	$V_{\text{I}} = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V	-5	+5	μA	
Output leakage current	I <sub>O (L)</sub>	$V_{\text{O}} = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage	V <sub>OH</sub>	$I_{\text{O}} = -2.0 \text{ mA}$	2.4		V	
Low level output voltage	V <sub>OL</sub>	$I_{\text{O}} = +2.0 \text{ mA}$		0.4	V	

[μPD42S65805, 4265805]

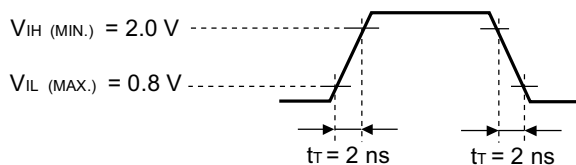
Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I <sub>CC1</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling	t <sub>RAC</sub> = 50 ns	135	mA	1, 2, 3
			t <sub>RC</sub> = t <sub>RC (MIN.)</sub> , I <sub>O</sub> = 0 mA	t <sub>RAC</sub> = 60 ns	115		
Standby current	μPD42S65805	I <sub>CC2</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH (MIN.)}$ , I <sub>O</sub> = 0 mA		1.0	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ , I <sub>O</sub> = 0 mA		0.2		
	μPD4265805	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH (MIN.)}$ , I <sub>O</sub> = 0 mA		1.0			
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ , I <sub>O</sub> = 0 mA		0.5			
$\overline{\text{RAS}}$ only refresh current		I <sub>CC3</sub>	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{IH (MIN.)}$	t <sub>RAC</sub> = 50 ns	135	mA	1, 2, 3, 4
			t <sub>RC</sub> = t <sub>RC (MIN.)</sub> , I <sub>O</sub> = 0 mA	t <sub>RAC</sub> = 60 ns	115		
Operating current (Hyper page mode (EDO))		I <sub>CC4</sub>	$\overline{\text{RAS}} \leq V_{IL (MAX.)}$ , $\overline{\text{CAS}}$ cycling	t <sub>RAC</sub> = 50 ns	105	mA	1, 2, 5
			t <sub>HPC</sub> = t <sub>HPC (MIN.)</sub> , I <sub>O</sub> = 0 mA	t <sub>RAC</sub> = 60 ns	95		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I <sub>CC5</sub>	$\overline{\text{RAS}}$ cycling	t <sub>RAC</sub> = 50 ns	135	mA	1, 2
			t <sub>RC</sub> = t <sub>RC (MIN.)</sub> , I <sub>O</sub> = 0 mA	t <sub>RAC</sub> = 60 ns	115		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (4,096 cycles/128 ms, only for the μPD42S65805)		I <sub>CC6</sub>	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: t <sub>RC</sub> = 31.3 μs $\overline{\text{RAS}}, \overline{\text{CAS}}$ : V <sub>CC</sub> - 0.2 V ≤ V <sub>IH</sub> ≤ V <sub>IH (MAX.)</sub> 0 V ≤ V <sub>IL</sub> ≤ 0.2 V	t <sub>RAS</sub> ≤ 300 ns	500	μA	1, 2
			Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Address: V <sub>IH</sub> or V <sub>IL</sub> WE, OE: V <sub>IH</sub> I <sub>O</sub> = 0 mA	t <sub>RAS</sub> ≤ 1 μs	600	μA	1, 2
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh current (only for the μPD42S65805)		I <sub>CC7</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}}$ : t <sub>RASS</sub> = 5 ms V <sub>CC</sub> - 0.2 V ≤ V <sub>IH</sub> ≤ V <sub>IH (MAX.)</sub> 0 V ≤ V <sub>IL</sub> ≤ 0.2 V I <sub>O</sub> = 0 mA		400	μA	2
Input leakage current		I <sub>I (L)</sub>	V <sub>I</sub> = 0 to 3.6 V All other pins not under test = 0 V	-5	+5	μA	
Output leakage current		I <sub>O (L)</sub>	V <sub>O</sub> = 0 to 3.6 V Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage		V <sub>OH</sub>	I <sub>O</sub> = -2.0 mA	2.4		V	
Low level output voltage		V <sub>OL</sub>	I <sub>O</sub> = +2.0 mA		0.4	V	

- Notes**
- I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub>, I<sub>CC5</sub> and I<sub>CC6</sub> depend on cycle rates (t<sub>RC</sub> and t<sub>HPC</sub>).
  - Specified values are obtained with outputs unloaded.
  - I<sub>CC1</sub> and I<sub>CC3</sub> are measured assuming that address can be changed once or less during  $\overline{\text{RAS}} \leq V_{IL (MAX.)}$  and  $\overline{\text{CAS}} \geq V_{IH (MIN.)}$ .
  - I<sub>CC3</sub> is measured assuming that all column address inputs are held at either high or low.
  - I<sub>CC4</sub> is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

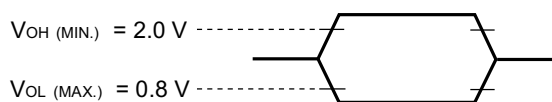
**AC Characteristics (Recommended Operating Conditions unless otherwise noted)**

**AC Characteristics Test Conditions**

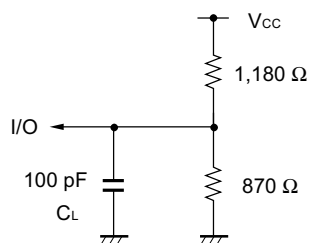
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



**Common to Read, Write, Read Modify Write Cycle**

Parameter	Symbol	trac = 50 ns		trac = 60 ns		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.			
Read / Write cycle time	t <sub>RC</sub>	84	–	104	–	ns		
$\overline{\text{RAS}}$ precharge time	t <sub>RP</sub>	30	–	40	–	ns		
$\overline{\text{CAS}}$ precharge time	t <sub>CPN</sub>	7	–	10	–	ns		
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	50	10,000	60	10,000	ns	1	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	8	10,000	10	10,000	ns		
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	13	–	15	–	ns		
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	38	–	40	–	ns		
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RCD</sub>	11	37	14	45	ns	2	
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAD</sub>	9	25	12	30	ns	2	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	5	–	5	–	ns	3	
Row address setup time	t <sub>ASR</sub>	0	–	0	–	ns		
Row address hold time	t <sub>RAH</sub>	7	–	10	–	ns		
Column address setup time	t <sub>ASC</sub>	0	–	0	–	ns		
Column address hold time	t <sub>CAH</sub>	7	–	10	–	ns		
$\overline{\text{OE}}$ lead time referenced to $\overline{\text{RAS}}$	t <sub>OES</sub>	0	–	0	–	ns		
$\overline{\text{CAS}}$ to data setup time	t <sub>CLZ</sub>	0	–	0	–	ns		
$\overline{\text{OE}}$ to data setup time	t <sub>OLZ</sub>	0	–	0	–	ns		
$\overline{\text{OE}}$ to data delay time	t <sub>OED</sub>	10	–	13	–	ns		
Transition time (rise and fall)	t <sub>r</sub>	1	50	1	50	ns		
Refresh time	μPD42S65805	t <sub>REF</sub>	–	128	–	128	ms	4
	μPD4264805, 4265805	t <sub>REF</sub>	–	64	–	64	ms	

★

- Notes 1.** In  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles,  $t_{\text{RAS(MAX)}}$  is 100 μs.  
 If  $10 \mu\text{s} < t_{\text{RAS}} < 100 \mu\text{s}$ ,  $\overline{\text{RAS}}$  precharge time for  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh ( $t_{\text{RPS}}$ ) is applied.
- 2.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{RAC (MAX.)}}$	$t_{\text{RAC (MAX.)}}$
$t_{\text{RAD}} > t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{AA (MAX.)}}$	$t_{\text{RAD}} + t_{\text{AA (MAX.)}}$
$t_{\text{RCD}} > t_{\text{RCD (MAX.)}}$	$t_{\text{CAC (MAX.)}}$	$t_{\text{RCD}} + t_{\text{CAC (MAX.)}}$

$t_{\text{RAD (MAX.)}}$  and  $t_{\text{RCD (MAX.)}}$  are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time ( $t_{\text{RAC}}$ ,  $t_{\text{AA}}$  or  $t_{\text{CAC}}$ ) is to be used for finding out when output data will be available. Therefore, the input conditions  $t_{\text{RAD}} \geq t_{\text{RAD (MAX.)}}$  and  $t_{\text{RCD}} \geq t_{\text{RCD (MAX.)}}$  will not cause any operation problems.

- 3.**  $t_{\text{CRP (MIN.)}}$  requirement is applied to  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  cycles.
- 4.** This specification is applied only to the μPD42S65805.

**Read Cycle**

Parameter	Symbol	$t_{\text{RAC}} = 50 \text{ ns}$		$t_{\text{RAC}} = 60 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	–	50	–	60	ns	1
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	–	13	–	15	ns	1
Access time from column address	$t_{\text{AA}}$	–	25	–	30	ns	1
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	–	13	–	15	ns	
Column address lead time referenced to $\overline{\text{RAS}}$	$t_{\text{RAL}}$	25	–	30	–	ns	
Read command setup time	$t_{\text{RCS}}$	0	–	0	–	ns	
Read command hold time referenced to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	–	0	–	ns	2
Read command hold time referenced to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{\text{OE}}$	$t_{\text{OEZ}}$	0	10	0	13	ns	3
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	$t_{\text{CHO}}$	5	–	5	–	ns	4

- Notes 1.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{RAC (MAX.)}}$	$t_{\text{RAC (MAX.)}}$
$t_{\text{RAD}} > t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{AA (MAX.)}}$	$t_{\text{RAD}} + t_{\text{AA (MAX.)}}$
$t_{\text{RCD}} > t_{\text{RCD (MAX.)}}$	$t_{\text{CAC (MAX.)}}$	$t_{\text{RCD}} + t_{\text{CAC (MAX.)}}$

$t_{\text{RAD (MAX.)}}$  and  $t_{\text{RCD (MAX.)}}$  are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time ( $t_{\text{RAC}}$ ,  $t_{\text{AA}}$  or  $t_{\text{CAC}}$ ) is to be used for finding out when output data will be available. Therefore, the input conditions  $t_{\text{RAD}} \geq t_{\text{RAD (MAX.)}}$  and  $t_{\text{RCD}} \geq t_{\text{RCD (MAX.)}}$  will not cause any operation problems.

- 2.** Either  $t_{\text{RCH (MIN.)}}$  or  $t_{\text{RRH (MIN.)}}$  should be met in read cycles.
- 3.**  $t_{\text{OEZ (MAX.)}}$  defines the time when the output achieves the condition of Hi-Z and is not referenced to  $V_{\text{OH}}$  or  $V_{\text{OL}}$ .
- 4.**  $\overline{\text{WE}}$ : inactive (in read cycle)  
 $\overline{\text{CAS}}$ : inactive,  $\overline{\text{OE}}$ : active .....  $t_{\text{CHO}}$  is effective.  
 $\overline{\text{CAS}}$ ,  $\overline{\text{OE}}$ : active .....  $t_{\text{OCH}}$  is effective.

**Write Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t <sub>WCH</sub>	7	–	10	–	ns	1
$\overline{WE}$ pulse width	t <sub>WP</sub>	7	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t <sub>RWL</sub>	13	–	15	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t <sub>CWL</sub>	7	–	10	–	ns	
$\overline{WE}$ setup time	t <sub>WCS</sub>	0	–	0	–	ns	2
$\overline{OE}$ hold time	t <sub>OEH</sub>	0	–	0	–	ns	
Data-in setup time	t <sub>DS</sub>	0	–	0	–	ns	3
Data-in hold time	t <sub>DH</sub>	7	–	10	–	ns	3

- Notes**
1. t<sub>WP (MIN.)</sub> is applied to late write cycles or read modify write cycles. In early write cycles, t<sub>WCH (MIN.)</sub> should be met.
  2. If t<sub>WCS</sub> ≥ t<sub>WCS (MIN.)</sub>, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
  3. t<sub>DS (MIN.)</sub> and t<sub>DH (MIN.)</sub> are referenced to the  $\overline{CAS}$  falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the  $\overline{WE}$  falling edge.

**Read Modify Write Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t <sub>RWC</sub>	107	–	133	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t <sub>RWD</sub>	64	–	77	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t <sub>CWD</sub>	27	–	32	–	ns	1
Column address to $\overline{WE}$ delay time	t <sub>AWD</sub>	39	–	47	–	ns	1

- Note**
1. If t<sub>WCS</sub> ≥ t<sub>WCS (MIN.)</sub>, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t<sub>RWD</sub> ≥ t<sub>RWD (MIN.)</sub>, t<sub>CWD</sub> ≥ t<sub>CWD (MIN.)</sub>, t<sub>AWD</sub> ≥ t<sub>AWD (MIN.)</sub> and t<sub>CPWD</sub> ≥ t<sub>CPWD (MIN.)</sub>, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t <sub>HPC</sub>	20	–	25	–	ns	1
$\overline{\text{RAS}}$ pulse width	t <sub>RASP</sub>	50	125,000	60	125,000	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>HCAS</sub>	8	10,000	10	10,000	ns	
$\overline{\text{CAS}}$ precharge time	t <sub>CP</sub>	7	–	10	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>ACP</sub>	–	30	–	35	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t <sub>CPWD</sub>	41	–	52	–	ns	2
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t <sub>RHCP</sub>	30	–	35	–	ns	
Read modify write cycle time	t <sub>HPRWC</sub>	52	–	66	–	ns	
Data output hold time	t <sub>DHC</sub>	5	–	5	–	ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	t <sub>OCH</sub>	5	–	5	–	ns	3
$\overline{\text{OE}}$ precharge time	t <sub>OEP</sub>	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{\text{WE}}$	t <sub>WEZ</sub>	0	10	0	13	ns	4, 5
$\overline{\text{WE}}$ pulse width	t <sub>WPZ</sub>	7	–	10	–	ns	5
Output buffer turn-off delay from $\overline{\text{RAS}}$	t <sub>OFR</sub>	0	10	0	13	ns	4, 5
Output buffer turn-off delay from $\overline{\text{CAS}}$	t <sub>OFC</sub>	0	10	0	13	ns	4, 5

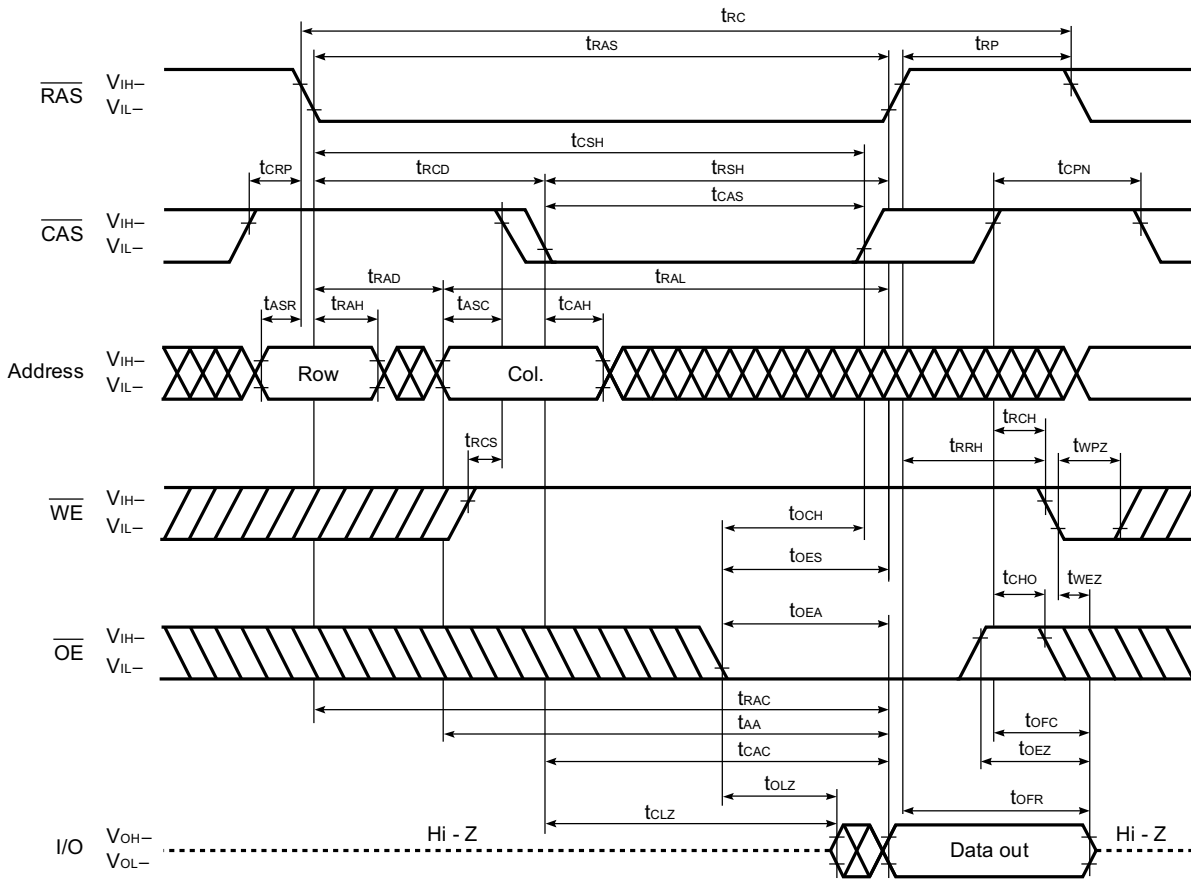
- Notes**
- t<sub>HPC</sub> (MIN.) is applied to  $\overline{\text{CAS}}$  access.
  - If t<sub>WCS</sub> ≥ t<sub>WCS</sub> (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t<sub>TRWD</sub> ≥ t<sub>TRWD</sub> (MIN.), t<sub>TCWD</sub> ≥ t<sub>TCWD</sub> (MIN.), t<sub>TAWD</sub> ≥ t<sub>TAWD</sub> (MIN.) and t<sub>CPWD</sub> ≥ t<sub>CPWD</sub> (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
  - $\overline{\text{WE}}$ : inactive (in read cycle)  
 $\overline{\text{CAS}}$ : inactive,  $\overline{\text{OE}}$ : active ..... t<sub>CHO</sub> is effective.  
 $\overline{\text{CAS}}$ ,  $\overline{\text{OE}}$ : active ..... t<sub>OCH</sub> is effective.
  - t<sub>OFC</sub> (MAX.), t<sub>OFR</sub> (MAX.) and t<sub>WEZ</sub> (MAX.) define the time when the output achieves the conditions of Hi-Z and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
  - To make I/Os to Hi-Z in read cycle, it is necessary to control  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  as follows. The effective specification depends on state of each signal.
    - Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are inactive (at the end of the read cycle)  
 $\overline{\text{WE}}$ : inactive,  $\overline{\text{OE}}$ : active  
t<sub>OFC</sub> is effective when  $\overline{\text{RAS}}$  is inactivated before  $\overline{\text{CAS}}$  is inactivated.  
t<sub>OFR</sub> is effective when  $\overline{\text{CAS}}$  is inactivated before  $\overline{\text{RAS}}$  is inactivated.  
The slower of t<sub>OFC</sub> and t<sub>OFR</sub> becomes effective.
    - Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are active or either  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  is active (in read cycle)  
 $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : inactive ..... t<sub>OEZ</sub> is effective.  
Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are inactive or  $\overline{\text{RAS}}$  is active and  $\overline{\text{CAS}}$  is inactive (at the end of read cycle)  
 $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : active and either t<sub>TRRH</sub> or t<sub>TRCH</sub> must be met ..... t<sub>WEZ</sub> and t<sub>WPZ</sub> are effective.  
The faster of t<sub>OEZ</sub> and t<sub>WEZ</sub> becomes effective.  
The faster of (1) and (2) becomes effective.

Refresh Cycle

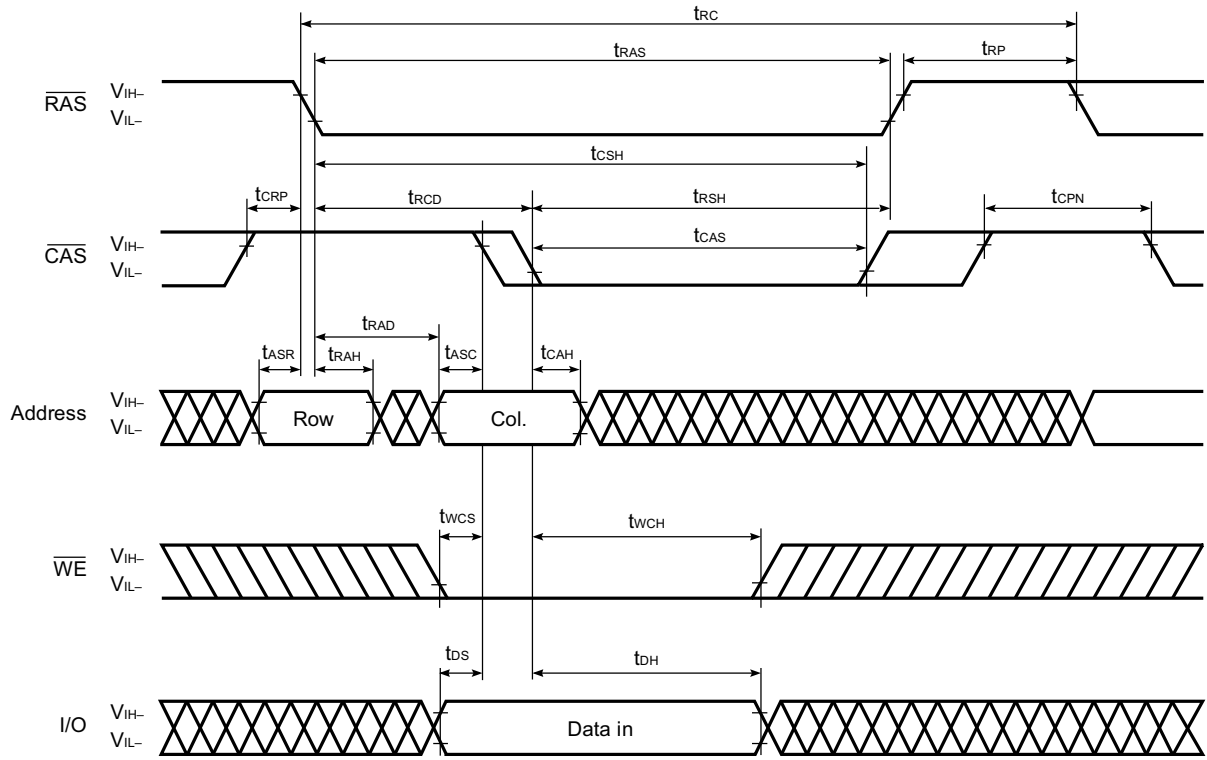
Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ setup time	t <sub>CSR</sub>	5	–	5	–	ns	
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t <sub>CHR</sub>	10	–	10	–	ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t <sub>RPC</sub>	5	–	5	–	ns	
$\overline{\text{RAS}}$ pulse width ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t <sub>RASS</sub>	100	–	100	–	μs	1
$\overline{\text{RAS}}$ precharge time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t <sub>RPS</sub>	90	–	110	–	ns	1
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t <sub>CHS</sub>	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ setup time	t <sub>WSR</sub>	10	–	10	–	ns	
$\overline{\text{WE}}$ hold time	t <sub>WHR</sub>	15	–	15	–	ns	

**Note 1.** This specification is applied only to the μPD42S65805.

Read Cycle

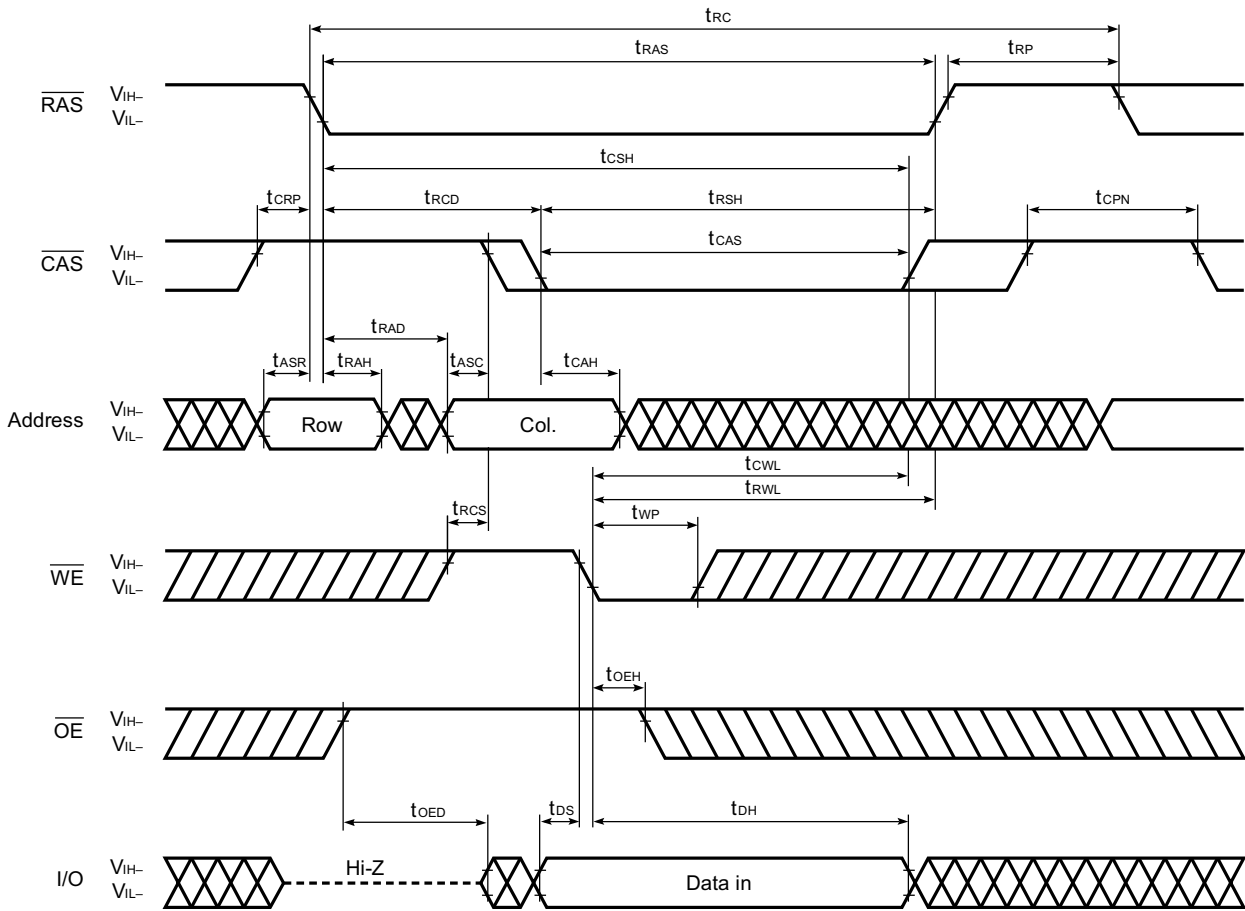


Early Write Cycle

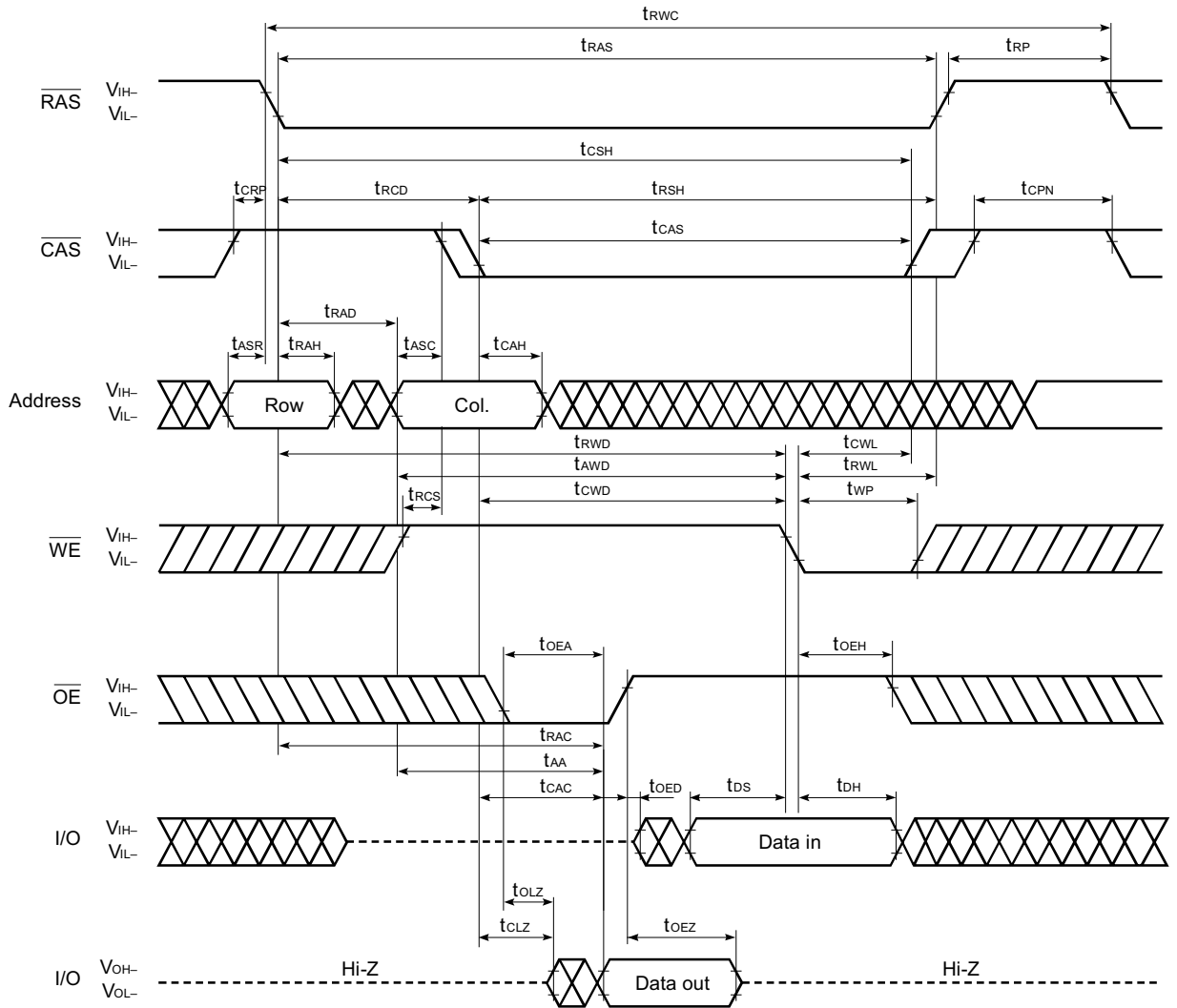


Remark  $\overline{OE}$ : Don't care

Late Write Cycle



Read Modify Write Cycle

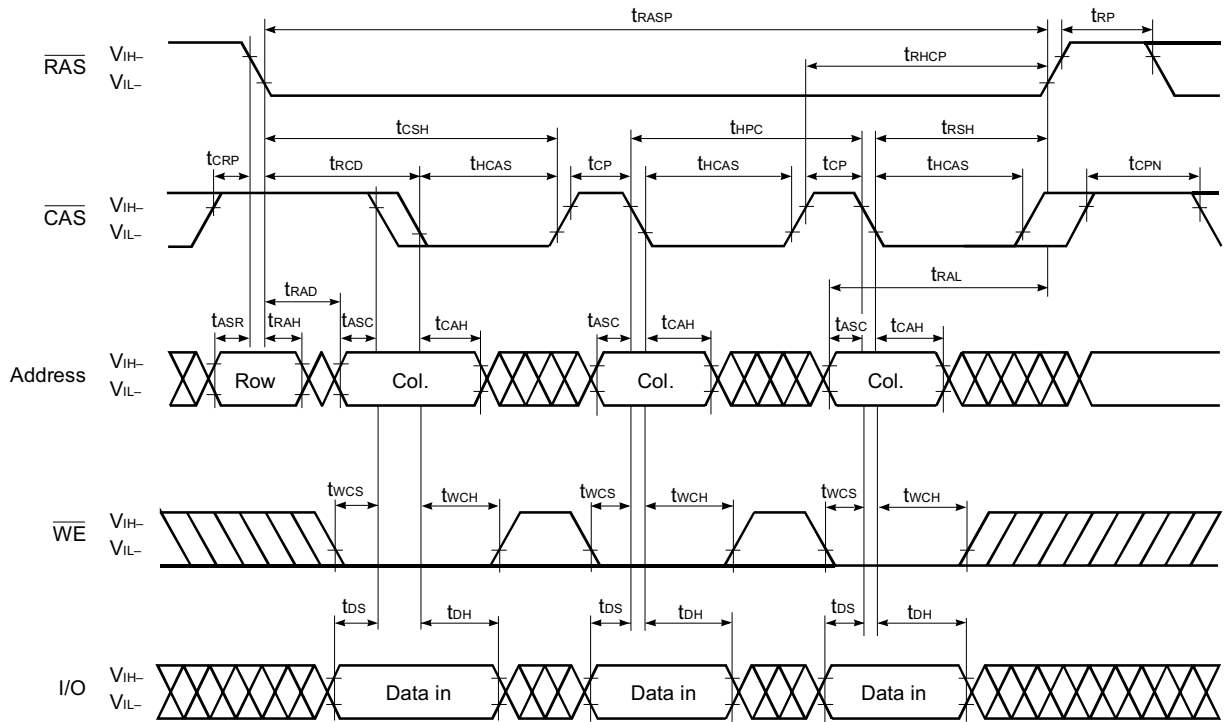






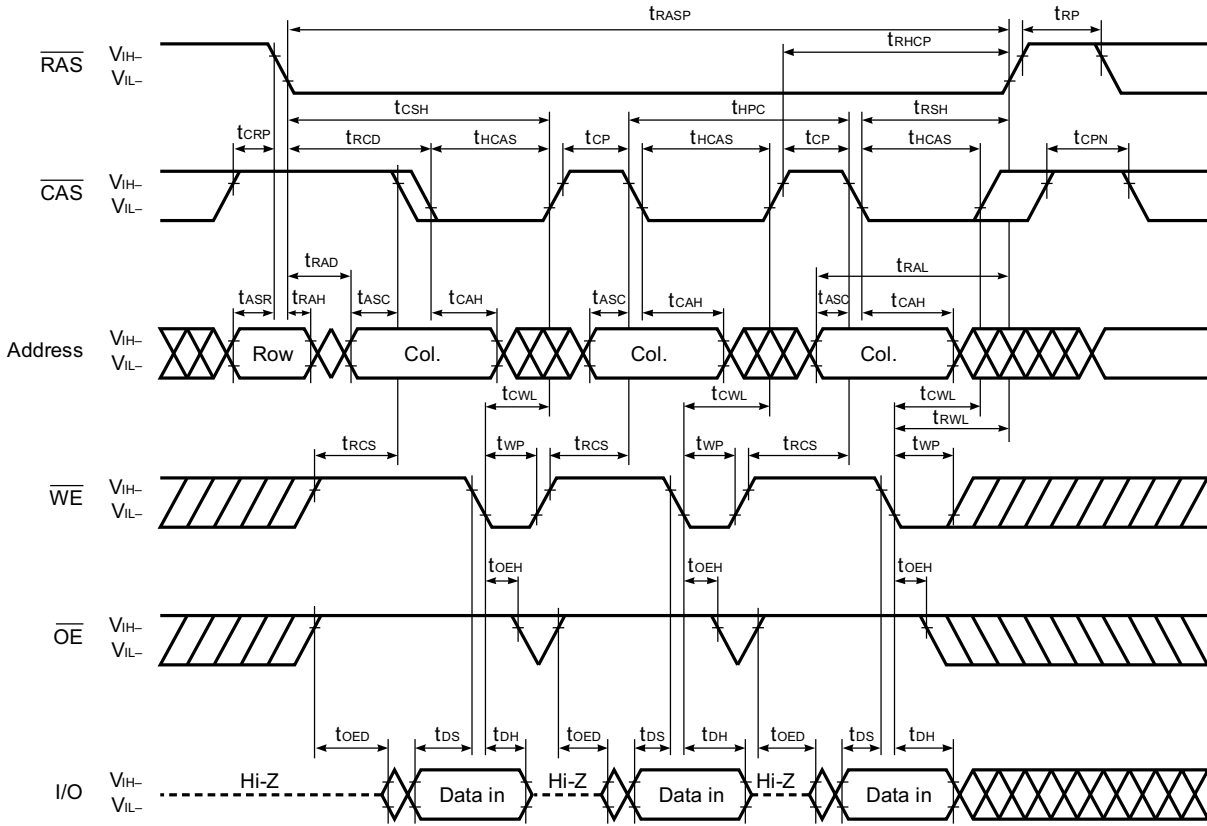


Hyper Page Mode (EDO) Early Write Cycle



- Remarks**
1.  $\overline{OE}$ : Don't care
  2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive  $\overline{CAS}$  cycles within the same  $\overline{RAS}$  cycle.

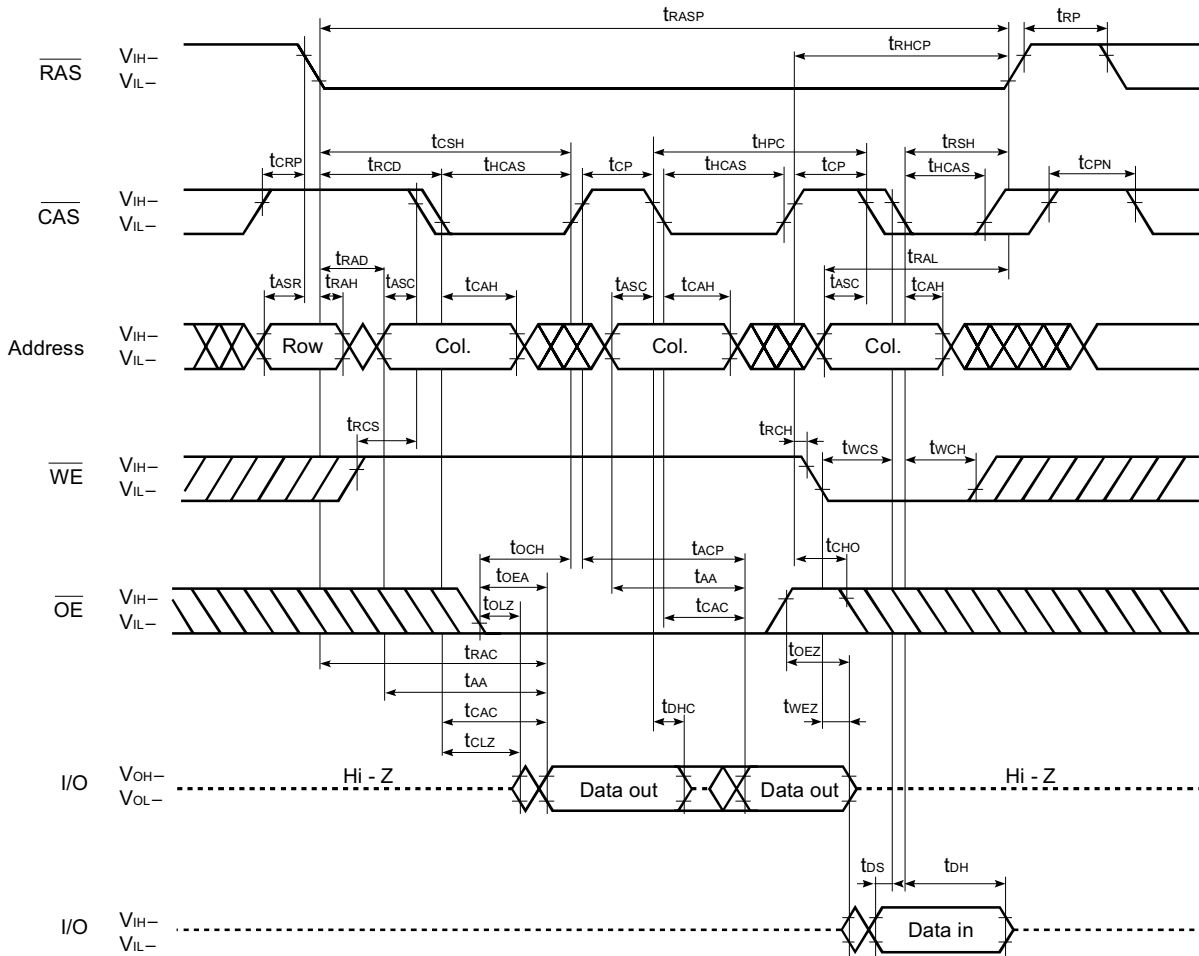
Hyper Page Mode (EDO) Late Write Cycle



**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive  $\overline{\text{CAS}}$  cycles within the same  $\overline{\text{RAS}}$  cycle.

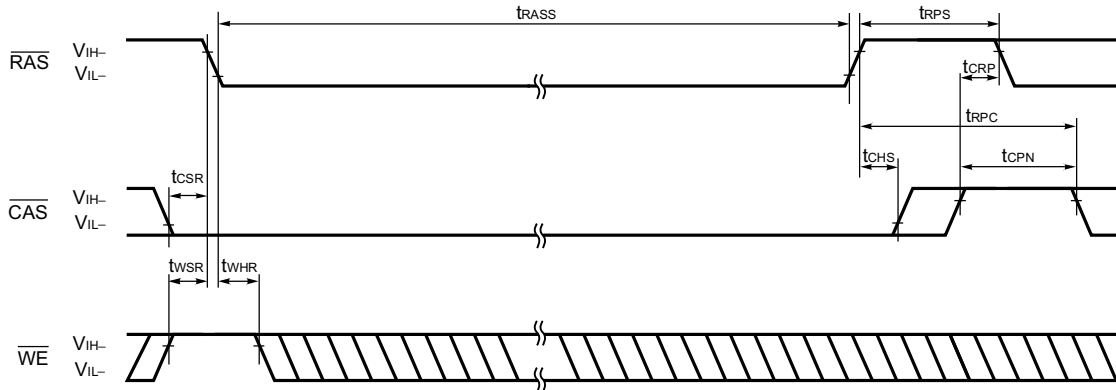


Hyper Page Mode (EDO) Read and Write Cycle



**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

★ **CAS Before RAS Self Refresh Cycle (Only for the μPD42S65805)**



**Remark** Address,  $\overline{OE}$ : Don't care I/O: Hi-Z

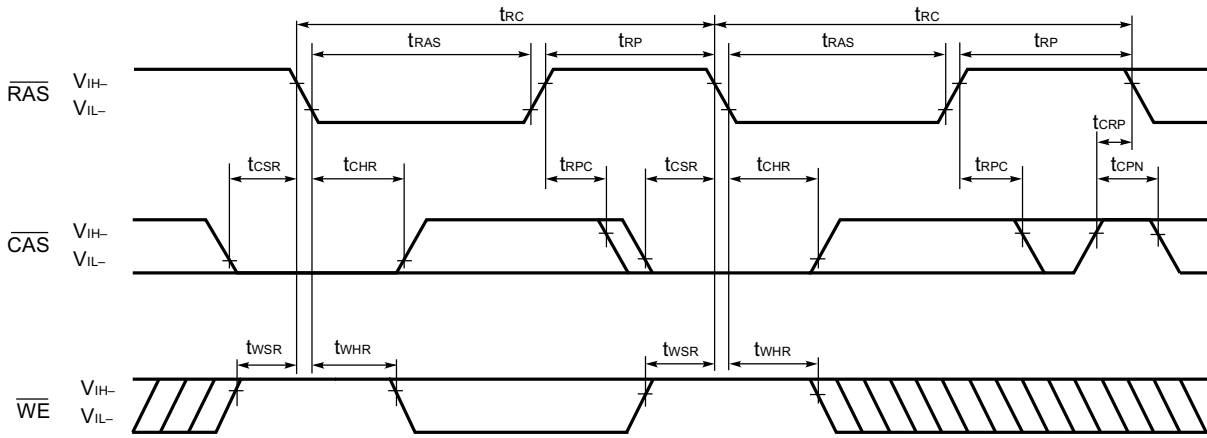
**Cautions on Use of CAS Before RAS Self Refresh**

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

- (1) **Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh**  
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 4,096 times within a 64 ms interval just before and after setting CAS before RAS self refresh.
- (2) **Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh**  
When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 4,096 times within a 64 ms interval just before and after setting CAS before RAS self refresh.
- (3) If  $t_{RASS(MIN.)}$  is not satisfied at the beginning of CAS before RAS self refresh cycles ( $t_{RAS} < 100 \mu s$ ), CAS before RAS refresh cycles will be executed one time.  
If  $10 \mu s < t_{RAS} < 100 \mu s$ , RAS precharge time for CAS before RAS self refresh ( $t_{RPS}$ ) is applied.  
And refresh cycles (4,096/128 ms) should be met.

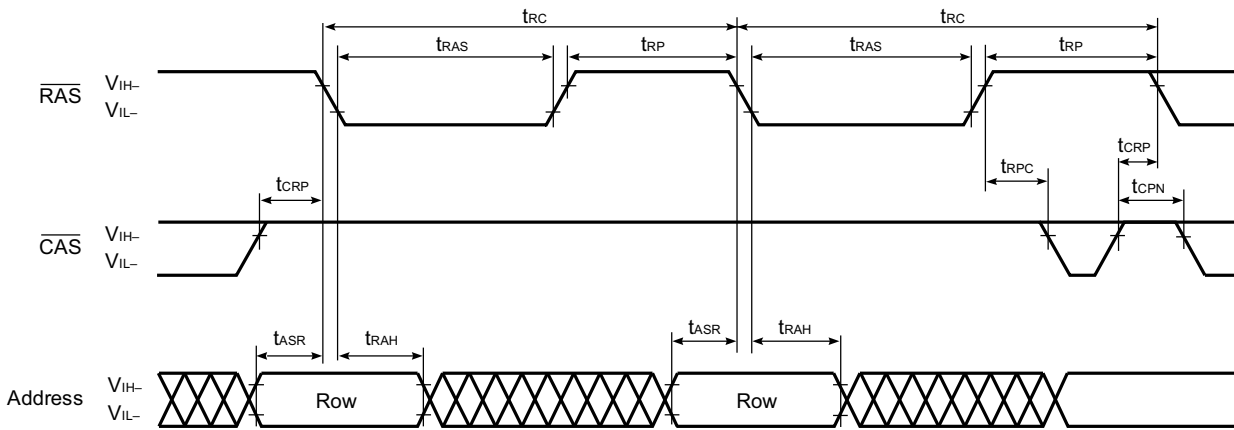
For details, please refer to **How to use DRAM** User's Manual.

**CAS Before RAS Refresh Cycle**



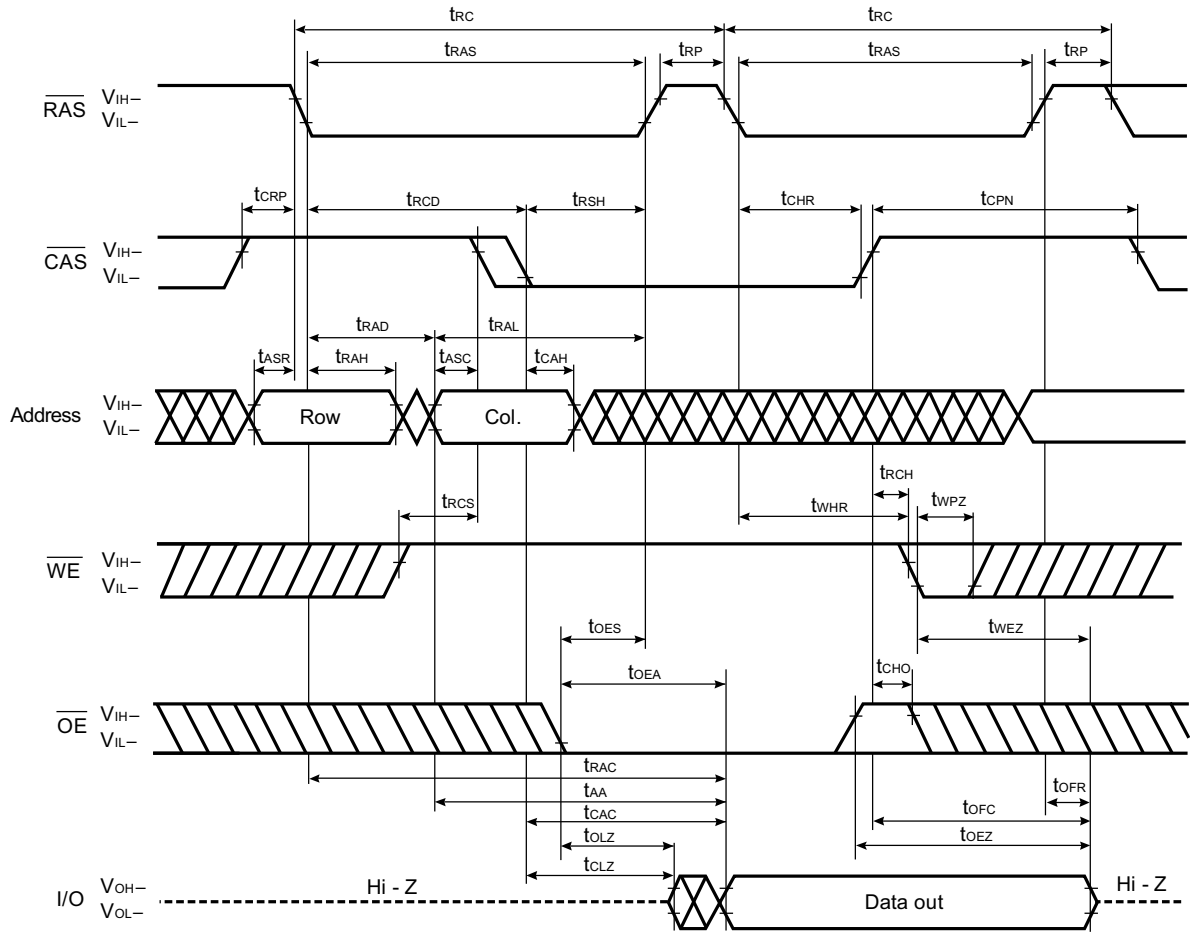
**Remark** Address,  $\overline{\text{OE}}$ : Don't care I/O: Hi-Z

**RAS Only Refresh Cycle**

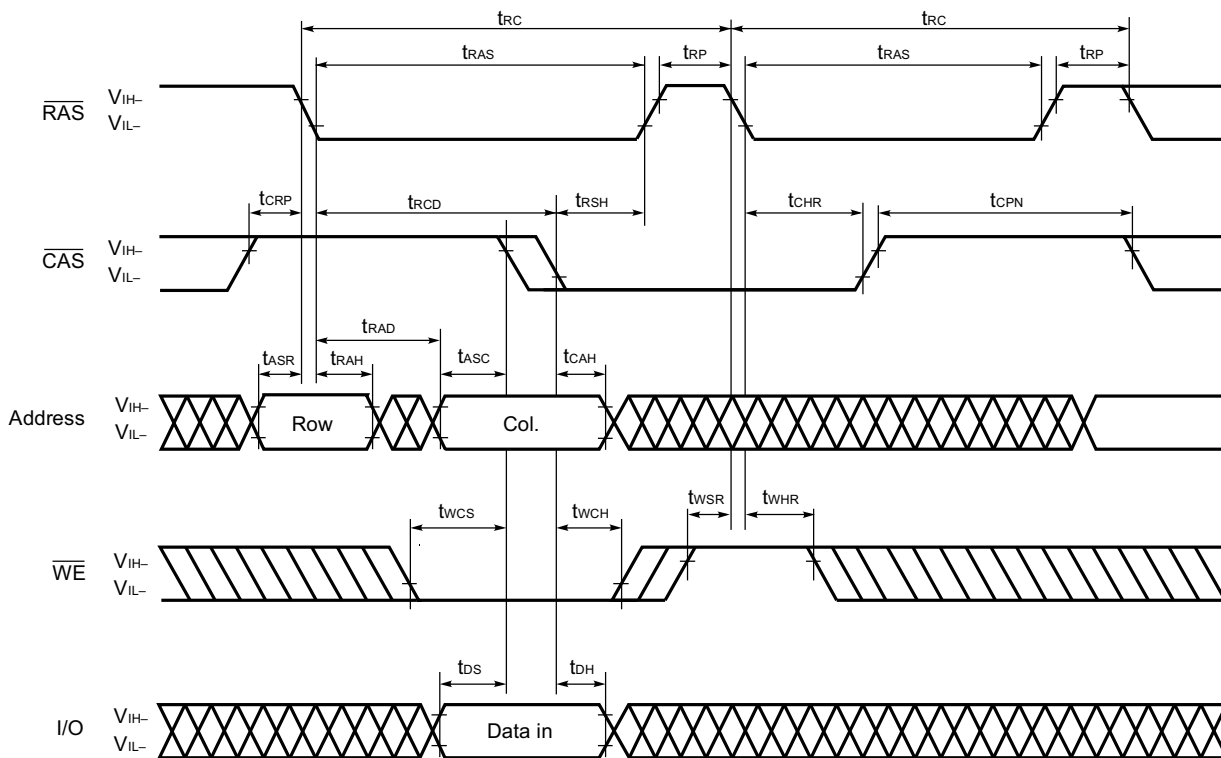


**Remark**  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



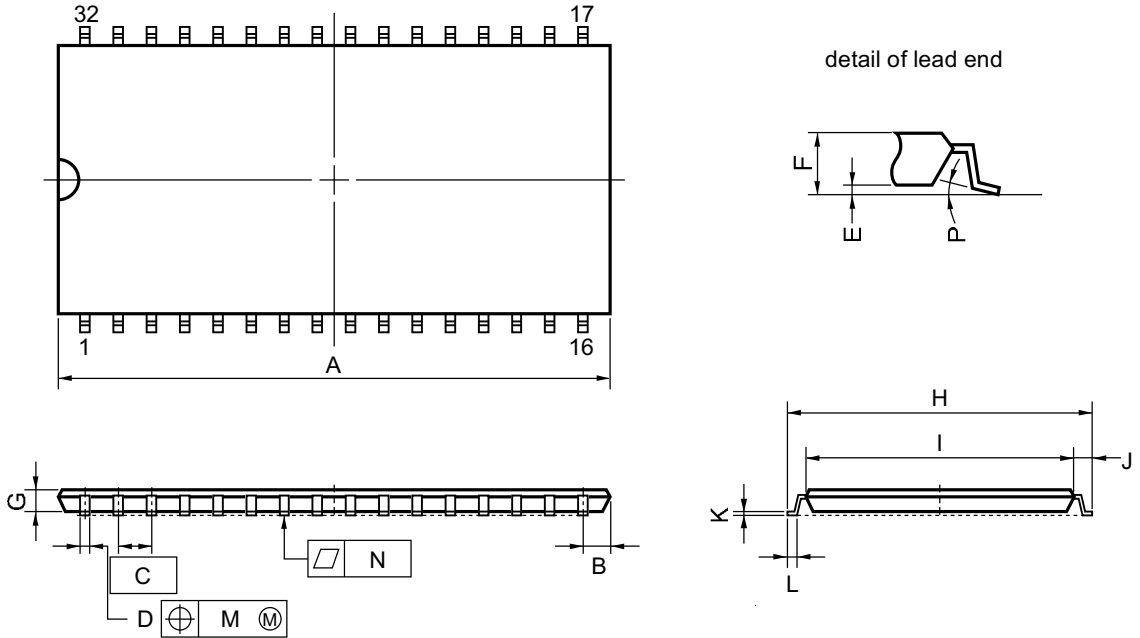
Hidden Refresh Cycle (Write)



Remark  $\overline{\text{OE}}$ : Don't care

Package Drawings

32PIN PLASTIC TSOP(II) (400 mil)



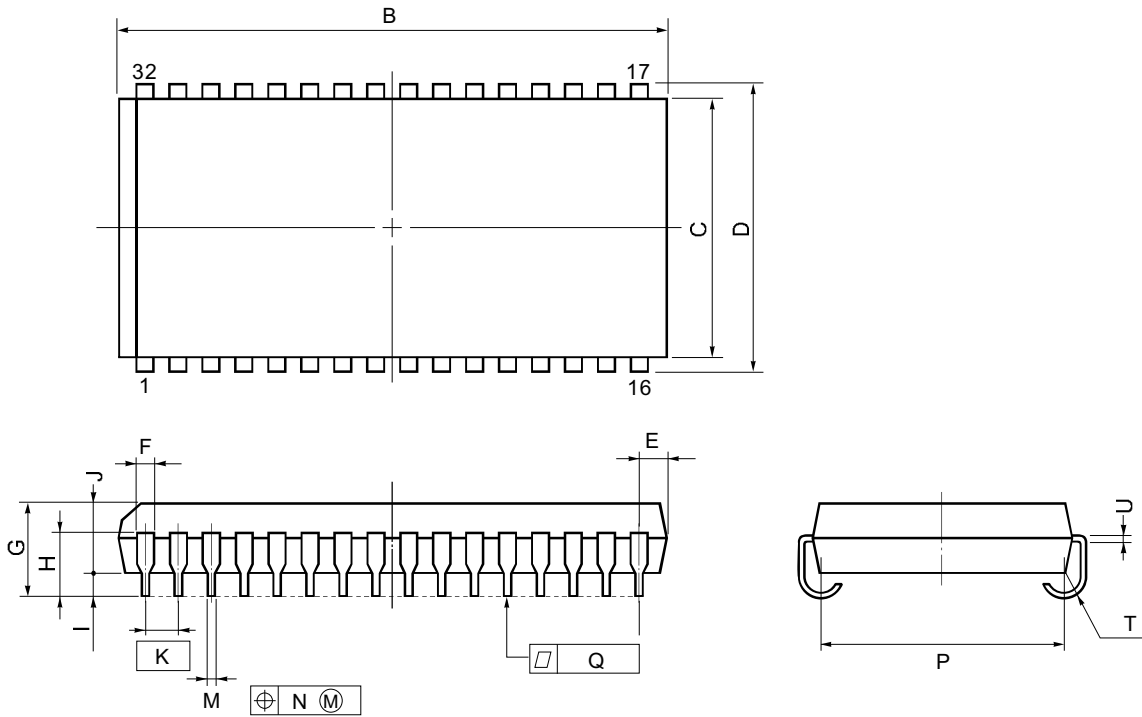
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 <sup>+0.08</sup> <sub>-0.07</sub>	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
K	0.145 <sup>+0.025</sup> <sub>-0.015</sub>	0.006±0.001
L	0.5±0.1	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
M	0.21	0.009
N	0.10	0.004
P	3° <sup>+7°</sup> <sub>-3°</sub>	3° <sup>+7°</sup> <sub>-3°</sub>

S32G5-50-7JD2

32 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P32LE-400A

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	0.040 <sup>+0.004</sup> <sub>-0.005</sub>
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 <sup>+0.004</sup> <sub>-0.005</sub>
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	0.20 <sup>+0.10</sup> <sub>-0.05</sub>	0.008 <sup>+0.004</sup> <sub>-0.002</sub>

**★ Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD4264805, 42S65805, 4265805.

**Types of Surface Mount Device**

$\mu$ PD4264805G5-7JD, 42S65805G5-7JD, 4265805G5-7JD: 32-pin plastic TSOP (II) (400 mil)

$\mu$ PD4264805LE, 42S65805LE, 4265805LE: 32-pin plastic SOJ (400 mil)

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

## [MEMO]

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.