

Current Mode PWM Controller

FEATURES

- Automatic Feed Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double Pulse Suppression
- 500mA (Peak) Totem-pole Outputs
- $\pm 1\%$ Bandgap Reference
- Under-voltage Lockout
- Soft Start Capability
- Shutdown Terminal
- 500kHz Operation

DESCRIPTION

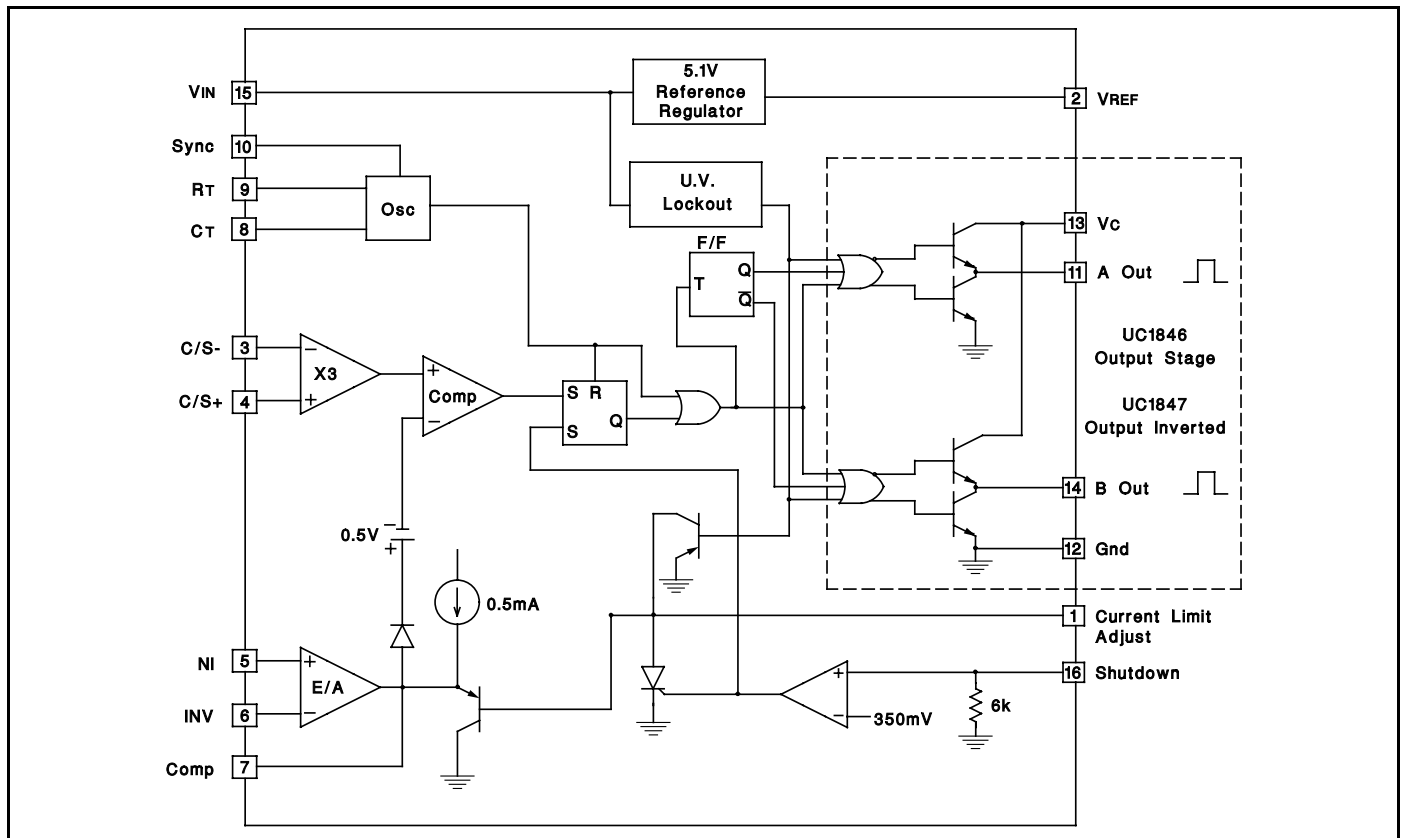
The UC1846/7 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a $\pm 1\%$ trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

BLOCK DIAGRAM

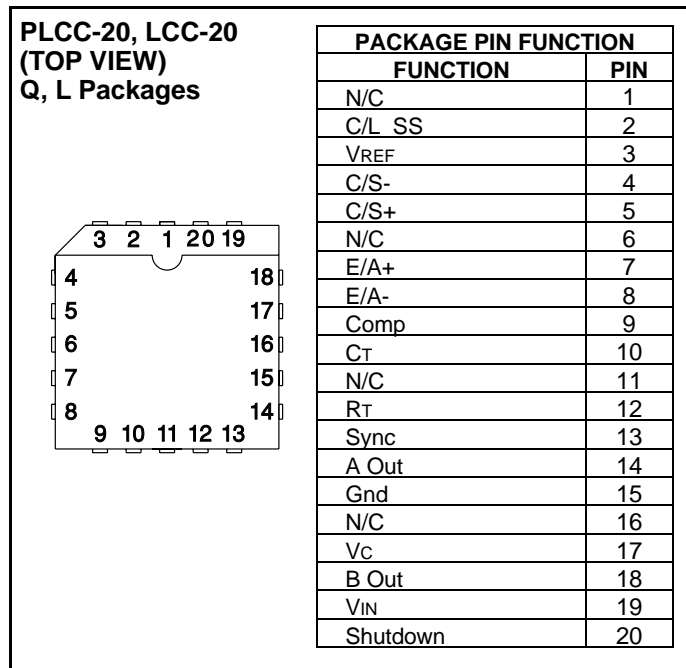
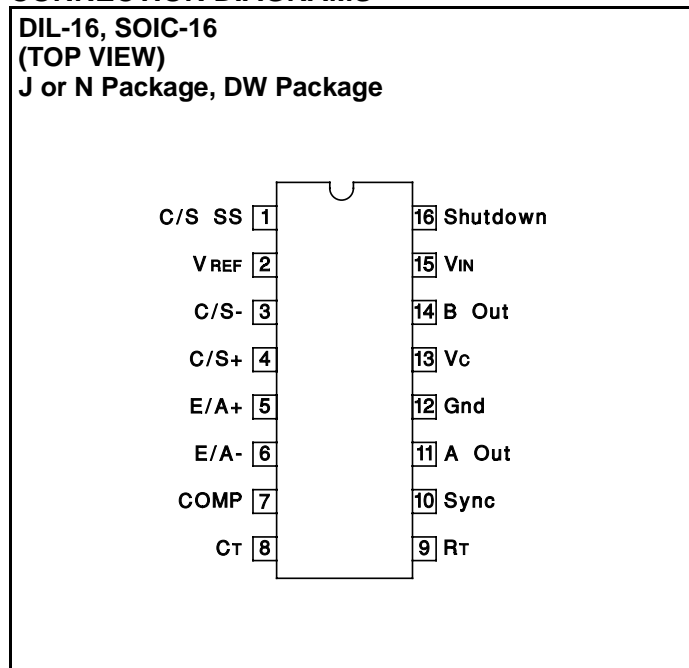


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pin 15)	+40V
Collector Supply Voltage (Pin 13)	+40V
Output Current, Source or Sink (Pins 11, 14)	500mA
Analog Inputs (Pins 3, 4, 5, 6, 16)	-0.3V to +V _{IN}
Reference Output Current (Pin 2)	-30mA
Sync Output Current (Pin 10)	-5mA
Error Amplifier Output Current (Pin 7)	-5mA
Soft Start Sink Current (Pin 1)	50mA
Oscillator Charging Current (Pin 9)	5mA
Power Dissipation at T _A =25°C	1000mW
Power Dissipation at T _C =25°C	2000mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

Note 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL and SOIC packages only.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T _J =25°C, I _o =1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V _{IN} =8V to 40V		5	20		5	20	mV
Load Regulation	I _L =1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T _J =25°C (Note 2)		100			100		μV
Long Term Stability	T _J =125°C, 1000 Hrs. (Note 2)		5			5		mV
Short Circuit Output Current	VREF=0V	-10	-45		-10	-45		mA

ELECTRICAL CHARACTERISTICS (cont.) (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for UC1846/7; -40°C to $+85^\circ\text{C}$ for the UC2846/7; and 0°C to $+70^\circ\text{C}$ for the UC3846/7; $V_{IN} = 15\text{V}$, $R_T = 10\text{k}$, $C_T = 4.7\text{nF}$, $T_A = T_J$.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Oscillator Section								
Initial Accuracy	$T_J = 25^\circ\text{C}$	39	43	47	39	43	47	kHz
Voltage Stability	$V_{IN} = 8\text{V}$ to 40V		-1	2		-1	2	%
Temperature Stability	Over Operating Range (Note 2)		-1			-1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8=0V	3.9			3.9			V
Sync Input Low Level	Pin 8=0V			2.5			2.5	V
Sync Input Current	Sync Voltage=3.9V, Pin 8=0V		1.3	1.5		1.3	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	μA
Input Offset Current			40	250		40	250	nA
Common Mode Range	$V_{IN} = 8\text{V}$ to 40V	0		$V_{IN} - 2\text{V}$	0		$V_{IN} - 2\text{V}$	V
Open Loop Voltage Gain	$\Delta V_O = 1.2$ to 3V , $V_{CM} = 2\text{V}$	80	105		80	105		dB
Unity Gain Bandwidth	$T_J = 25^\circ\text{C}$ (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	$V_{CM} = 0\text{V}$ to 38V , $V_{IN} = 40\text{V}$	75	100		75	100		dB
PSRR	$V_{IN} = 8\text{V}$ to 40V	80	105		80	105		dB
Output Sink Current	$V_{ID} = -15\text{mV}$ to -5V , $V_{PIN 7} = 1.2\text{V}$	2	6		2	6		mA
Output Source Current	$V_{ID} = 15\text{mV}$ to 5V , $V_{PIN 7} = 2.5\text{V}$	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	$R_L = (\text{Pin } 7) 15\text{k}\Omega$	4.3	4.6		4.3	4.6		V
Low Level Output Voltage			0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{PIN 3} = 0\text{V}$, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ($V_{PIN 4} - V_{PIN 3}$)	Pin 1 Open (Note 3) $R_L (\text{Pin } 7) = 15\text{k}\Omega$	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{PIN 1} = 0.5\text{V}$, Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	$V_{CM} = 1\text{V}$ to 12V	60	83		60	83		dB
PSRR	$V_{IN} = 8\text{V}$ to 40V	60	84		60	84		dB
Input Bias Current	$V_{PIN 1} = 0.5\text{V}$, Pin 7 Open (Note 3)		-2.5	-10		-2.5	-10	μA
Input Offset Current	$V_{PIN 1} = 0.5\text{V}$, Pin 7 Open (Note 3)		0.08	1		0.08	1	μA
Input Common Mode Range		0		$V_{IN} - 3$	0		$V_{IN} - 3$	V
Delay to Outputs	$T_J = 25^\circ\text{C}$, (Note 2)		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{PIN 3} = 0\text{V}$, $V_{PIN 4} = 0\text{V}$, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN 5} = V_{REF}$, $V_{PIN 6} = 0\text{V}$		-10	-30		-10	-30	μA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{PIN 1}$)	(Note 6)	3.0	1.5		3.0	1.5		mA

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for UC1846/7; -40°C to $+85^\circ\text{C}$ for the UC2846/7; and 0°C to $+70^\circ\text{C}$ for the UC3846/7; $V_{IN} = 15\text{V}$, $R_T = 10\text{k}$, $C_T = 4.7\text{nF}$, $T_A = T_J$.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Shutdown Terminal Section (cont.)								
Maximum Non-Latching Current (I _{PIN 1})	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	$T_J = 25^\circ\text{C}$ (Note 2)		300	600		300	600	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	$V_C = 40\text{V}$ (Note 5)			200			200	μA
Output Low Level	I _{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I _{SINK} = 100mA		0.4	2.1		0.4	2.1	V
Output High Level	I _{SOURCE} = 20mA	13	13.5		13	13.5		V
	I _{SOURCE} = 100mA	12	13.5		12	13.5		V
Rise Time	$C_L = 1\text{nF}$, $T_J = 25^\circ\text{C}$ (Note 2)		50	300		50	300	ns
Fall Time	$C_L = 1\text{nF}$, $T_J = 25^\circ\text{C}$ (Note 2)		50	300		50	300	ns
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
Total Standby Current								
Supply Current			17	21		17	21	mA

Note 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 3. Parameter measured at trip point of latch with $V_{PIN 5} = V_{REF}$, $V_{PIN 6} = 0\text{V}$.

Note 4. Amplifier gain defined as: $G = \frac{\Delta V_{PIN 7}}{\Delta V_{PIN 4}}$; $\Delta V_{PIN 4} = 0$ to 1.0V .

Note 5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.

Note 6. Current into Pin 1 guaranteed to latch circuit in shutdown state.

Note 7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

APPLICATIONS DATA

Oscillator Circuit

Output deadtime is determined by the external capacitor, C_T , according to the formula: $\tau_d (\mu\text{s}) = 145C_T (\mu\text{f}) \left(\frac{I_D}{I_D - \frac{3.6}{R_T (k\Omega)}} \right)$.

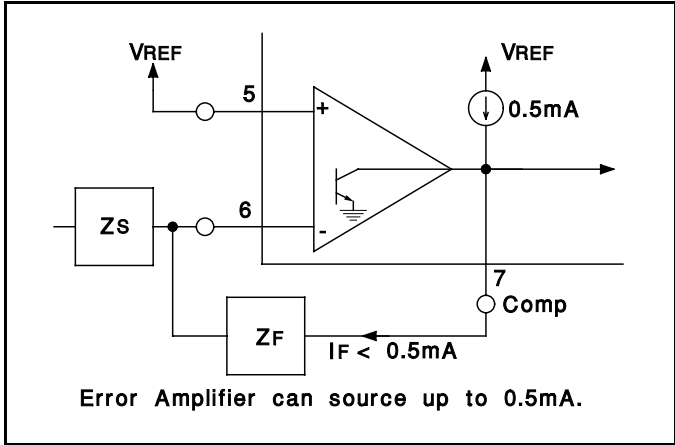
I_D = Oscillator discharge current at 25°C is typically 7.5.

For large values of R_T : $\tau_d (\mu\text{s}) \approx 145C_T (\mu\text{f})$.

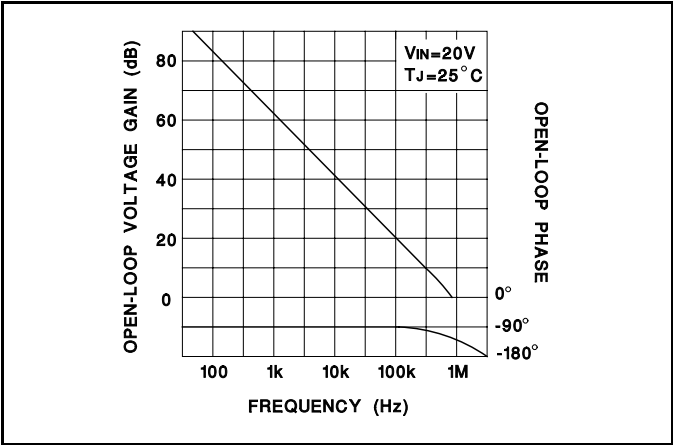
Oscillator frequency is approximated by the formula: $f_T (\text{kHz}) \approx \frac{2.2}{R_T (k\Omega) \bullet C_T (\mu\text{f})}$.

APPLICATIONS DATA (cont.)

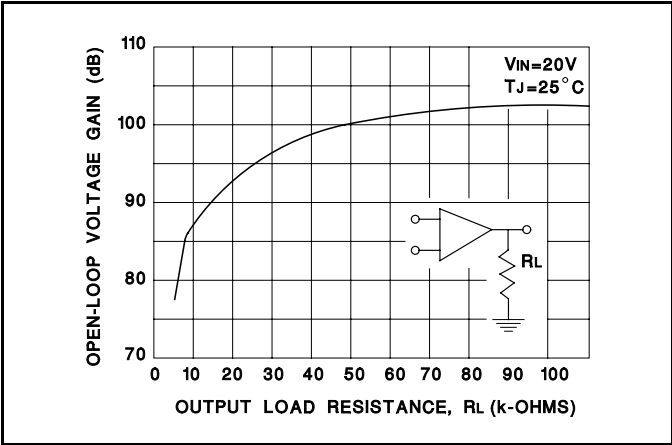
Error Amp Output Configuration



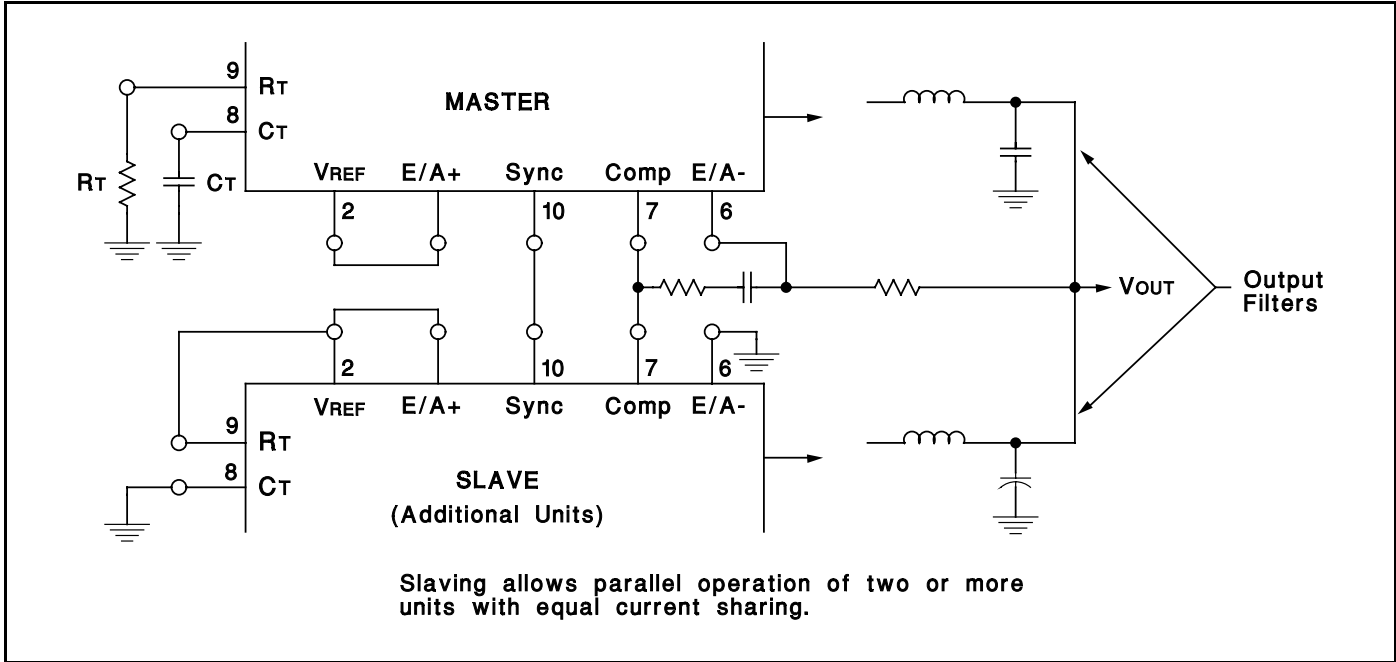
Error Amp Gain and Phase vs Frequency



Error Amp Open-Logic D.C. Gain vs Load Resistance

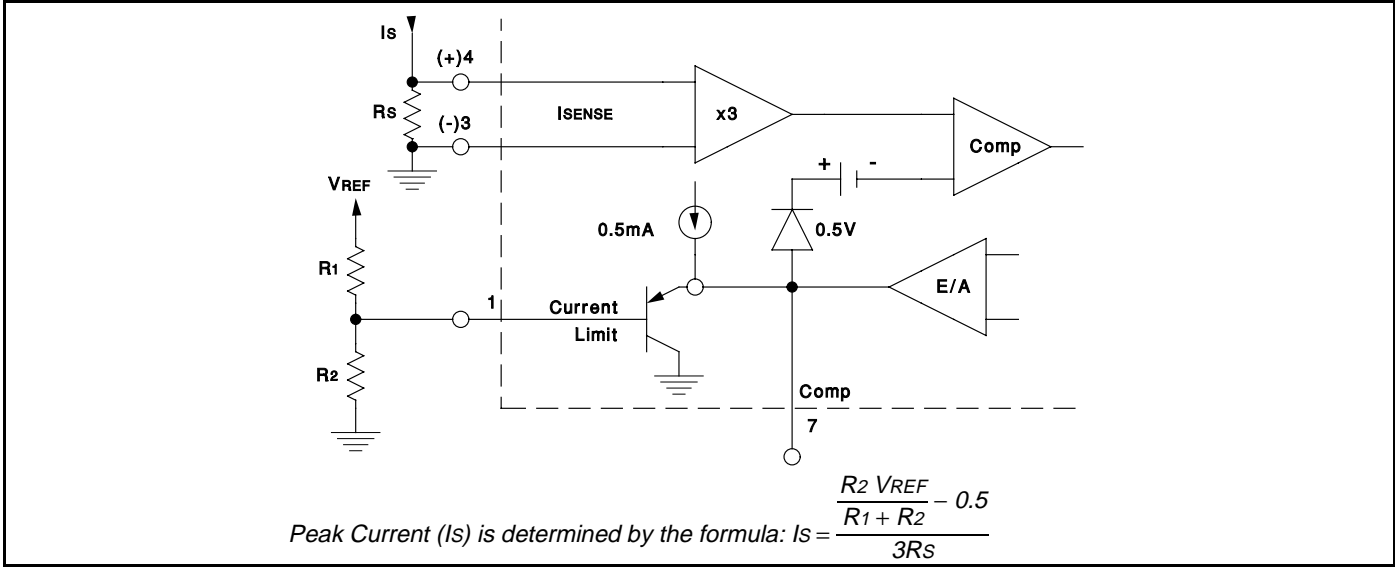


Parallel Operation

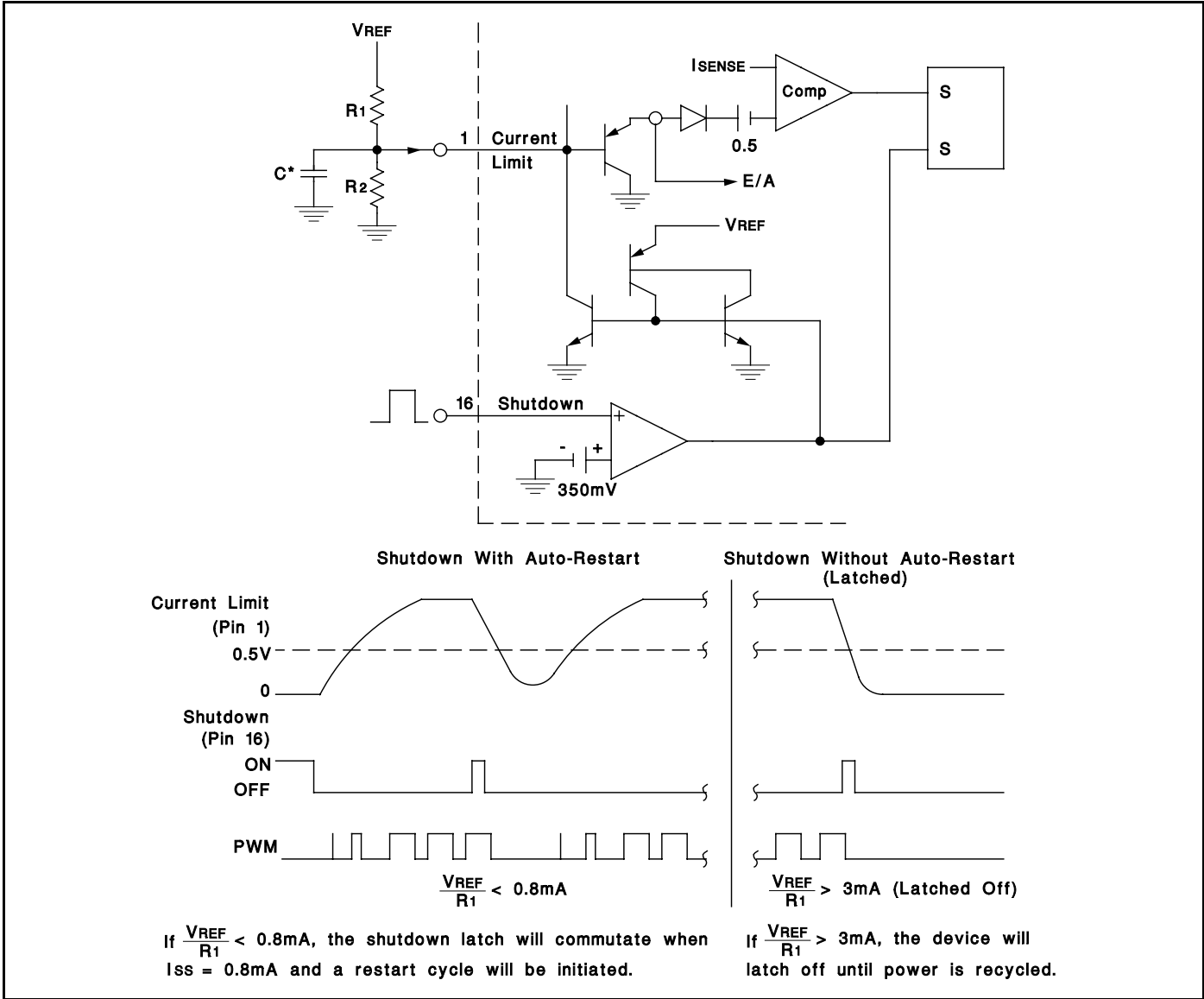


APPLICATIONS DATA (cont.)

Pulse by Pulse Current Limiting

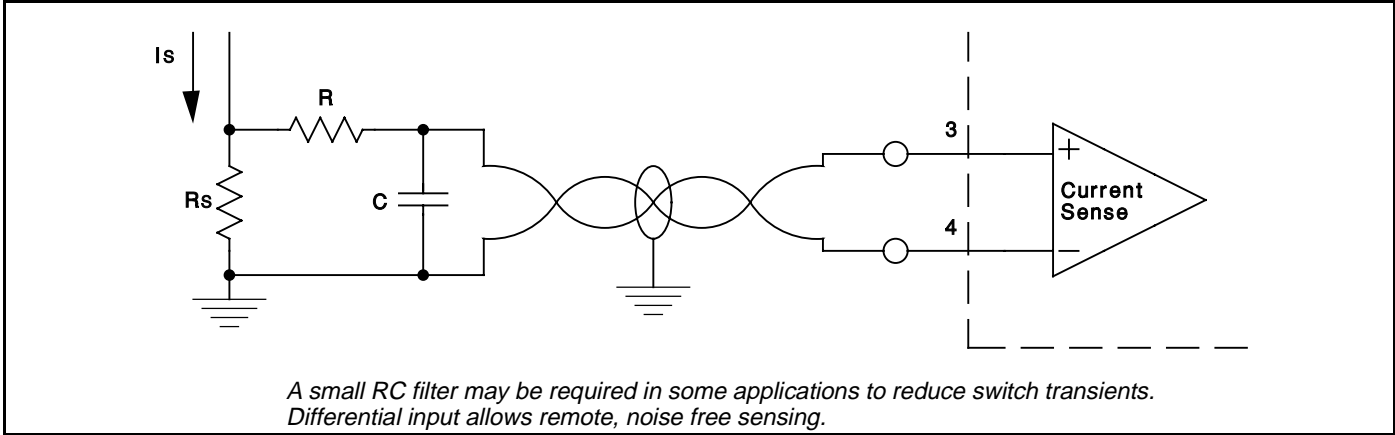


Soft Start and Shutdown /Restart Functions

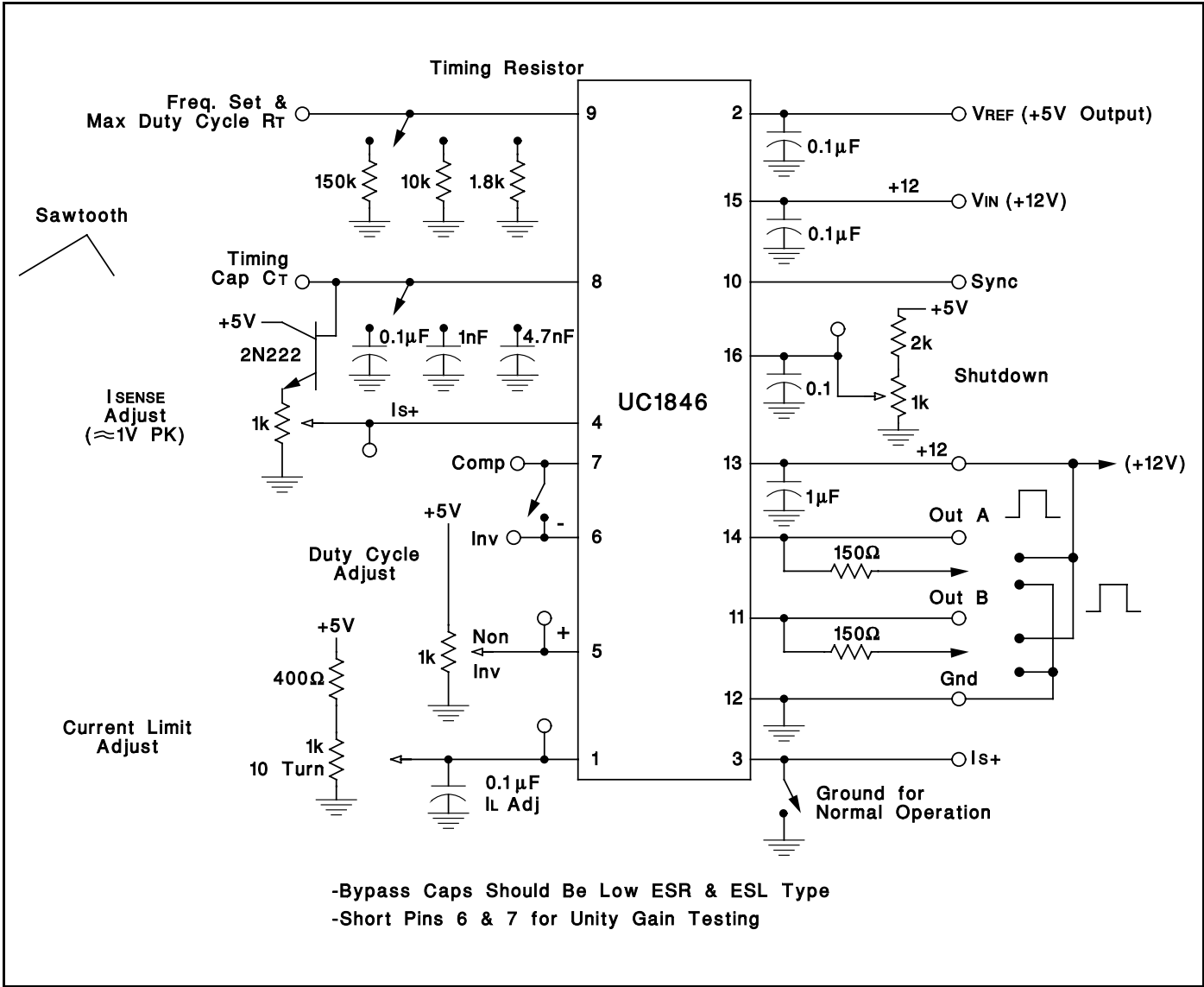


APPLICATIONS DATA (cont.)

Current Sense Amp Connection



UC1846 Open Loop Test Circuit



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