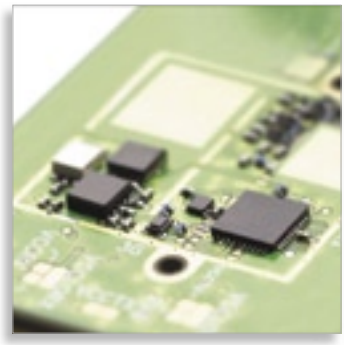

Single-chip UMTS radio

Philips UMTS transceiver SiP UAA3582 for WCDMA-FDD and dual-mode GSM/GPRS/EDGE/ UMTS mobile handsets

Designed for UMTS Band I applications, the UAA3582 offers complete receiver and transmitter functionality in a single package. It also offers HSDPA capability and low power consumption. When combined with a 3G power amplifier and a few passive components, it creates a high-performance solution with a very small footprint.

Key features

- Single-chip solution for UMTS Band I applications
  - Complete Rx/Tx functionality
  - Fully integrated channel filters for Band I
  - Fully integrated fractional-N PLL with AFC control capability
  - Fully integrated VCO with supply voltage regulator
  - Fully integrated Rx/Tx baluns, loop filters, decoupling capacitors
- 3GPP release 5, power class 3 and 4
- HSDPA capability
- Low noise, wide dynamic range for Zero-IF Rx and Tx
- Precise range for gain control
  - Rx: 95 dB in steps of 1 dB
  - Tx: 80 dB with 0.12-dB minimum resolution
- Rx voltage gain: 99 dB
- Tx output power: +5 dBm average
- Supply voltage: 2.5 to 3 V
- Three-wire serial bus interface
- Lead-free HVQFN40 package

Applications

- WCDMA-FDD handsets
- Dual-mode GSM/GPRS/EDGE/UMTS handsets

The UAA3582, an advanced transceiver for UMTS operation, is specially designed for the FDD mode of WCDMA that operates in Band I (Tx 1920-1980 MHz, Rx 2110-2170 MHz). It includes HSDPA capability, consumes very little power, and is available in a lead-free HVQFN40 package.

The transceiver uses a direct-conversion architecture and is implemented in a proven BiCMOS technology. For receiver operation, it includes an RF front-end (including the LNA), a channel filter, and a programmable gain amplifier (PGA). For transmitter operation, it has a voltage-baseband interface, an upmixer, and a two-stage RF PGA. The receiver and transmitter functions are supported by an on-chip RF VCO with a supply voltage regulator and an on-chip fractional-N PLL.

Additional functions, including transmit biasing, loop filters, decoupling capacitors, and matching circuitry for the LNA and SAW filter, are included in the package via a passive-integration die.

The transceiver supports a supply voltage range from 2.5 to 3.0 V and is fully controllable via a three-wire serial interface that resets on a V_{DD} voltage rise.

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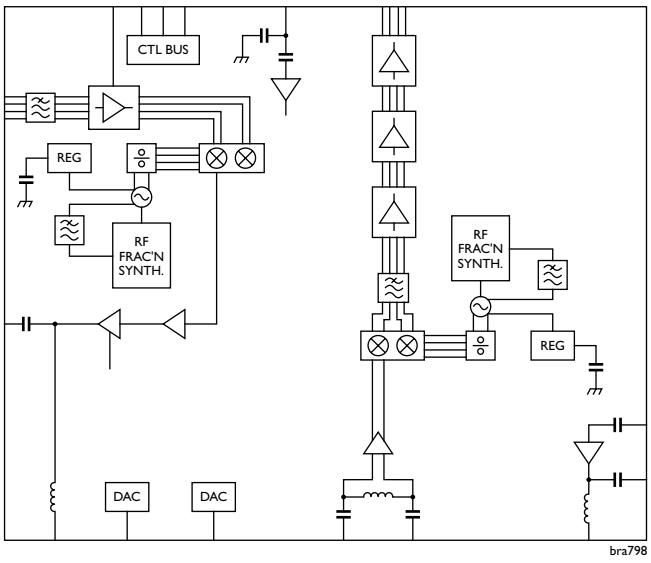
RF front-end

The RF front-end converts the aerial RF signal from W-CDMA Band I to a Zero-IF frequency. The first stage of conversion uses a single-ended LNA with a 16-dB gain step. The LNA is followed, via an external filter, by an IQ down-mixer consisting of a mixer driven in parallel by quadrature out-of-phase LO signals. The I and Q ZIF signals are then low-pass filtered to provide protection from high-frequency offset interference and fed into the channel filter. The Zero-IF I and Q outputs are applied to the low-pass channel filter with provisions for the 4x8-dB gain steps in front of the filter.

Channel filter

The on-chip channel filter is a self-calibrating filter (6 poles, 2 zeros) that has a 2.152-MHz cut-off frequency and second-order group delay compensation (2 poles, 2 zeros).

The Zero-IF I and Q signals, having passed through the channel filter, are further amplified with provisions for 39x1-dB steps and DC offset compensation. The Zero-IF output buffer provides close rail-to-rail output signals.



UAA3582 block diagram

IQ modulator

The transmitter IQ modulator supports I and Q inputs with differential voltage. It converts input signals to RF output frequency and is designed to achieve LO and image suppression.

RF voltage gain amplifier

The transmit output stage provides at least +5 dBm of maximum power control at the single-ended 50-Ω output. Gain is programmed via the three-wire bus.

Power amplifier controls

Two 10-bit ADCs, programmed via the three-wire bus, are used to control the DC/DC converter and the bias of the power amplifier.

RF VCO

The fully integrated VCO consists of 16 frequency ranges selected internally according to the frequency programming. The VCO self-calibrates for manufacturing tolerances, examining each low-to-high logical transition for the SYNON bit in the control register or each change of the integer divider ratio of the integrated RF fractional-N synthesizer.

RF fractional-N synthesizer PLL

The RF VCO is synthesized by the on-chip RF fractional-N synthesizer PLL. The frequency is set via the three-wire serial programming bus. The PLL is based on Sigma-Delta (ΣΔ) fractional-N synthesis that enables the required channel frequency, including Automatic Frequency Control (AFC) from a free-running external 26-MHz reference frequency, to be obtained. The PLL achieves very close-in-phase noise, allowing wider PLL loop bandwidth and shorter settling time.

The programmable main dividers, which are controlled by a second-order ΣΔ modulus controller, divide the RF VCO signals down to frequencies of 26 MHz (with 12-Hz step programmability). Their phase is then compared in a digital Phase/Frequency Detector (PFD) to the 26-MHz reference clock signal. The phase error information is fed back to the RF VCO via the charge pump circuit that "sources into" or "sinks" current from the loop filter capacitor, thus changing the VCO frequency such that the loop is locked in phase.

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