μPD7227
CMOS, Intelligent, Dot-Matrix LCD Controller/Driver

Description

The μPD7227 intelligent dot-matrix LCD controller/driver is a peripheral device designed to interface most microprocessors with a wide variety of dot matrix LCDs. It can directly drive any multiplexed LCD organized as 8 rows by 40 columns, and is easily cascaded up to 16 rows and 280 columns. The μPD7227 is equipped with several hardware logic blocks, such as an 8-bit serial interface, ASCII character generator, 40 x 16 static RAM with full read/write capability, and an LCD timing controller; all of which reduce microprocessor system software requirements. The μPD7227 is manufactured with a single 5 V CMOS process, and is available in a space-saving 64-pin plastic flat package.

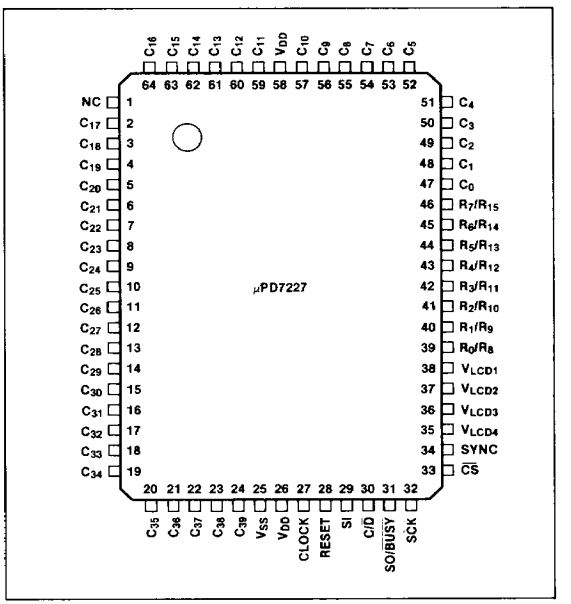
Features

- ☐ Single-chip LCD controller with direct LCD drive
- ☐ Compatible with most microprocessors
- ☐ Eight row drives
  - — Designed for dot-matrix LCD configurations up to 280 dots
  - — Designed for 5 x 7 dot-matrix character LCD configuration up to 8 characters
  - — Cascadable to 16 row drives
- ☐ 40 column drives
  - — Cascadable to 280 column drives
- ☐ Hardware logic blocks reduce system software requirements
  - — 8-bit serial interface for communication
  - — ASCII 5 x 7 dot-matrix character generator with 64-character vocabulary
  - — 40 x 16-bit static RAM for data storage, retrieval, and complete back-up memory capability.
  - — Voltage controller generates LCD bias voltages
  - — Timing controller synchronizes column drives with sequentially-multiplexed row drives
- ☐ Single +5 V power supply
- ☐ CMOS technology

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7227G-12	64-pin plastic QFP	1000 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	NC	No connection
2-24, 47-57, 59-64	C_0-C_{39}	LCD column driver outputs
25	V_{SS}	Ground
26, 58	V_{DD}	Power
27	CLOCK	System clock input
28	RESET	Reset input
29	SI	Serial input
30	C/$\overline{D}$	Command or data select input
31	SO/$\overline{BUSY}$	Serial output or busy output
32	$\overline{SCK}$	Serial clock input
33	CS	Chip select input
34	SYNC	Synchronization port
35-38	V_{LCD1}-V_{LCD4}	LCD bias voltage supply inputs
39-46	R_0/R_8-R_7/R_{15}	LCD row driver outputs

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Pin Functions

C_0-C_{39}

LCD column driver outputs.

R0/8-R7/15

LCD row driver outputs.

V_{LCD1}-V_{LCD4}

LCD bias voltage supply inputs to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across VDD.

SI

Serial input from the microprocessor.

SO/$\overline{BUSY}$

Serial output from the μPD7227 to the microprocessor when in read mode and C/$\overline{D}$ is low. When $\overline{BUSY}$ (active low), handshake output indicates the μPD7227 is ready to receive/send the next data byte.

$\overline{SCK}$

Serial clock input. Synchronizes 8-bit serial data transfer between the microprocessor and μPD7227.

C/$\overline{D}$

Command/data select input. Distinguishes serially input data byte as a command or as display data.

$\overline{CS}$

Chip select input. Enables the μPD7227 for communication with the microprocessor.

SYNC

Synchronization port. For multichip operation, tie all SYNC lines together and configure with the MODE SET command.

CLOCK

System clock input. Connect to external clock source.

RESET

Reset input. RC circuit or pulse initializes the μPD7227 after power-up.

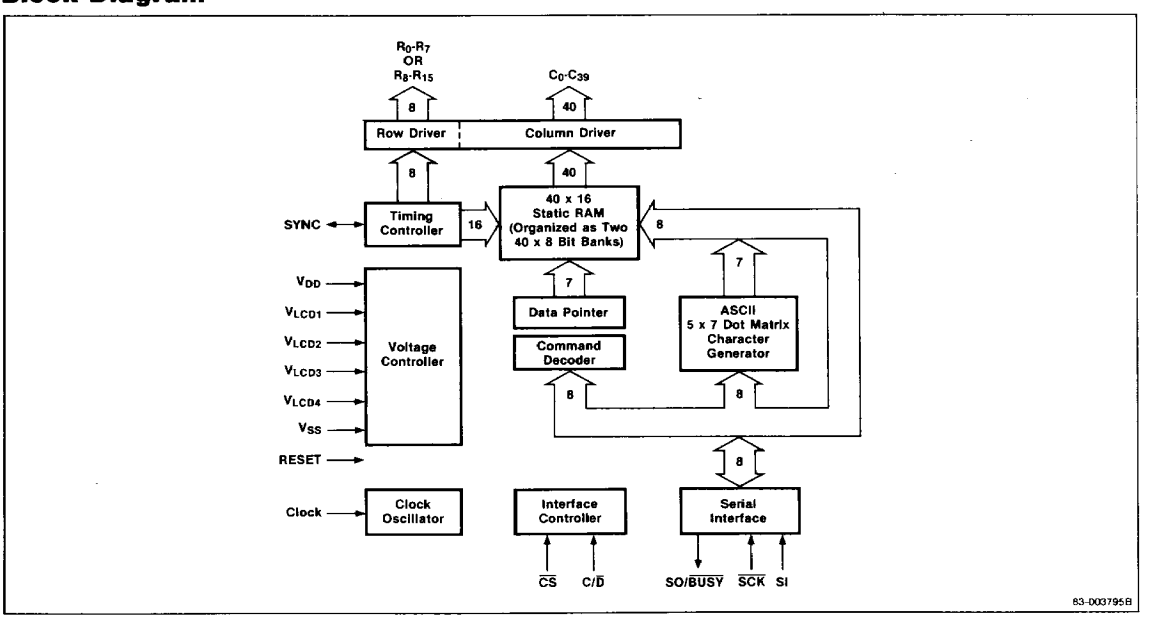
V_{DD}

Power supply positive. Apply single voltage 5 V ± 10% for proper operation.

V_{SS}

Ground.

Block Diagram



Absolute Maximum Ratings

T_A = 25°C

Power supply, V_{DD}	−0.3 V to +7.0 V
All inputs and outputs with respect to V_{CC}	−0.3 V to V_{DD} +0.3 V
Storage temperature, T_{STG}	−65°C to +150°C
Operating temperature, T_{OPT}	−10°C to +70°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input capacitance	C_I		10	pF	fϕ = 1 MHz
Output capacitance	C_O		25	pF	Unmeasured pins returned to ground.
Input/output capacitance	C_{IO}		15	pF SYNC	

DC Characteristics

T_A = −10°C to +70°C, V_{DD} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Input voltage, low	V_{IL}	0		0.3 V_{DD}	V	
Input leakage current, high	I_{LIH}			+10	μA	V_{IH} = V_{DD}
Input leakage current, low	I_{LIL}			−10	μA	V_{IH} = 0V
Output voltage, high	V_{OH1}	V_{DD}-0.5			V	SO/BUSY, I_{OH} = −400 μA
	V_{OH2}	V_{DD}-0.5			V	SYNC, I_{OH} = −100 μA
Output voltage, low	V_{OL1}			0.45	V	SO/BUSY, I_{OL} = +1.7 mA
				0.45	V	SYNC, I_{OL} = +100 μA
Output leakage current, high	I_{LOH}			+10	μA	V_{OH} = V_{DD}
Output leakage current, low	I_{LOL}			−10	μA	V_{OL} = 0V
LCD operating voltage	V_{LCD}	3.0		V_{DD}	V	8-row multiplexed LCD drive configuration
			V_{DD}		V	16-row multiplexed LCD drive configuration
Row drive output impedance	R_{ROW}		4	8	kΩ	
Column drive output impedance	R_{COLUMN}		10	15	kΩ	
Supply current	I_{DD}		200	400	μA	f0 = 400 KHz

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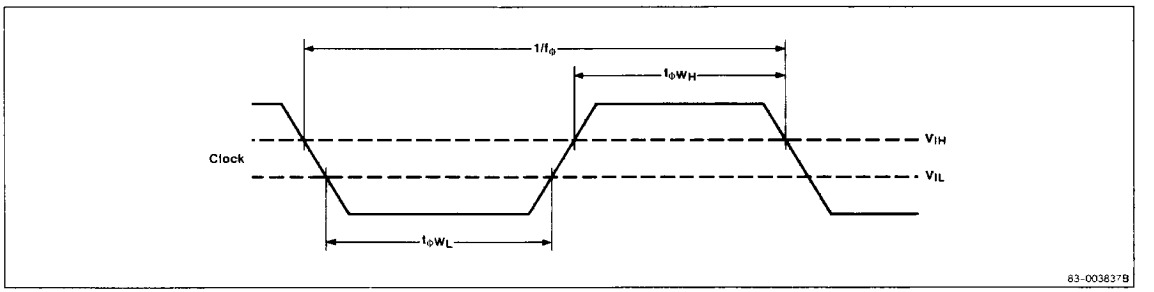
AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5.0V \pm 10\%$

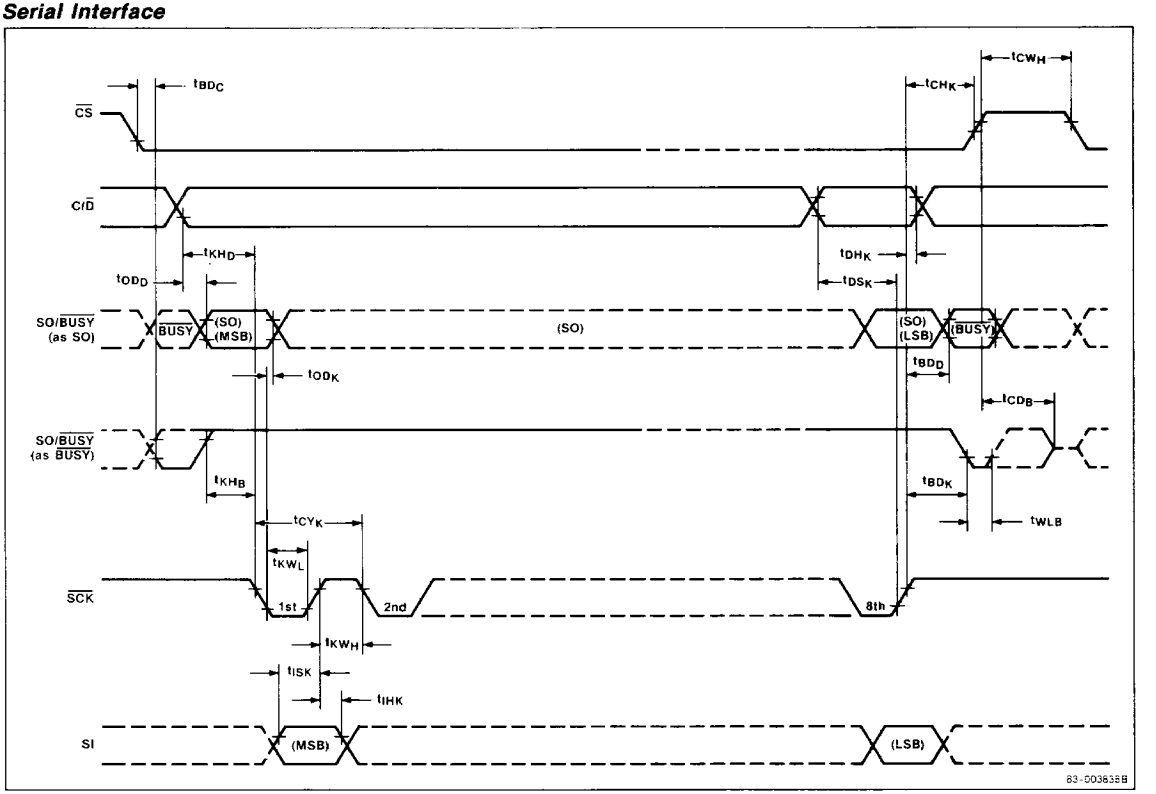
Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Clock frequency	$f\phi$	100	1000	KHz	
Clock pulse width high	$t_{\phi WH}$	400		ns	
Clock pulse width low	$t_{\phi WL}$	400		ns	
$\overline{SCK}$ cycle	t_{CYK}	0.9		μs	
$\overline{SCK}$ pulse width high	t_{KWH}	400		ns	
$\overline{SCK}$ pulse width low	t_{KWL}	400		ns	
$\overline{SCK}$ hold time after $\overline{BUSY}$↑	t_{KHB}	0		ns	
SI setup time to $\overline{SCK}$↑	t_{ISK}	100		ns	
SI hold time after $\overline{SCK}$↑	t_{IHK}	250		ns	
SO delay time after $\overline{SCK}$↓	t_{ODK}		320	ns	C_{LOAD} = 50 pF
SO delay time after C/$\overline{D}$↓	t_{ODD}		2	μs	
$\overline{SCK}$ hold time after C/$\overline{D}$↓	t_{KHD}	2		μs	
$\overline{BUSY}$ delay time after 8th $\overline{SCK}$↑	t_{BDK}		3	μs	C_{LOAD} = 50 pF
$\overline{BUSY}$ delay time after C/$\overline{D}$↑	t_{BDD}		2	μs	
$\overline{BUSY}$ delay time after $\overline{CS}$↓	t_{BDC}		2	μs	
C/$\overline{D}$ setup time to 8th $\overline{SCK}$↑	t_{DSK}	2		μs	
C/$\overline{D}$ hold time after 8th $\overline{SCK}$↑	t_{DHK}	2		μs	
$\overline{CS}$ hold time after 8th $\overline{SCK}$↑	t_{CHK}	2		μs	
$\overline{CS}$ pulse width high	t_{CWH}	2/fϕ		μs	
$\overline{CS}$↑ delay time to $\overline{BUSY}$ floating	t_{CDB}	2		μs	C_{LOAD} = 50 pF
SYNC load capacitance	C_{LOADS}		100	pF	
$\overline{BUSY}$ low level width	t_{WLB}	18	64	1/fϕ	C_{LOAD} = 50 pF

Timing Waveforms

Clock Waveform



Serial Interface



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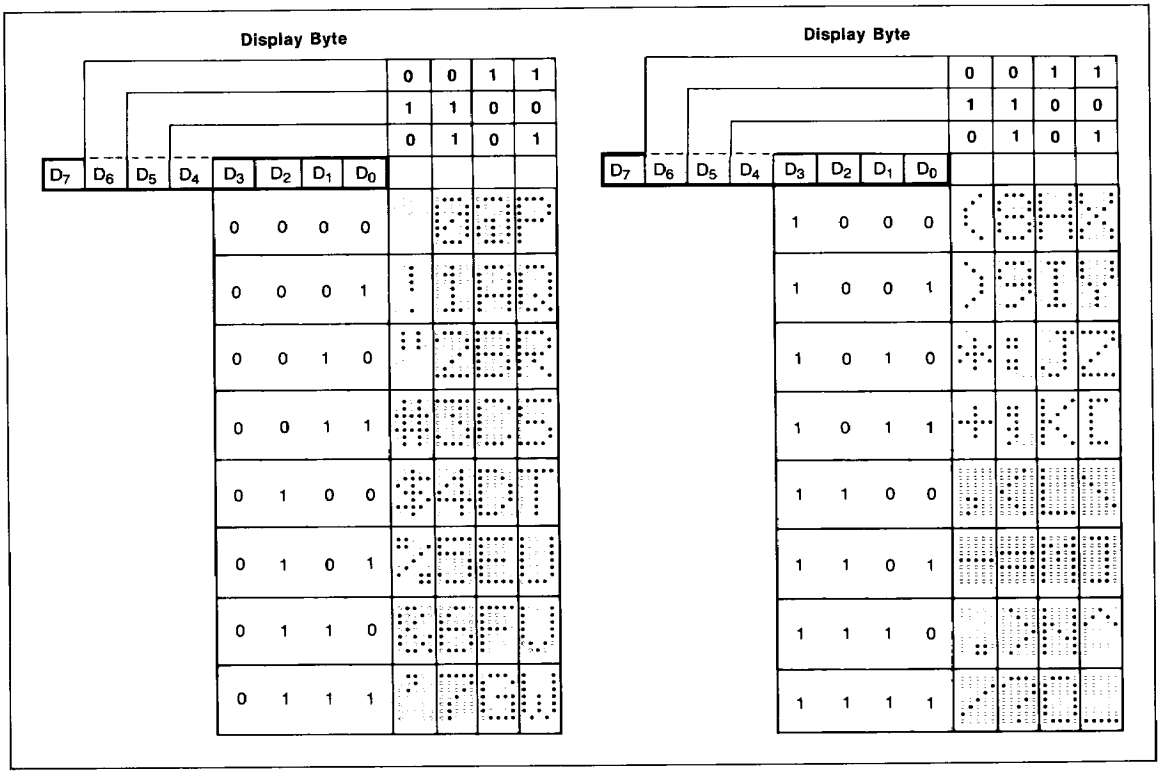
Command Summary

Command	Description	Instruction Code Binary D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
Mode Set	Initialize the μPD7227, including selection of 1. LCD drive configuration 2. Row driver port function 3. RAM bank 4. SYNC port function	0	0	0	1	1	D_2	D_1	D_0	18-1F
Frame Frequency Set	Set LCD frame frequency	0	0	0	1	0	D_2	D_1	D_0	10-14
Load Data Pointer	Load data pointer with 7 bits of immediate data	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0	80-E7
Write Mode	Write display byte in serial register to RAM location addressed by data pointer; modify data pointer	0	1	1	0	0	1	D_1	D_0	64-67
Read Mode	Load RAM contents addressed by data pointer into serial register for output; modify data pointer	0	1	1	0	0	0	D_1	D_0	60-63
AND Mode	Perform a logical AND between the display byte in the serial register and the RAM contents addressed by data pointer; write result to same RAM location; modify data pointer	0	1	1	0	1	1	D_1	D_0	6C-6F
OR Mode	Perform a logical OR between the display byte in the serial register and the RAM contents addressed by data pointer; write result to same RAM location; modify data pointer	0	1	1	0	1	0	D_1	D_0	68-6B
Character Mode	Decode display byte in serial register into 5 x 7 character with character generator; write character to RAM location addressed by data pointer; increment data pointer by 5	0	1	1	1	0	0	1	0	72
Set Bit	Set single bit of RAM location addressed by data pointer; modify data pointer	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
Reset Bit	Reset single bit of RAM location addressed by data pointer; modify data pointer	0	0	1	D_4	D_3	D_2	D_1	D_0	20-3F
Enable Display	Turn on the LCD	0	0	0	0	1	0	0	1	09
Disable Display	Turn off the ICD	0	0	0	0	1	0	0	0	08

Further details of operation can be found in the μPD7227 intelligent dot-matrix LCD controller/driver technical manual.

5 × 7 Character Set as Generated in μPD7227



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