p-channel JFETs designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

Performance Curves PS
See Section 5

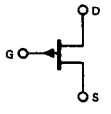
BENEFITS

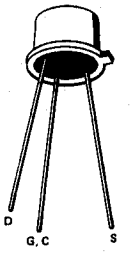
- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (U304)
- High Off-Isolation
  $I_{D(off)} < 500$ pA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . 30 V
Gate Current . . . . . 50 mA
Total Device Dissipation, Free-Air
(Derate 2.8 mW/°C) . . . . . 350 mW
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

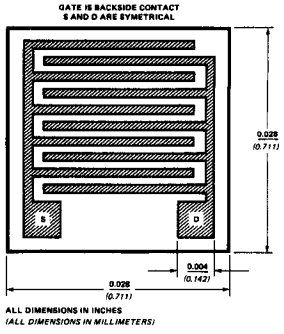
		Characteristic		U304 Min	U304 Max	U305 Min	U305 Max	U306 Min	U306 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		500		500		500	pA	$V_{GS} = 20$ V, $V_{DS} = 0$	
2					1.0		1.0		1.0	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4		$V_{DS} = -15$ V, $I_D = -1\ \mu A$	
5		$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6		$V_{GS} = 0$, $I_D = -15$ mA (U304), $I_D = -7$ mA (U305), $I_D = -3$ mA (U306)	
6		I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	$V_{DS} = -15$ V, $V_{GS} = 0$	
7		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	$V_{DS} = -15$ V, $V_{GS} = 12$ V (U304), $V_{GS} = 7$ V (U305), $V_{GS} = 5$ V (U306)	
8					-1.0		-1.0		-1.0	µA		150°C
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		85		110		175	Ω	$V_{GS} = 0$ V, $I_D = -1$ mA	
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		85		110		175	Ω	$V_{GS} = 0$ V, $I_D = 0$	f = 1 kHz
11		C_{iss}	Common-Source Input Capacitance		27		27		27	pF	$V_{DS} = -15$ V, $V_{GS} = 0$	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		$V_{DS} = 0$, $V_{GS} = 12$ V (U304) $V_{GS} = 7$ V (U305), $V_{GS} = 5$ V (U306)	
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		20		25		25	ns		
14		t_r	Rise Time		15		25		35			
15		$t_{d(off)}$	Turn-OFF Delay Time		10		15		20			
16		t_f	Fall Time		25		40		60			

	U304	U305	U306
V_{DD}	-10 V	-6 V	-6 V
$V_{GS(off)}$	12 V	7 V	5 V
R_L	580 Ω	743 Ω	1800 Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	-15 mA	-7 mA	-3 mA

PS

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300 µs, duty cycle ≤ 3%.

© 1979 Siliconix incorporated



p-channel JFET
designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

Siliconix

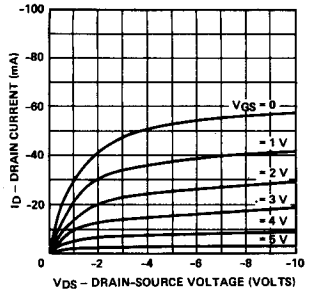
BENEFITS:

- Low Insertion Loss in Switching Systems $R_{ON} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(off)} < 500$ pA

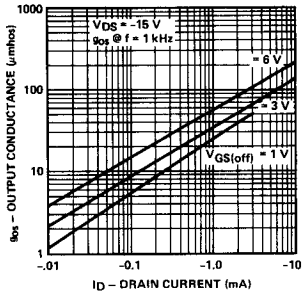
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N5018-19, 2N5114-16, U304-6
Single	TO-92	J174-7, J270-1, P1086-87, P1086E
Single	TO-92 Lead-form	J174-18 - 177-18, J270-18 - 271-18 P1086-18 - 87-18
Single	Chip	2N5018CHP-19CHP, 2N5114CHP-16CHP U304CHP-6CHP, P1086CHP-87CHP J270CHP-271CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

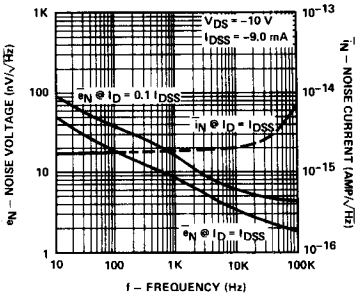
Output Characteristic



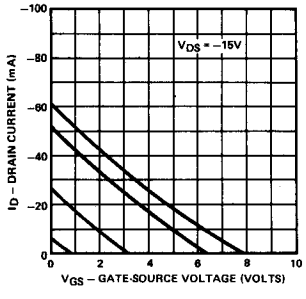
Common-Source Output Conductance vs Drain Current



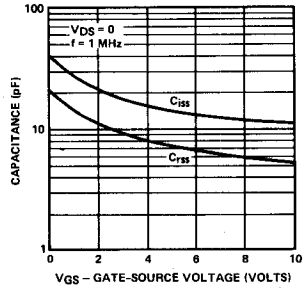
Equivalent Input Noise Voltage and Noise Current vs Frequency



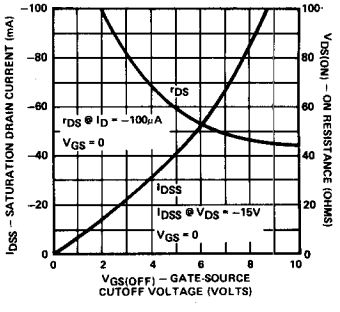
Transfer Characteristics



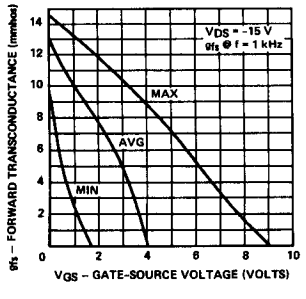
Common-Source Capacitance vs Gate-Source Voltage



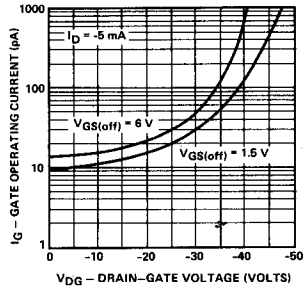
Saturation Drain Current and Drain-Source ON Resistance vs. Gate-Source Cutoff Voltage



Transconductance Characteristics



Gate Operating Current vs Drain-Gate Voltage



© 1979 Siliconix Incorporated