μPD8080AF 8-BIT N-CHANNEL MICROPROCESSOR FAMILY

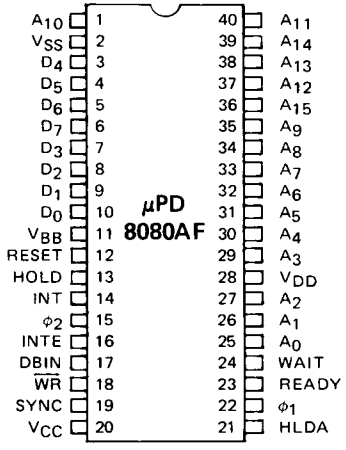
DESCRIPTION

The μPD8080AF is a complete 8-bit parallel processor for use in general purpose digital computer systems. It is fabricated on a single LSI chip using N-channel silicon gate MOS process, which offers much higher performance than conventional microprocessors (1.28 μs minimum instruction cycle). A complete microcomputer system is formed when the μPD8080AF is interfaced with I/O ports (up to 256 input and 256 output ports) and any type or speed of semiconductor memory. It is available in a 40 pin ceramic or plastic package.

FEATURES

- 78 Powerful Instructions
- Three Devices – Three Clock Frequencies
  μPD8080AF – 2.0 MHz
  μPD8080AF-2 – 2.5 MHz
  μPD8080AF-1 – 3.0 MHz
- Direct Access to 64K Bytes of Memory with 16-Bit Program Counter
- 256 8-Bit Input Ports and 256 8-Bit Output Ports
- Double Length Operations Including Addition
- Automatic Stack Memory Operation with 16-Bit Stack Pointer
- TTL Compatible (Except Clocks)
- Multi-byte Interrupt Capability
- **Fully** Compatible with Industry Standard 8080A
- Available in either Plastic or Ceramic Package

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The μPD8080AF contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8080AF also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8080AF utilizes a 16-bit address bus to directly address 64K bytes of memory, is TTL compatible (1.9 mA), and utilizes the following addressing modes: Direct; Register; Register Indirect; and Immediate.

The μPD8080AF has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8080AF also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

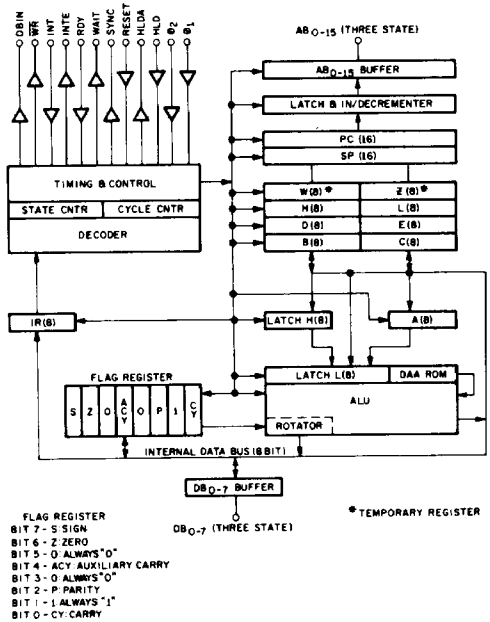
This processor is designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data buses are employed to allow direct interface to memories and I/O ports. Control signals, requiring no decoding, are provided directly by the processor. All buses, including the control bus, are TTL compatible.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address and data lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data buses.

The μPD8080AF has the capability to accept a multiple byte instruction upon an interrupt. This means that a CALL instruction can be inserted so that any address in the memory can be the starting location for an interrupt program. This allows the assignment of a separate location for each interrupt operation, and as a result no polling is required to determine which operation is to be performed.

NEC offers three versions of the μPD8080AF. These processors have all the features of the μPD8080AF except the clock frequency ranges from 2.0 MHz to 3.0 MHz. These units meet the performance requirements of a variety of systems while maintaining software and hardware compatibility with other 8080A devices.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 25-27, 29-40	$A_{15} - A_0$	Address Bus (output three-state)	The address bus is used to address memory (up to 64K 8-bit words) or specify the I/O device number (up to 256 input and 256 output devices). A_0 is the least significant bit.
2	V_{SS}	Ground (input)	Ground
3-10	$D_7 - D_0$	Data Bus (input/output three-state)	The bidirectional data bus communicates between the processor, memory, and I/O devices for instructions and data transfers. During each sync time, the data bus contains a status word that describes the current machine cycle. D_0 is the least significant bit.
11	V_{BB}	V_{BB} Supply Voltage (input)	-5V ± 5%
12	RESET	Reset (input)	If the RESET signal is activated, the program counter is cleared. After RESET, the program starts at location 0 in memory. The INTE and HLDA flip-flops are also reset. The flags, accumulator, stack pointer, and registers are not cleared. (Note: External synchronization is not required for the RESET input signal which must be active for a minimum of 3 clock periods.)
13	HOLD	Hold (input)	HOLD requests the processor to enter the HOLD state. The HOLD state allows an external device to gain control of the μPD8080AF address and data buses as soon as the μPD8080AF has completed its use of these buses for the current machine cycle. It is recognized under the following conditions: • The processor is in the HALT state. • The processor is in the T_2 or T_W stage and the READY signal is active. As a result of entering the HOLD state, the ADDRESS BUS ($A_{15} - A_0$) and DATA BUS ($D_7 - D_0$) are in their high impedance state. The processor indicates its state on the HOLD ACKNOWLEDGE (HLDA) pin.
14	INT	Interrupt Request (input)	The μPD8080AF recognizes an interrupt request on this line at the end of the current instruction or while halted. If the μPD8080AF is in the HOLD state, or if the Interrupt Enable flip-flop is reset, it will not honor the request.
15	ϕ_2	Phase Two (input)	Phase two of processor clock.
16	INTE (1)	Interrupt Enable (output)	INTE indicates the content of the internal interrupt enable flip-flop. This flip-flop is set by the Enable (EI) or reset by the Disable (DI) interrupt instructions and inhibits interrupts from being accepted by the processor when it is reset. INTE is automatically reset (disabling further interrupts) during T_1 of the instruction fetch cycle (M_1) when an interrupt is accepted and is also reset by the RESET signal.
17	DBIN	Data Bus In (output)	DBIN indicates that the data bus is in the input mode. This signal is used to enable the gating of data onto the μPD8080AF data bus from memory or input ports.
18	$\overline{WR}$	Write (output)	$\overline{WR}$ is used for memory WRITE or I/O output control. The data on the data bus is valid while the $\overline{WR}$ signal is active ($\overline{WR} = 0$).
19	SYNC	Synchronizing Signal (output)	The SYNC signal indicates the beginning of each machine cycle.
20	V_{CC}	V_{CC} Supply Voltage (input)	+5V ± 5%
21	HLDA	Hold Acknowledge (output)	HLDA is in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
All Output Voltages ① . . . . . -0.3 to +20 Volts
All Input Voltages ① . . . . . -0.3 to +20 Volts
Supply Voltages V_{CC}, V_{DD} and V_{SS} ① . . . . . -0.3 to +20 Volts
Power Dissipation 1.5W
Note: ① Relative to V_{BB}.

$T_a = 25°C$

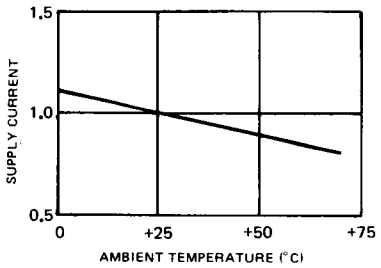
*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage	V_{ILC}	V_{SS} - 1		V_{SS} + 0.8	V	
Clock Input High Voltage	V_{IHC}	9.0		V_{DD} + 1	V	
Input Low Voltage	V_{IL}	V_{SS} - 1		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	3.3		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.9 mA on all outputs
Output High Voltage	V_{OH}	3.7			V	I_{OH} = -150 μA ②
Avg. Power Supply Current (V_{DD})	$I_{DD(AV)}$		40	70	mA	t_{CY} min
Avg. Power Supply Current (V_{CC})	$I_{CC(AV)}$		60	80	mA	t_{CY} min
Avg. Power Supply Current (V_{BB})	$I_{BB(AV)}$		0.01	1	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ②	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Clock Leakage	I_{CL}			±10 ②	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
Data Bus Leakage in Input Mode	I_{DL} ①			-100 ②	μA	$V_{SS} \leq V_{IN} \leq V_{SS} + 0.8V$
				-2 ②	mA	$V_{SS} + 0.8V \leq V_{IN} \leq V_{CC}$
Address and Data Bus Leakage During HOLD	I_{FL}			+10 ②	μA	$V_{ADDR/DATA} = V_{CC}$
				-100 ②		$V_{ADDR/DATA} = V_{SS} + 0.45V$

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED ③



Notes: ① When DBIN is high and $V_{IN} > V_{IH}$ internal active pull-up resistors will be switched onto the data bus.
② Minus (-) designates current flow out of the device.
③ ΔI supply/ΔT_a = -0.45%/°C.

CAPACITANCE

$T_a = 25°C$, $V_{CC} = V_{DD} = V_{SS} = 0V$, $V_{BB} = -5V$.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ		17	25	pF	f_c = 1 MHz
Input Capacitance	C_{IN}		6	10	pF	Unmeasured Pins
Output Capacitance	C_{OUT}		10	20	pF	Returned to V_{SS}

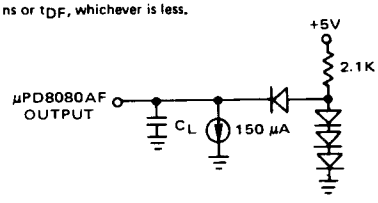
AC CHARACTERISTICS
μPD8080AF

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

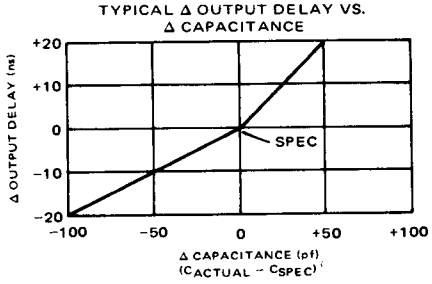
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.48		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi 1}$	60			nsec	
φ2 Pulse Width	$t_{\phi 2}$	220			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	80			nsec	
Address Output Delay From φ2	t_{DA} ②			200	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			220	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	30			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	150			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	120			nsec	
HOLD Setup Time to φ2	t_{HS}	140			nsec	
INT Setup Time During φ2 (During φ1 in Halt Mode)	t_{IS}	120			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes: ① Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.

② Load Circuit.



③ Actual $t_{CY} = t_{D3} + t_{r\phi 2} + t_{\phi 2} + t_{f\phi 2} + t_{D2} + t_{r\phi 1} > t_{CY}$ Min.



AC CHARACTERISTICS
μPD8080AF-1

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.32		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		25	nsec	
φ1 Pulse Width	$t_{\phi1}$	50			nsec	
φ2 Pulse Width	$t_{\phi2}$	145			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	60			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	60			nsec	
Address Output Delay From φ2	t_{DA} ②			150	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			180	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			110	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		130	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	10			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	120			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued:

④ The following are relevant when interfacing the μPD8080AF to devices having V_{IH} = 3.3V.

a. Maximum output rise time from 0.8V to 3.3V = 100 ns at C_L = SPEC.

b. Output delay when measured to 3.0V = SPEC +60 ns at C_L = SPEC.

c. If $C_L \neq$ SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.

AC CHARACTERISTICS
μPD8080AF-2

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0,38		2,0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	175			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	70			nsec	
Address Output Delay From φ2	t_{DA} ②			175	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			200	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	20			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	130			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued: ⑤

Device	t_{AW}
μPD8080AF	$2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$
μPD8080AF-2	$2\,t_{CY} - t_{D3} - t_{r\phi2} - 130$
μPD8080AF-1	$2\,t_{CY} - t_{D3} - t_{r\phi2} - 110$

⑥

Device	t_{DW}
μPD8080AF	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-2	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-1	$t_{CY} - t_{D3} - t_{r\phi2} - 150$

⑦ If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.

⑧ $t_{HF} = t_{D3} + t_{r\phi2} - 50$ ns.

⑨ $t_{WF} = t_{D3} + t_{r\phi2} - 10$ ns.

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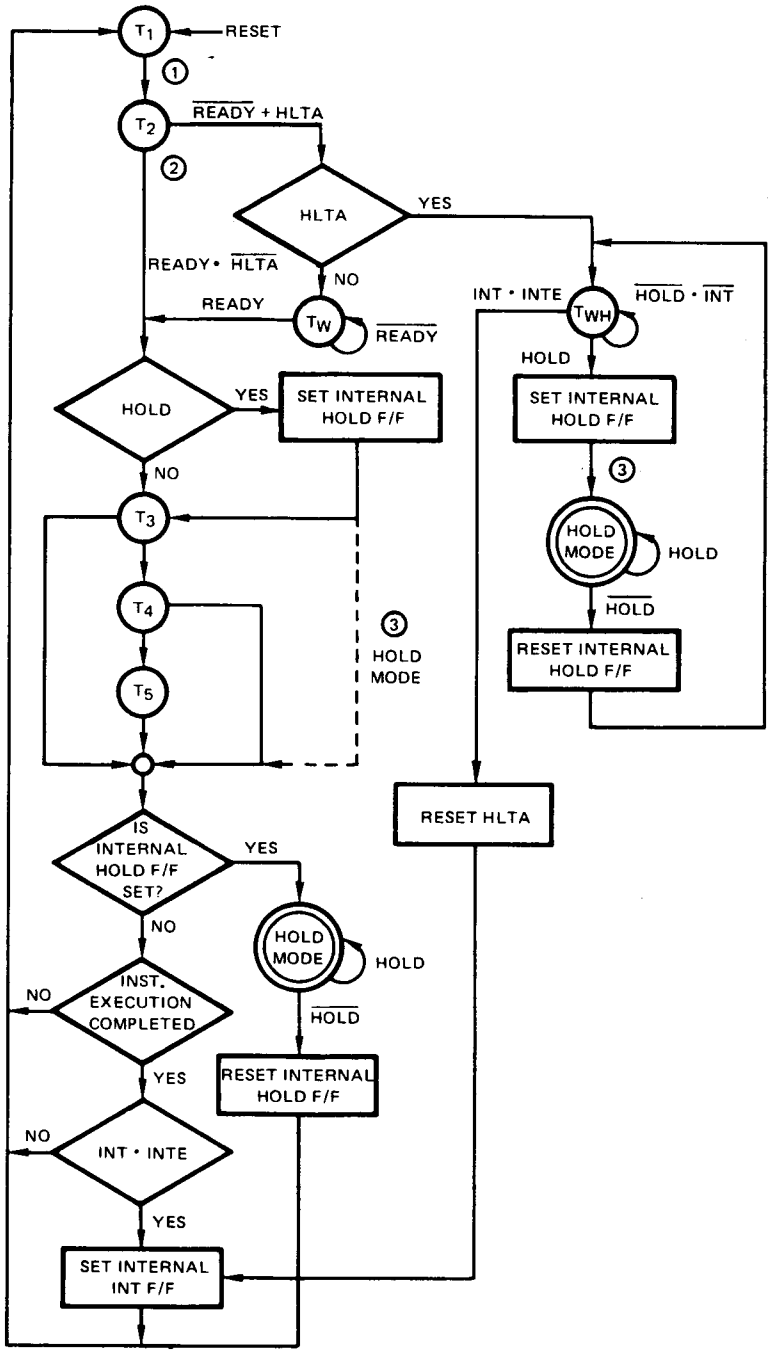
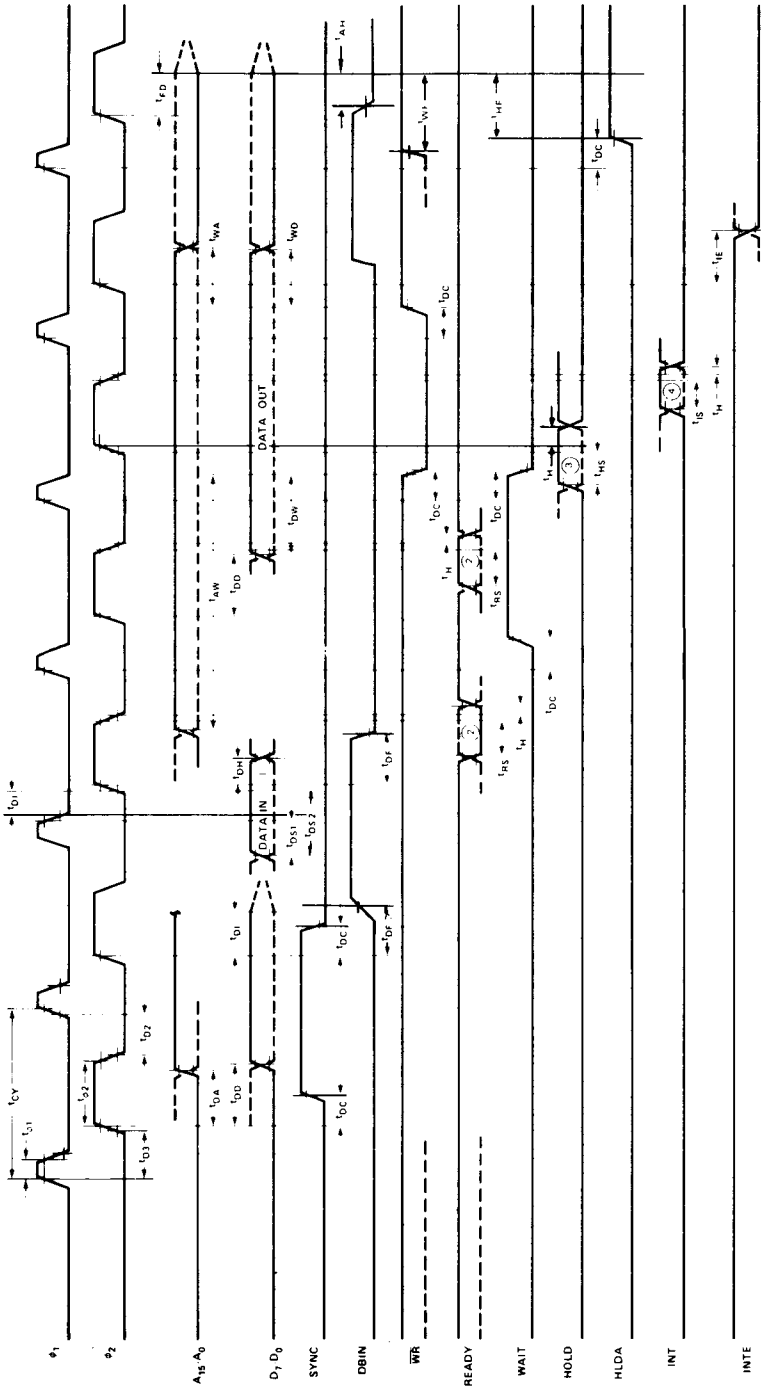
PROCESSOR STATE TRANSITION DIAGRAM



Notes:
1. INTE F/F is reset if internal INT F/F is set.
2. Internal INT F/F is reset if INTE F/F is reset.
3. If required, T_4 and T_5 are completed simultaneously with entering hold state.

TIMING WAVEFORMS (5)

(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



Notes:
① Data in must be stable for this period during DBIN + T_3. Both t_{DS1} and t_{DS2} must be satisfied.
② Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
③ Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
④ Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized in the following instruction. (External synchronization is not required.)
⑤ This timing diagram shows timing relationships only; it does not represent any specific machine cycle.
⑥ Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V; "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.

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INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8080AF has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8080AF. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8080AF instruction set.

The special instruction group completes the μPD8080AF instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the μPD8080AF is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

MNEMONIC[1]	DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	5				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	5	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	5	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU - REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU - MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU - IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU - ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	17				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	11/17				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	11/17				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	11/17				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	11/17				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	11/17				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	11/17				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	11/17				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	11/17				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	5/11				
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11				
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11				
RC	Return on carry	1	1	0	1	1	0	0	0	5/11				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11				
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11				
RP	Return on positive	1	1	1	1	0	0	0	0	5/11				
RM	Return on minus	1	1	1	1	1	0	0	0	5/11				

MNEMONIC[1]	DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	11				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	11				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	11				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	11				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	5				
INX D	Increment DE	0	0	0	1	0	0	1	1	5				
INX H	Increment HL	0	0	1	0	0	0	1	1	5				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	5				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	5				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	5				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	5				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	5				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	18				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	5				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	5				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RST A	Restart	1	1	A	A	A	1	1	1	11				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				Cy
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	7				

Notes

[1] Operand Symbols used
- A = 8-bit address or expression
- s = source register
- d = destination register
- PSW = Processor Status Word
- SP = Stack Pointer
- D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
- D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
- ADDR = 16-bit Memory address expression

[2] ddd or sss = 000 B = 001 C = 010 D = 011 E = 100 H = 101 L = 110 Memory = 111 A.

[3] Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
- = flag not affected
0 = flag reset
1 = flag set

8

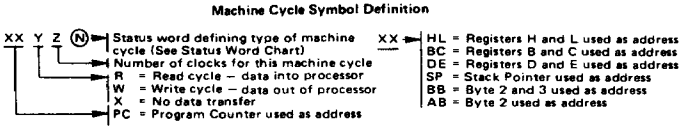
INSTRUCTION CYCLE TIMES

One to five machine cycles (M_1 -- M_5) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$). During ϕ_1 • SYNC of each machine cycle, a status word that identifies the type of machine cycle is available on the data bus.

Execution times and machine cycles used for each type of instruction are shown below.

INSTRUCTION	MACHINE CYCLES EXECUTED	CLOCK TIMES (MIN/MAX)
RST X and PUSH RP	PCR5 ① SPW3 ⑤ SPW3 ⑤	11
All CALL Instructions	PCR5 ① PCR3 ② PCR3 ② SPW3 ⑤ SPW3 ⑤	11/17
Conditional TURN Instructions	PCR5 ① SPR3 ④ SPR3 ④	5/11
RET Instruction	PCR4 ① SPR3 ④ SPR3 ④	10
XTHL	PCR4 ① SPR3 ④ SPR3 ④ SPW3 ⑤ SPW5 ⑤	18
DAD RP	PCR4 ① PCX3 Ⓧ PCX3 Ⓧ	10
INR R; INX RP, DCR R; DCX RP; PCHL; MOV R, R; SPHL	PCR5 ①	5
All JUMP Instructions and LXI RP	PCR4 ① PCR3 ② PCR3 ②	10
POP RP	PCR4 ① SPR3 ④ SPR3 ④	10
LDA	PCR4 ① PCR3 ② PCR3 ② BBR3 ②	13
STA	PCR4 ① PCR3 ② PCR3 ② BBW3 ③	13
LHLD	PCR4 ① PCR3 ② PCR3 ② BBR3 ② BBR3 ②	16
SHLD	PCR4 ① PCR3 ② PCR3 ② BBW3 ③ BBW3 ③	16
STAX B	PCR4 ① BCW3 ③	7
STAX D	PCR4 ① DEW3 ③	7
LDAX B	PCR4 ① BCR3 ②	7
LDAX D	PCR4 ① DER3 ②	7
MOV R, M; ADD M; ADC M; SUB M; SB B M; ANA M; XRA M; ORA M; CMP M	PCR4 ① HLR3 ②	7
INR M and DCR M	PCR4 ① HLR3 ② HLW3 ③	10
MVI M	PCR4 ① PCR3 ② HLW3 ③	10
MVI R; ADI; ACI; SUI; SBI; ANI; XRI; ORI; CPI	PCR4 ① PCR3 ②	7
MOV M, R	PCR4 ① HLW3 ③	7
EI; DI ADD R; ADC R; SUB R; SBB R; ANA R; XRA R; ORA R; CMP R; RLC; RRC; RAL; RAR; DAA; CMA; STC; CMC; NOP; XCHG	PCR4 ①	4
OUT	PCR4 ① PCR3 ② ABW3 ⑦	10
IN	PCR4 ① PCR3 ② ABR3 ⑥	10
HLT	PCR4 ① PCX3 ⑨	7

Machine Cycle Symbol Definition



Underlined (XXYZ(N)) indicates machine cycle is executed if condition is True.

STATUS INFORMATION DEFINITION

SYMBOLS	DATA BUS BIT	DEFINITION
INTA ①	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart or CALL instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO}$ = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP ①	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR ①	D_7	Designates that the data bus will be used for memory read data.

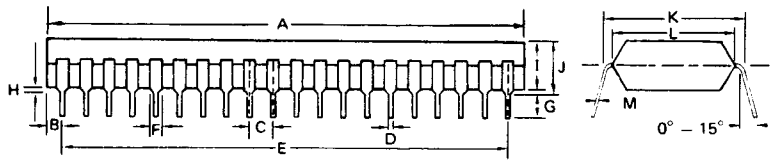
Note: ① These three status bits can be used to control the flow of data onto the μPD8080AF data bus.

STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INT. ACK. WHILE HALT
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

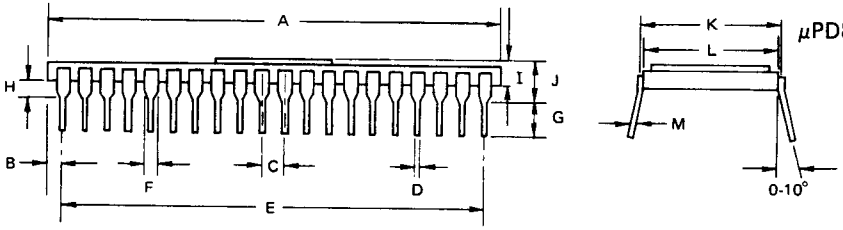
Ⓝ STATUS WORD



PACKAGE OUTLINE
μPD8080AFC

(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62 MAX	0.064 MAX
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24 TYP	0.600 TYP
L	13.2 TYP	0.520 TYP
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

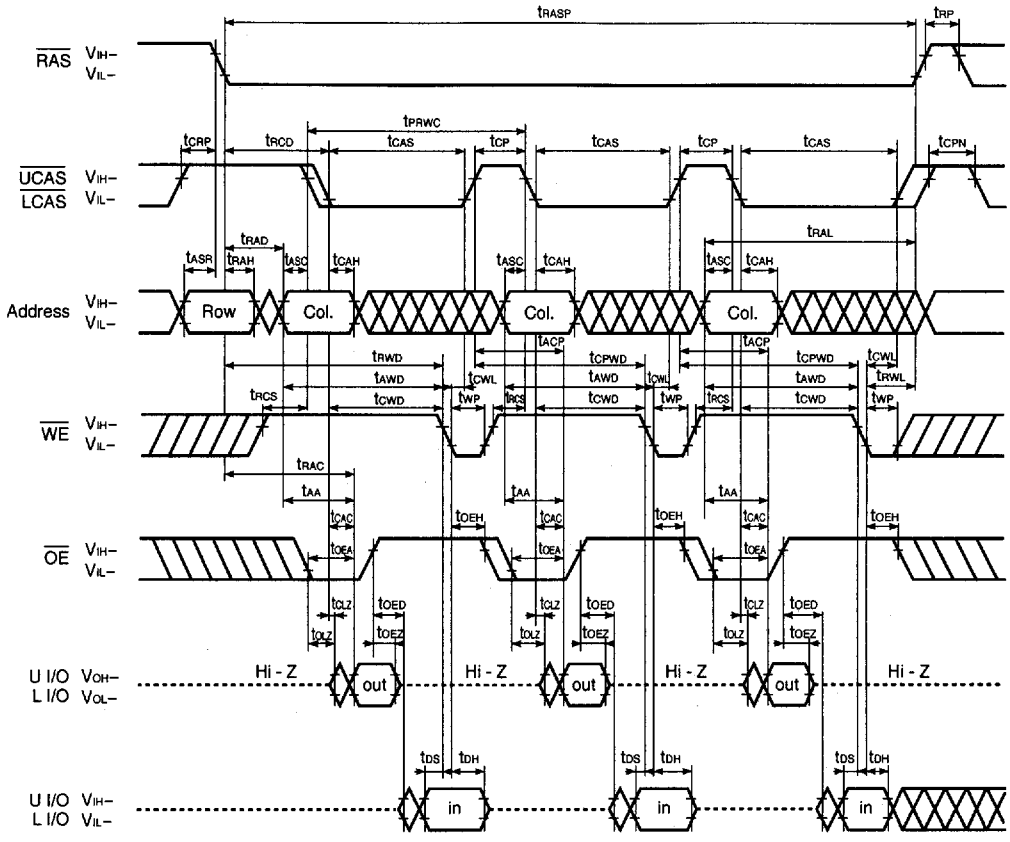


μPD8080AFD

(CERAMIC)

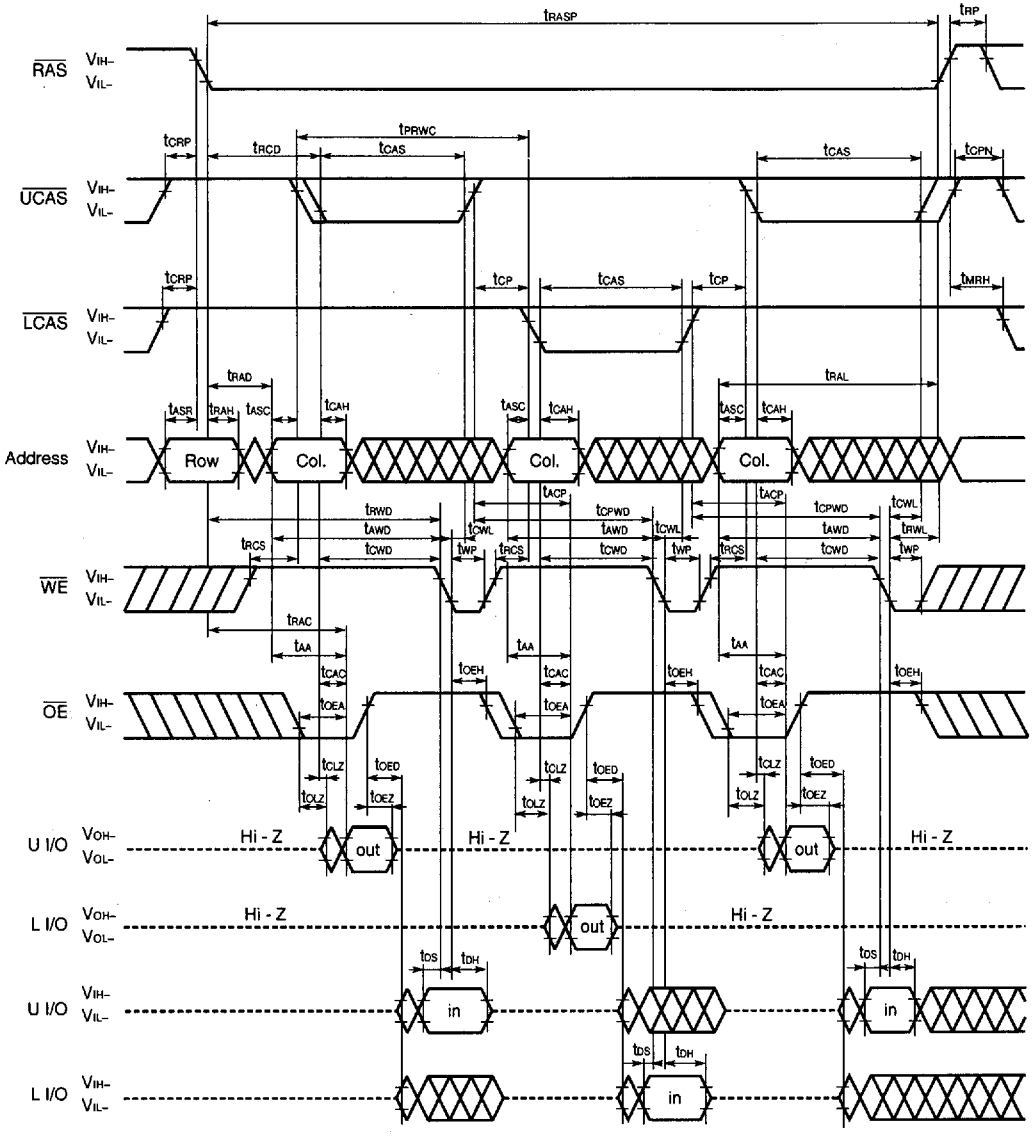
ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

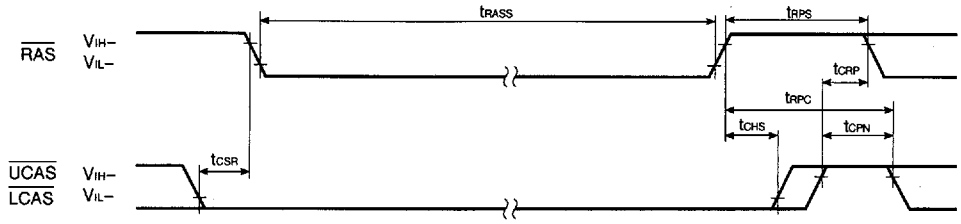
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

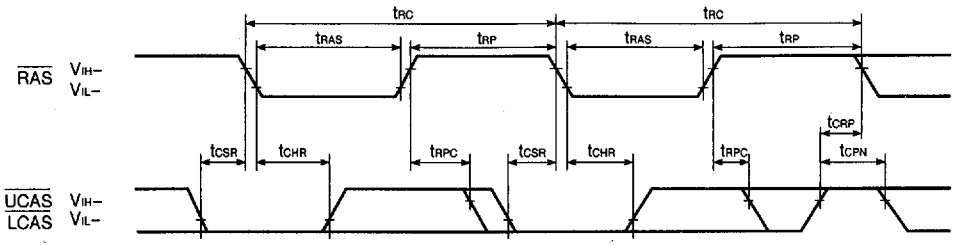
μPD42S18160: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

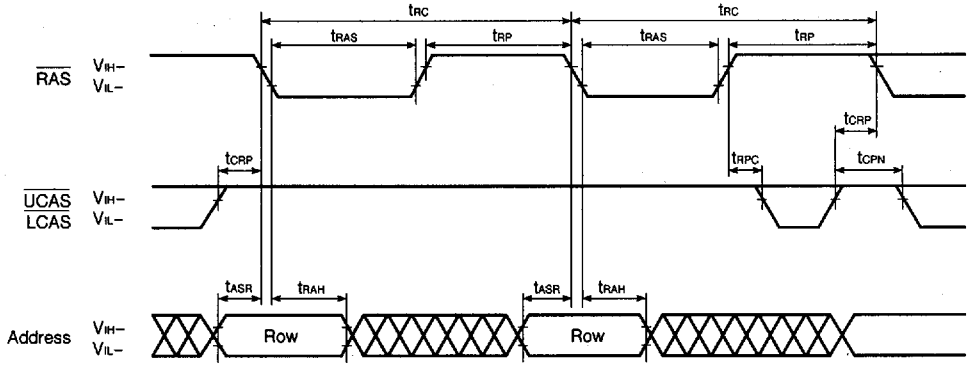
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)