

TPIC1301

3-HALF H-BRIDGE GATE-PROTECTED POWER DMOS ARRAY

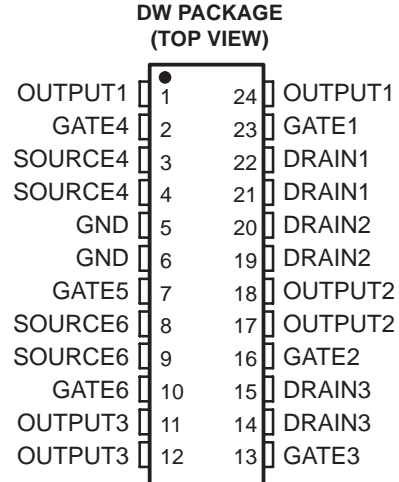
SLIS037 – NOVEMBER 1994

- Low $r_{DS(on)}$. . . 0.23 Ω Typ
- High Voltage Output . . . 60 V
- Extended ESD Capability . . . 4000 V
- Pulsed Current . . . 11.25 A Per Channel
- Fast Commutation Speed

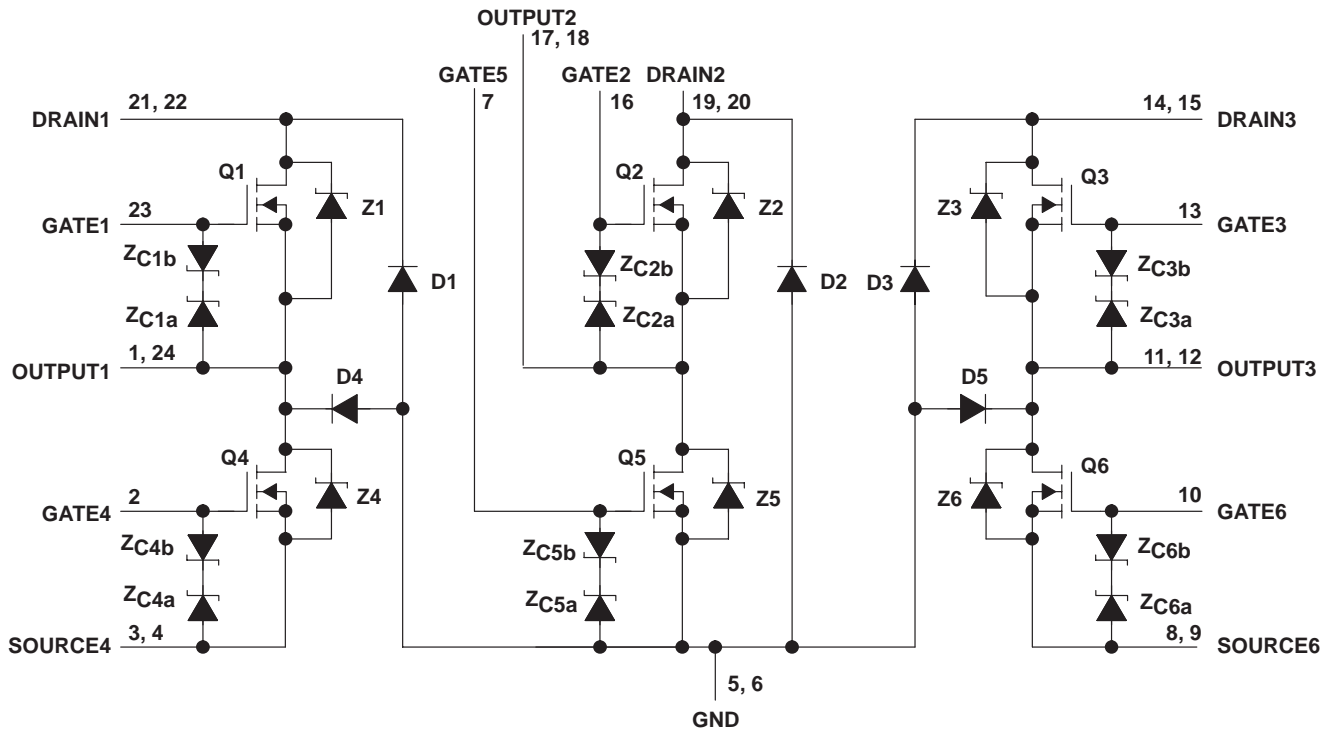
description

The TPIC1301 is a monolithic gate-protected power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as three half H-bridges. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC1301 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of -40°C to 125°C .



schematic



NOTE: For correct operation, no terminal pin may be taken below GND.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Copyright © 1994, Texas Instruments Incorporated

TPIC1301
3-HALF H-BRIDGE GATE-PROTECTED
POWER DMOS ARRAY

SLIS037 – NOVEMBER 1994

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-GND voltage, V_{DG}	100 V
Drain-to-source voltage, V_{DS}	60 V
Output-to-GND voltage	60 V
SOURCE4, SOURCE6-to-GND voltage	60 V
Gate-to-source voltage range, V_{GS}	-9 V to 18 V
Continuous drain current, each output, $T_C = 25^\circ\text{C}$	2.25 A
Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$	2.25 A
Pulsed drain current, each output, I_{max} , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15)	11.25 A
Continuous gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	± 50 mA
Pulsed gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	± 500 mA
Single-pulse avalanche energy, E_{AS} , $T_C = 25^\circ\text{C}$ (see Figures 4, 15, and 16)	17.2 mJ
Continuous total dissipation, $T_C = 25^\circ\text{C}$ (see Figure 15)	1.39 W
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating case temperature range, T_C	-40°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%



TPIC1301
3-HALF H-BRIDGE GATE-PROTECTED
POWER DMOS ARRAY

SLIS037 – NOVEMBER 1994

electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$,	$V_{GS} = 0$	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$, See Figure 5	$V_{DS} = V_{GS}$,	1.5	1.75	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	$I_{GS} = 250\ \mu\text{A}$		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	$I_{SG} = 250\ \mu\text{A}$		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1 – D5)	Drain-to-GND current = $250\ \mu\text{A}$		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 2.25\ \text{A}$, See Notes 2 and 3	$V_{GS} = 10\ \text{V}$,		0.52	0.62	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 2.25\ \text{A}$, $V_{GS} = 0$ (Z1 – Z6), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	$I_D = 2.25\ \text{A}$ (D1 – D5) See Notes 2 and 3			5		V
I_{DSS}	Drain current-gate shorted to source	$V_{DS} = 48\ \text{V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1		μA
			$T_C = 125^\circ\text{C}$	0.5	10		
I_{GSSF}	Forward-gate current, drain short circuited to source	$V_{GS} = 15\ \text{V}$,	$V_{DS} = 0$		20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	$V_{SG} = 5\ \text{V}$,	$V_{DS} = 0$		10	100	nA
I_{lkg}	Leakage current, drain-to-GND Gate shorted to source	$V_{DGND} = 48\ \text{V}$	$T_C = 25^\circ\text{C}$	0.05	1		μA
			$T_C = 125^\circ\text{C}$	0.5	10		
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10\ \text{V}$, $I_D = 2.25\ \text{A}$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$	0.23	0.275		Ω
			$T_C = 125^\circ\text{C}$	0.35	0.4		
g_{fs}	Forward transconductance	$V_{DS} = 15\ \text{V}$, See Notes 2 and 3 and Figure 9	$I_D = 1.125\ \text{A}$,	1.6	2.21		S
C_{iss}	Short-circuit input capacitance, common source	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$, See Figure 11			200	250	pF
C_{oss}	Short-circuit output capacitance, common source				175	220	
C_{rss}	Short-circuit reverse transfer capacitance, common source				40	75	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	$I_S = 1.125\ \text{A}$, $V_{GS} = 0$, See Figures 1 and 14	$V_{DS} = 48\ \text{V}$, $di/dt = 100\ \text{A}/\mu\text{s}$,		50		ns
Q_{RR}	Total diode charge		Z1, Z2, and Z3		65		nC



TPIC1301

3-HALF H-BRIDGE GATE-PROTECTED POWER DMOS ARRAY

SLIS037 – NOVEMBER 1994

resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$, $R_L = 20\ \Omega$, $t_{dis} = 10\text{ ns}$, See Figure 2 $t_{en} = 10\text{ ns}$,		25	50	ns
$t_{d(off)}$ Turn-off delay time			25	50	
t_r Rise time			15	30	
t_f Fall time			7	15	
Q_g Total gate charge	$V_{DS} = 48\text{ V}$, See Figure 3 $I_D = 1.125\text{ A}$, $V_{GS} = 10\text{ V}$,		6.2	7.4	nC
$Q_{gs(th)}$ Threshold gate-to-source charge			0.7	0.8	
Q_{gd} Gate-to-drain charge			2.4	2.9	
L_D Internal drain inductance			5		nH
L_S Internal source inductance			5		
R_g Internal gate resistance			0.25		Ω

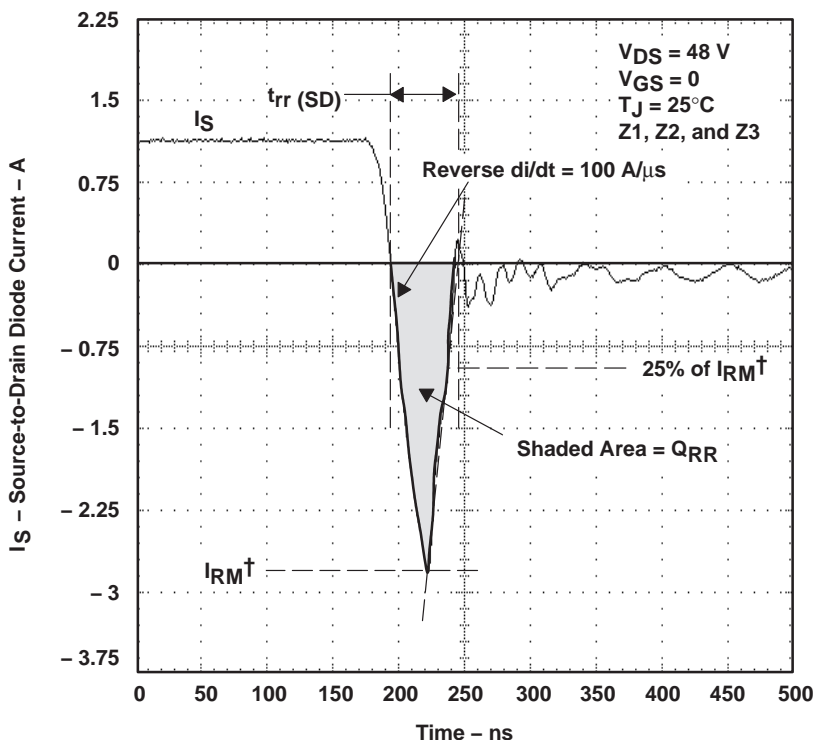
thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	See Notes 4 and 7		90		$^\circ\text{C}/\text{W}$
$R_{\theta JB}$ Junction-to-board thermal resistance	See Notes 5 and 7		45		$^\circ\text{C}/\text{W}$
$R_{\theta JP}$ Junction-to-pin thermal resistance	See Notes 6 and 7		28		$^\circ\text{C}/\text{W}$

- NOTES:
- Package mounted on an FR4 printed-circuit board with no heatsink.
 - Package mounted on a 24 in², 4-layer FR4 printed-circuit board.
 - Package mounted in intimate contact with infinite heatsink.
 - All outputs with equal power

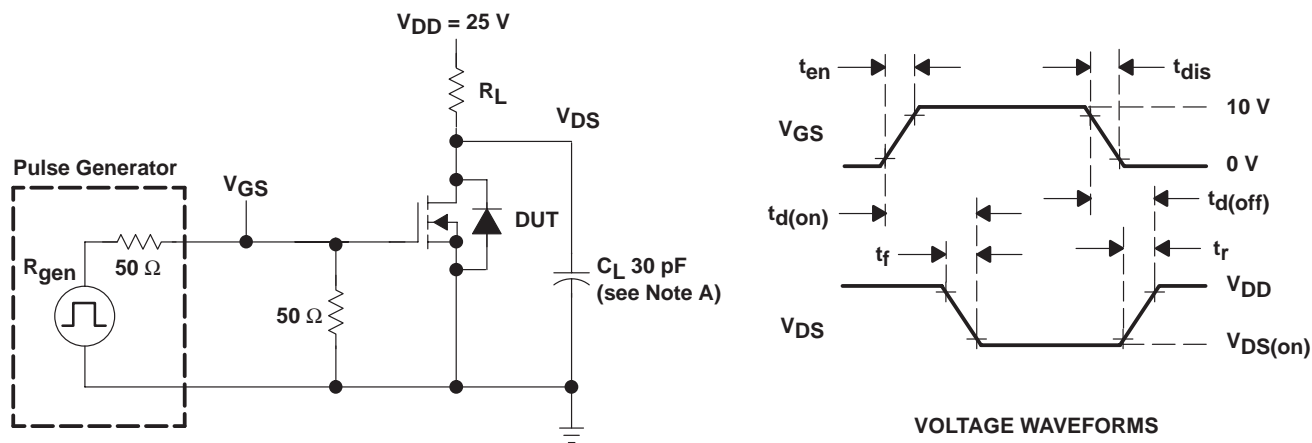


PARAMETER MEASUREMENT INFORMATION



$^\dagger I_{RM}$ = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

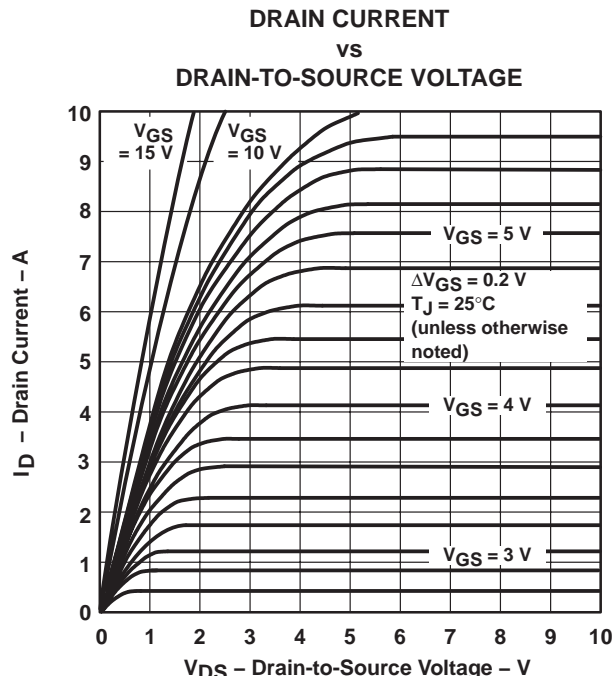
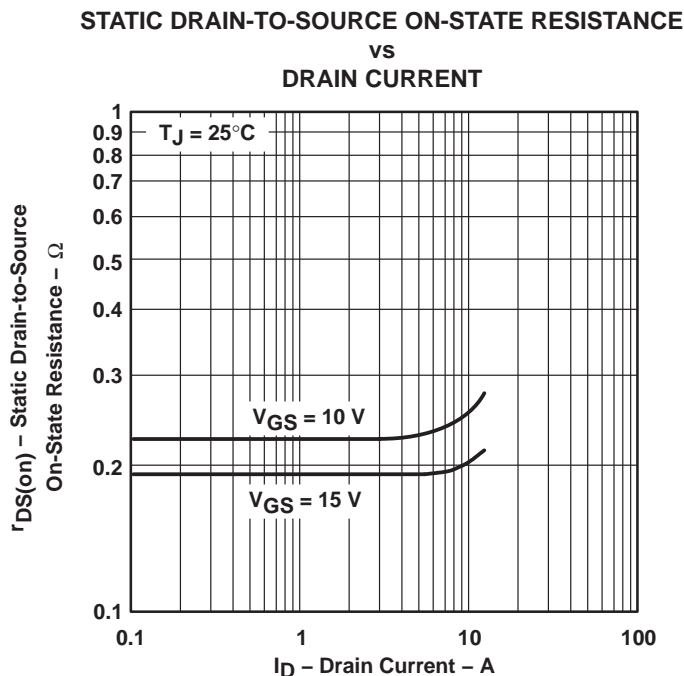
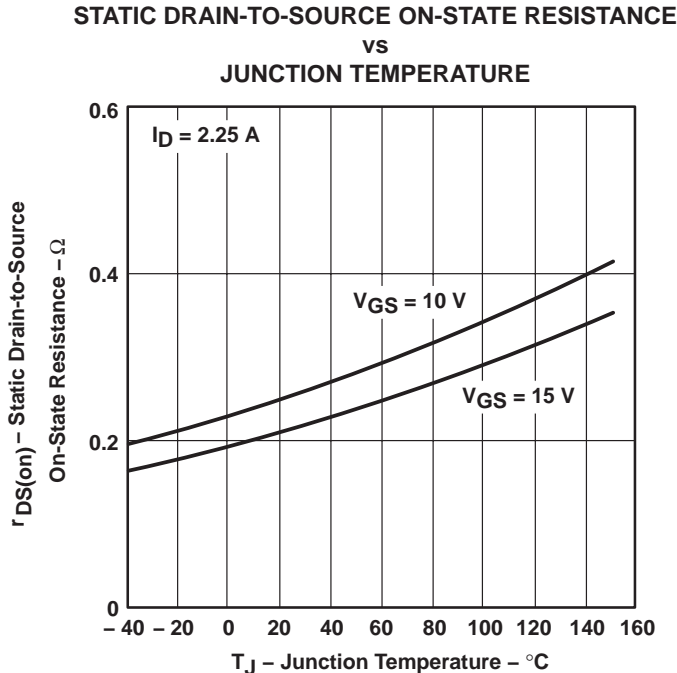
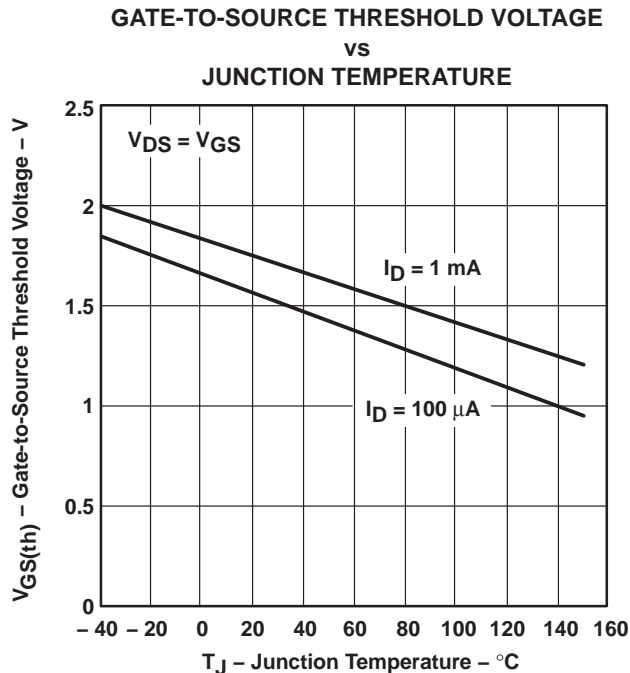


TEST CIRCUIT

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



TPIC1301 3-HALF H-BRIDGE GATE-PROTECTED POWER DMOS ARRAY

SLIS037 – NOVEMBER 1994

TYPICAL CHARACTERISTICS

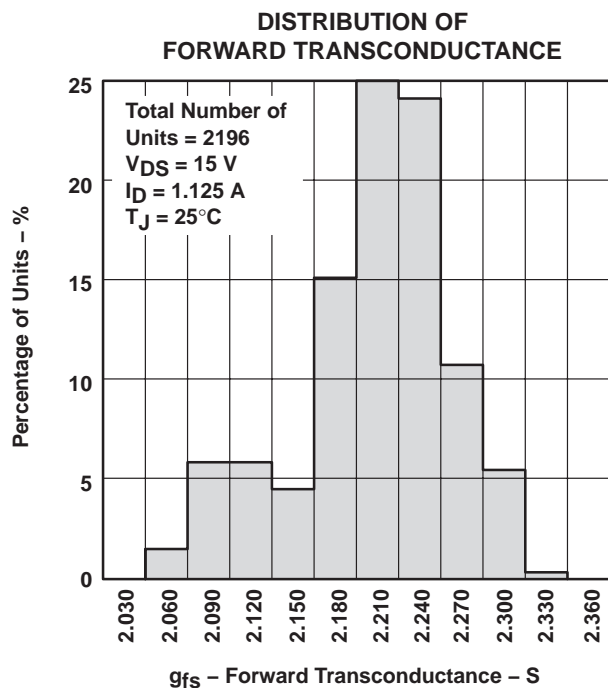


Figure 9

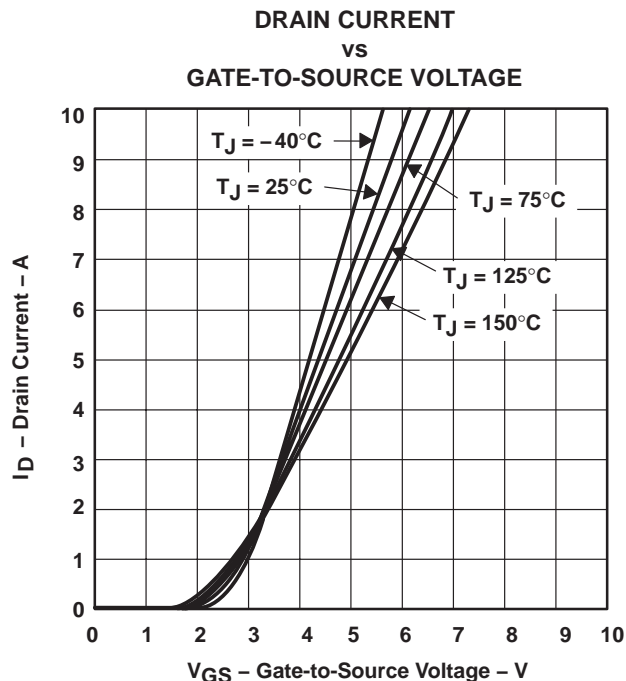


Figure 10

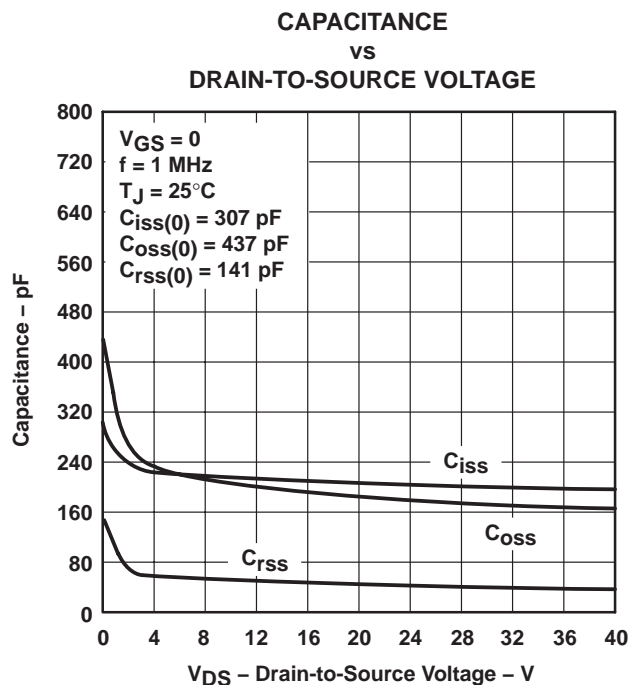


Figure 11

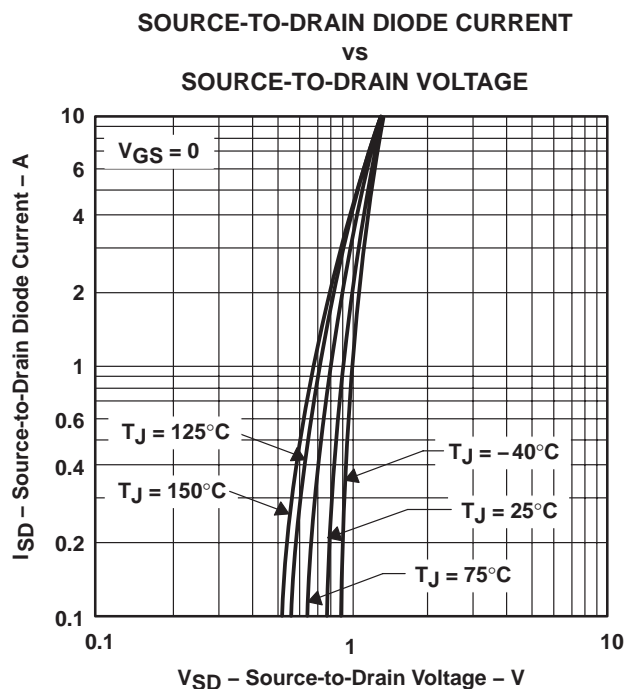


Figure 12



TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE

vs
GATE CHARGE

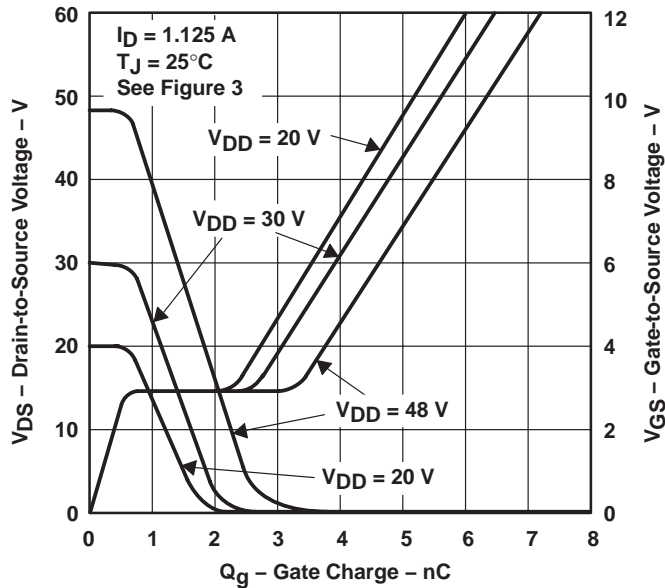


Figure 13

REVERSE RECOVERY TIME

vs
REVERSE di/dt

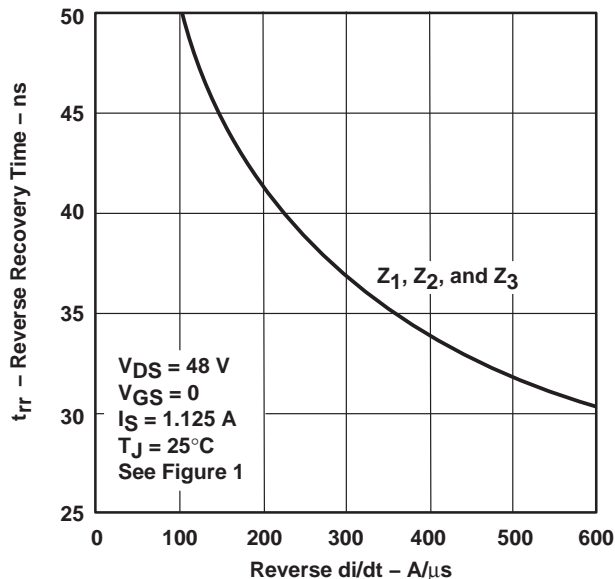


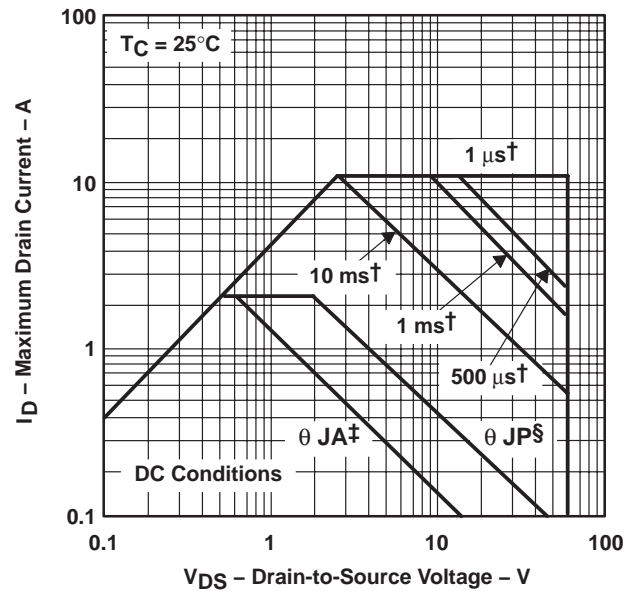
Figure 14

TPIC1301
3-HALF H-BRIDGE GATE-PROTECTED
POWER DMOS ARRAY

SLIS037 – NOVEMBER 1994

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
 ‡ Device mounted on FR4 printed-circuit board with no heatsink.
 § Device mounted in intimate contact with infinite heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

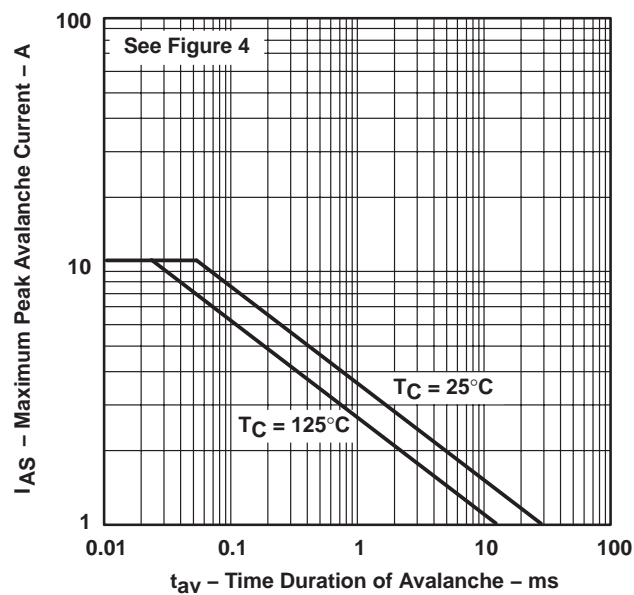
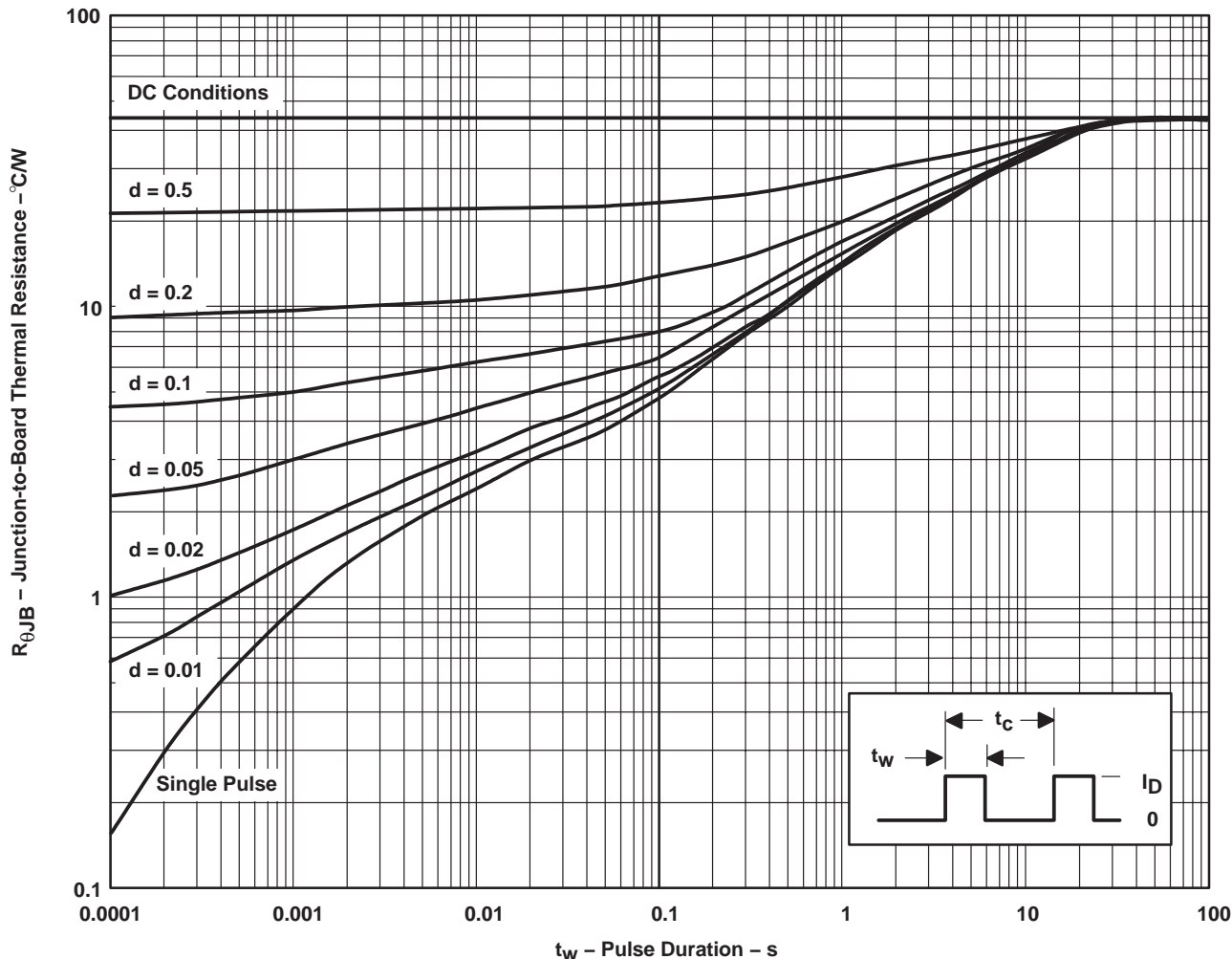


Figure 16

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
VS
PULSE DURATION



† Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink

NOTE A. $Z_{\theta B}(t) = r(t) R_{\theta JB}$
 t_w = pulse duration
 t_c = cycle time
 d = duty cycle = t_w/t_c

Figure 17

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPIC1301DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

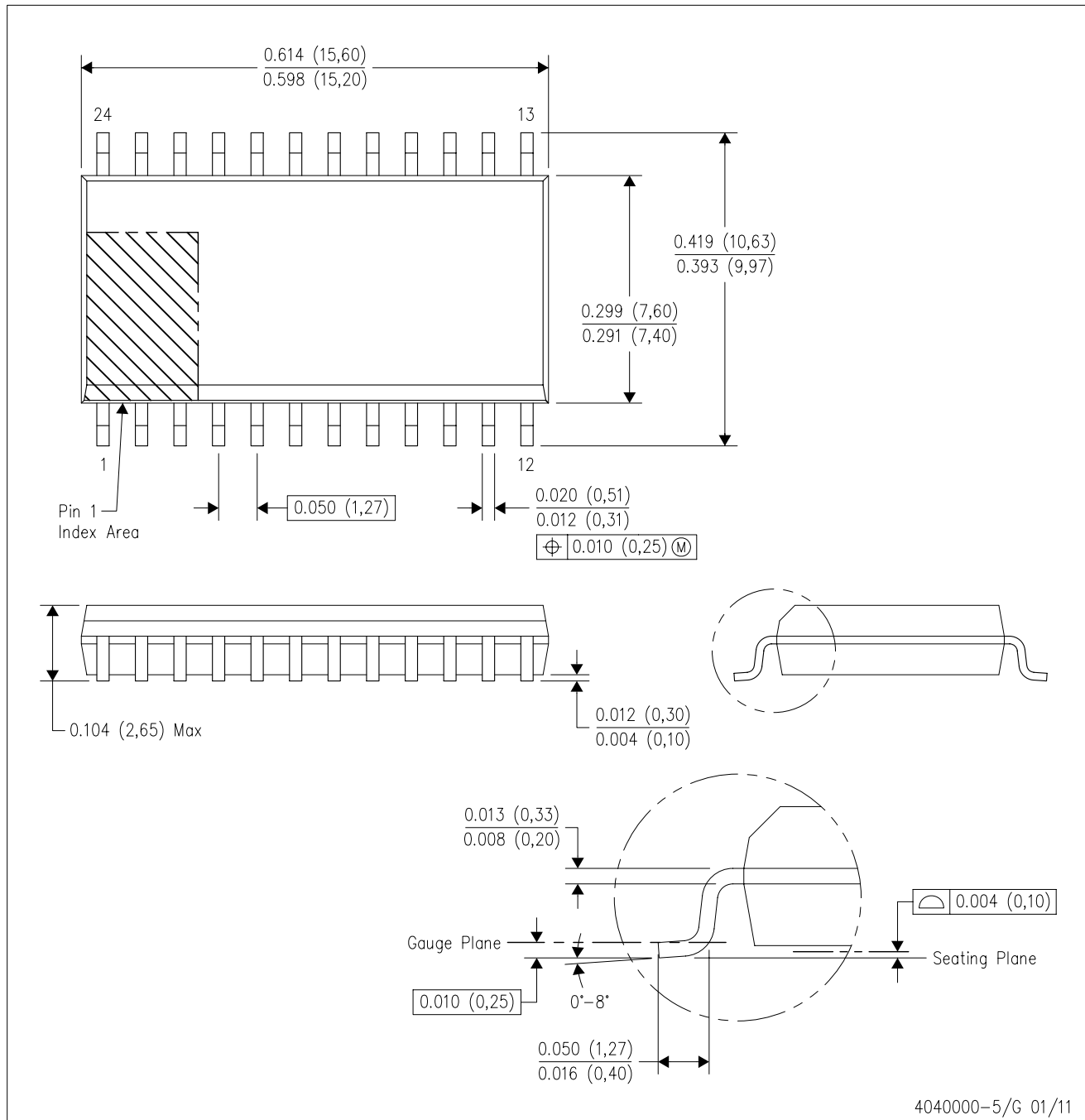
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video
Wireless	www.ti.com/wireless-apps

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated