Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package TO-92
20V	1.3Ω	0.5A	1.0V	TN0702N3

Features

❏ Low threshold — 1.0 volt max

❏ On resistance guaranteed at V_{GS} = 2, 3, and 5 volts

❏ High input impedance

❏ Low input capacitance —130pF typical

❏ Fast switching speeds

❏ Low on resistance

❏ Free from secondary breakdown

❏ Low input and output leakage

Applications

❏ Logic level interfaces

❏ Solid state relays

❏ Battery operated systems

❏ Photo voltaic drives

❏ Analog switches

❏ General purpose line drivers

❏ Telecom switches

Absolute Maximum Ratings

|	
Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds maximum.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option

S G D

TO-92

Note: See Package Outline section for dimensions.

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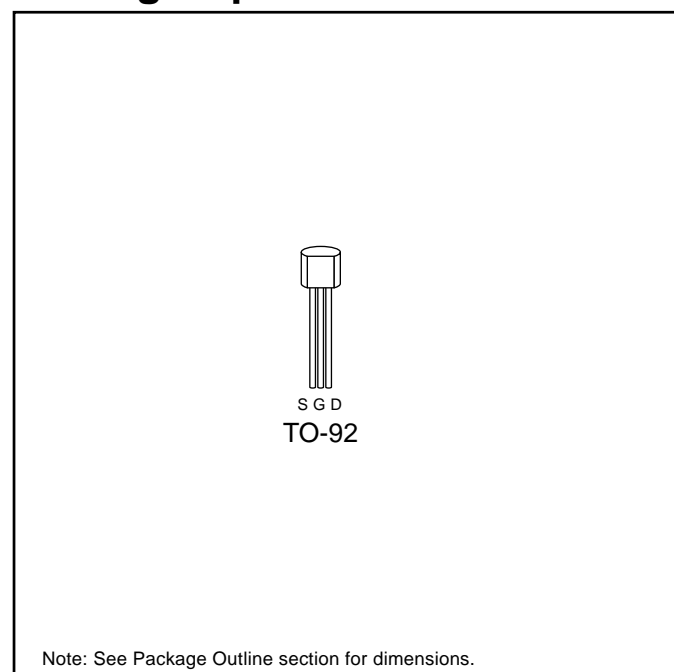
Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	0.53A	1.0A	1W	125	170	0.53A	1.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

| Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20			V	$V_{GS} = 0V$, $I_D = 1mA$
$V_{GS(th)}$	Gate Threshold Voltage	0.5	0.8	1.0	V	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			100	nA	$V_{DS} = 20V$, $V_{GS} = 0V$
				100	µA	$V_{DS} = 0.8$ Max Rating, $V_{GS} = 0V$, $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	0.5	1.0		A	$V_{GS} = V_{DS} = 5V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		4.0	5.0	Ω	$V_{GS} = 2V$, $I_D = 50mA$
			1.9	2.5		$V_{GS} = 3V$, $I_D = 200mA$
			1.0	1.3		$V_{GS} = 5V$, $I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/°C	$V_{GS} = 5V$, $I_D = 500mA$
G_{FS}	Forward Transconductance	100	500		m℧	$V_{DS} = 5V$, $I_D = 500mA$
C_{ISS}	Input Capacitance		130	200		
C_{OSS}	Common Source Output Capacitance		70	125	pF	$V_{GS} = 0V$, $V_{DS} = 20V$, f =1MHz
C_{RSS}	Reverse Transfer Capacitance		30	60		
$t_{d(ON)}$	Turn-ON Delay Time			20		
t_r	Rise Time			20	ns	$V_{DD} = 20V$, $I_D = 0.5A$, $R_{GEN} = 25\Omega$
$t_{d(OFF)}$	Turn-OFF Delay Time			30		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop			1.0	V	$V_{GS} = 0V$, $I_{SD} = 0.5A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwide stated. (Pulse test: 300 µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.
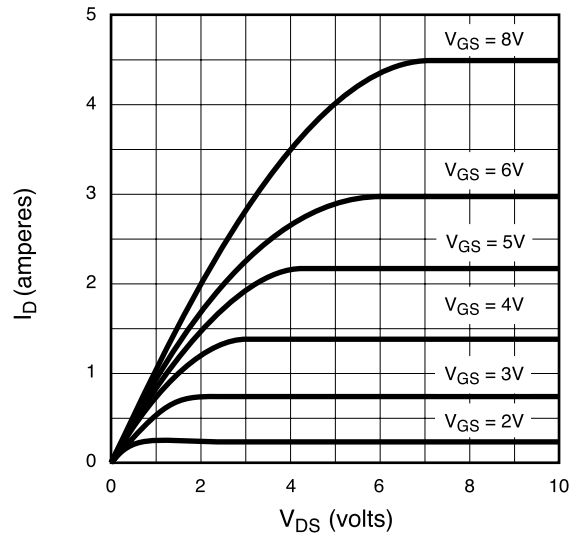
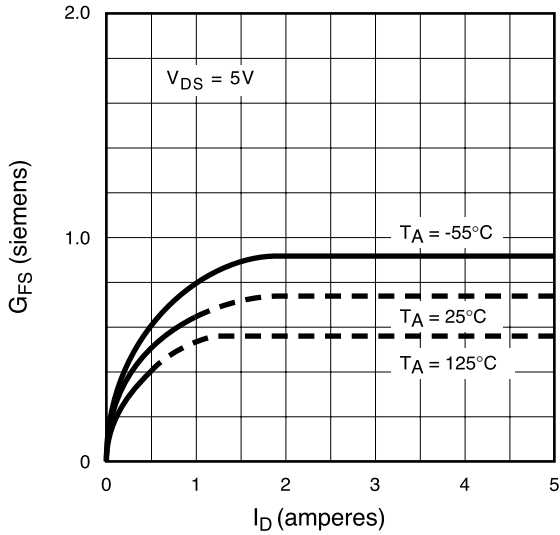## Switching Waveforms and Test Circuit
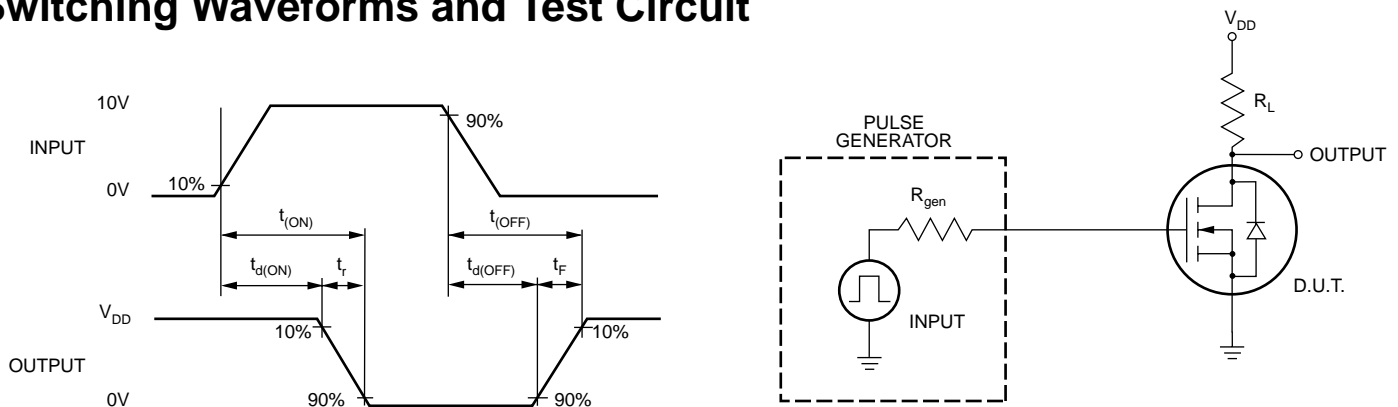
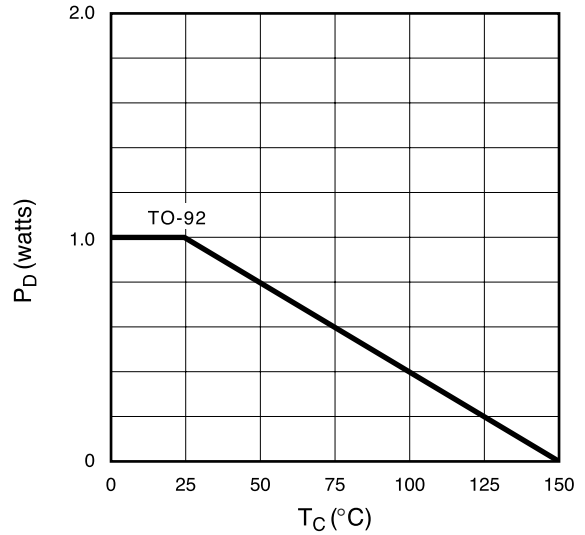# Typical Performance Curves

Output Characteristics
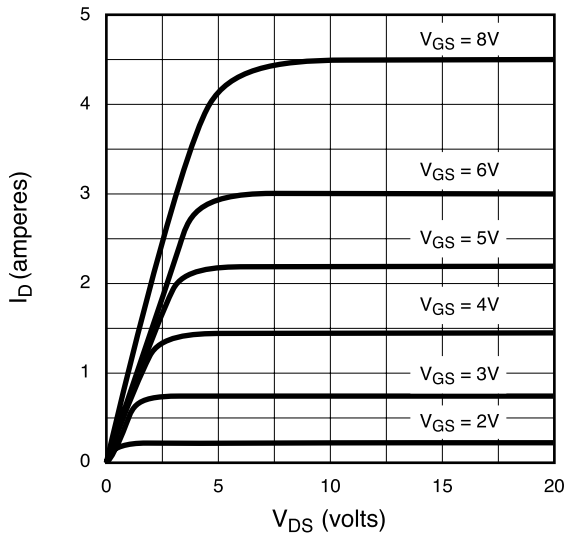
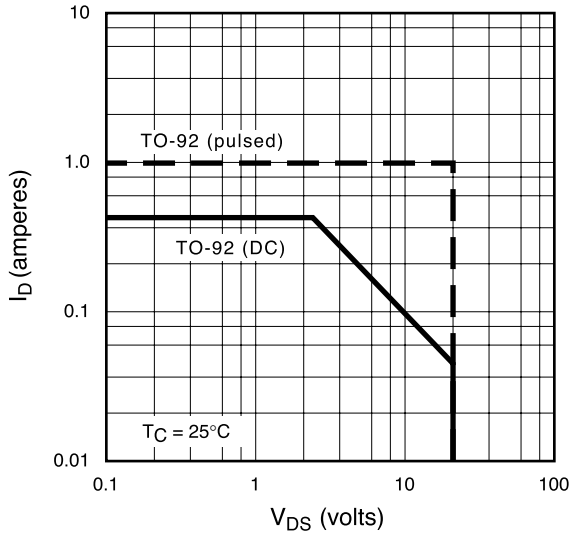### Saturation Characteristics

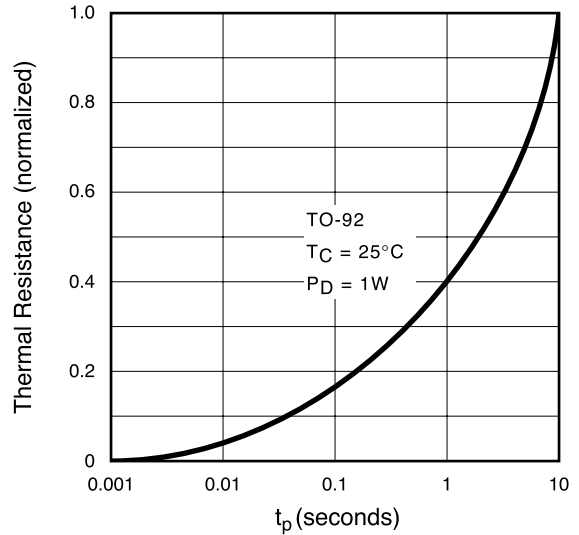### Transconductance vs. Drain Current

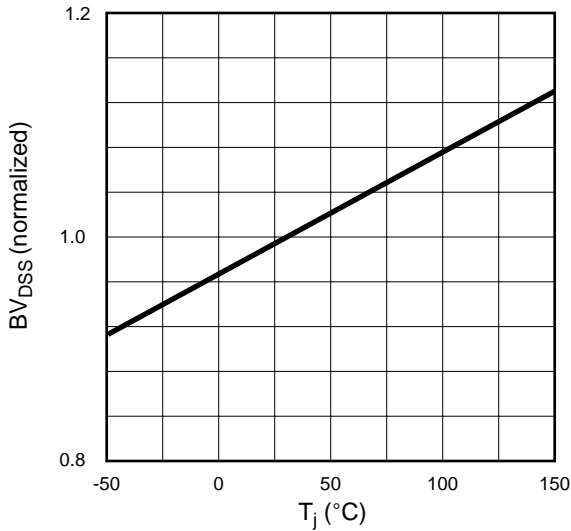### Power Dissipation vs. Case Temperature

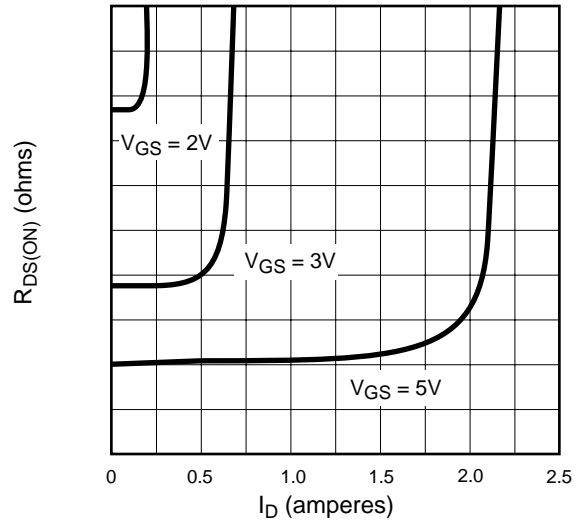### Maximum Rated Safe Operating Area

Thermal Response Characteristics
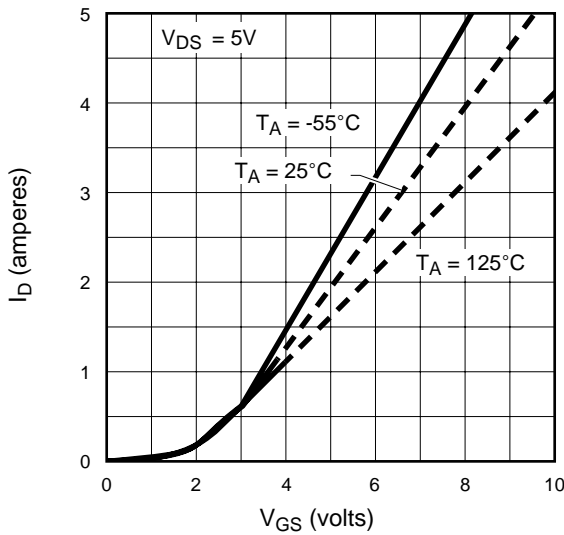
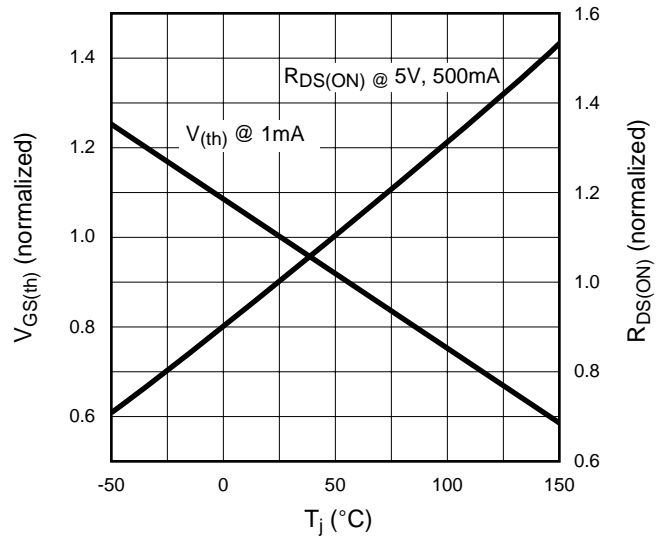## BV$_{DSS}$ Variation with Temperature

On-Resistance vs. Drain Current

Transfer Characteristics

V$_{(th)}$ and R$_{DS}$ Variation with Temperature
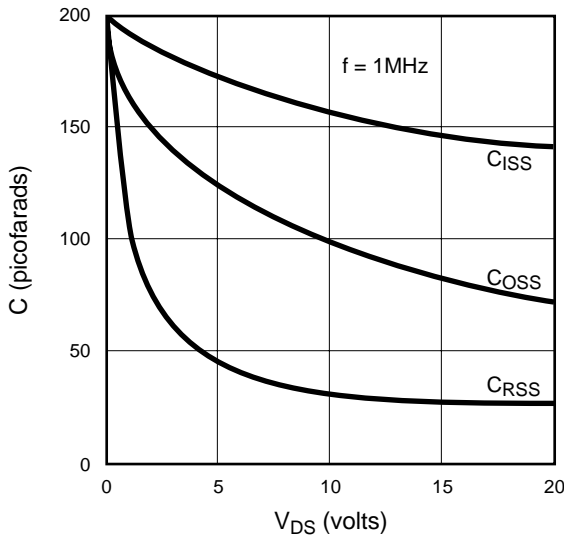

Capacitance vs. Drain-to-Source Voltage

Gate Drive Dynamic Characteristics

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