

# TOSHIBA MOS MEMORY PRODUCTS

## TMM27256BDI-15, TMM27256BDI-20

### DESCRIPTION

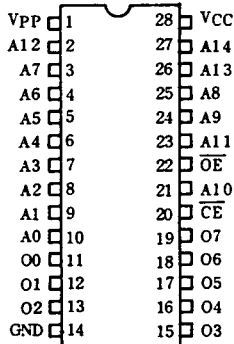
The TMM27256BDI is a 32,768 words × 8 bits ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM27256BDI's access time is 150ns/200ns, and the TMM27256BDI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input. For program operation, the programming is achieved by using the high speed programming mode. The TMM27256BDI is fabricated with the N-channel silicon double layer gate MOS technology.

### FEATURES

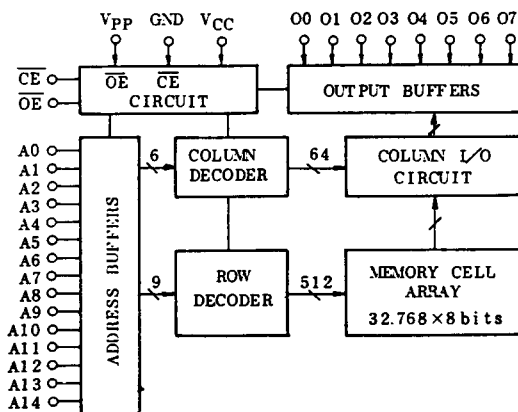
	-15	-20
V <sub>CC</sub>	5V±5%	
t <sub>ACC</sub>	150ns	200ns
I <sub>CC2</sub>	120mA	
I <sub>CC1</sub>	35mA	

- Wide operating temperature range -40 ~ 85°C
- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Pin compatible with i27256
- Standard 28 pin DIP cerdip package

### PIN CONNECTION



### BLOCK DIAGRAM



### PIN NAMES

A0~A14	Address Inputs
O0~O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V <sub>PP</sub>	Program Supply Voltage
V <sub>CC</sub>	Power Supply Voltage (+5V)
GND	Ground

### MODE SELECTION

MODE	PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O0 ~ O7 (11~13, 15~19)	POWER
Read		L	L	5V	5V	Date Out	Active
Output Deselect	*	H	High Impedance				
Standby	H	*	High Impedance			Standby	
Program	L	H		1) 12.5V	1) 6V	Data In	Active
Program Inhibit	H	H		2) 12.75V	2) 6.25V	High Impedance	
Program Verify	*	L				Data Out	

\*: H or L

1): HIGH SPEED PROGRAMMING MODE I  
2): HIGH SPEED PROGRAMMING MODE II

# TMM27256BDI-15, TMM27256BDI-20

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
$V_{CC}$	$V_{CC}$ Power Supply Voltage	-0.6 ~ 7.0	V
$V_{PP}$	Program Supply Voltage	-0.6 ~ 14.0	V
$V_{IN}$	Input Voltage	-0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ~ 7.0	V
$P_D$	Power Dissipation	1.5	W
$T_{SOLDER}$	Soldering Temperature • Time	260 • 10	°C • sec
$T_{STG}$	Storage Temperature	-65 ~ 125	°C
$T_{OPR}$	Operating Temperature	-40 ~ 85	°C

## READ OPERATION

### D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27256BDI-12/20
$T_a$	Operating Temperature	-40 ~ 85°C
$V_{CC}$	$V_{CC}$ Power Supply Voltage	5V±5%
$V_{PP}$	$V_{pp}$ Power Supply Voltage	2.2 ~ $V_{CC}+0.6V$

### D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$I_{LI}$	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
$I_{LO}$	Output Leakage Current	$V_{OUT}=0.4 \sim V_{CC}$	-	-	±10	μA
$I_{CC1}$	Supply Current (Standby)	$\overline{CE}=V_{IH}$	-	-	35	mA
$I_{CC2}$	Supply Current (Active)	$\overline{CE}=V_{IL}$	-	-	120	mA
$V_{IH}$	Input High Voltage	-	2.2	-	$V_{CC}+1.0$	V
$V_{IL}$	Input Low Voltage	-	-0.3	-	0.8	V
$V_{OH}$	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
$V_{OL}$	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
$I_{PPI}$	$V_{pp}$ Current	$V_{pp}=0 \sim V_{CC}+0.6$	-	-	±10	μA

# TMM27256BDI-15, TMM27256BDI-20

## A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27256BDI-15		TMM27256BDI-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
$t_{ACC}$	Address Access Time	-	150	-	200	ns
$t_{CE}$	$\overline{CE}$ to Output Valid	-	150	-	200	ns
$t_{OE}$	$\overline{OE}$ to Output Valid	-	70	-	70	ns
$t_{DF1}$	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
$t_{DF2}$	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
$t_{OH}$	Output Data Hold Time	0	-	0	-	ns

## A.C. TEST CONDITIONS

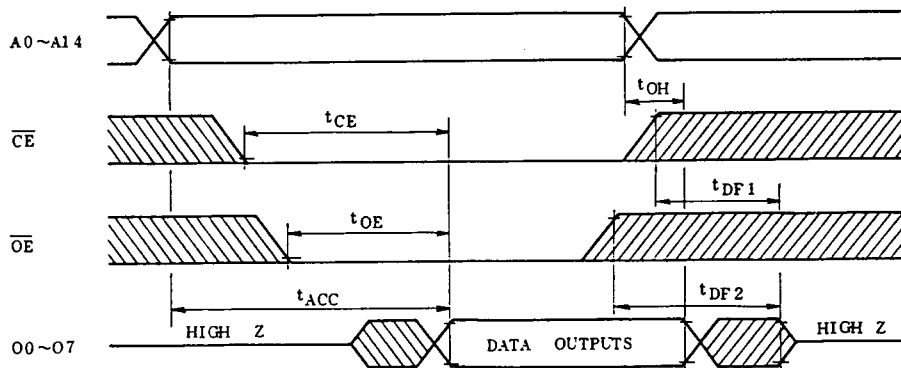
- Output Load : 1 TTL Gate and  $C_L=100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE\* ( $T_a=25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN}=0\text{V}$	-	4	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT}=0\text{V}$	-	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

## TIMING WAVEFORMS (READ)



# TMM27256BDI-15, TMM27256BDI-20

PROGRAM OPERATION (HIGH SPEED PROGRAMMING MODE I)

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{IH}$	Input High Voltage	2.2	-	$V_{CC}+1.0$	V
$V_{IL}$	Input Low Voltage	-0.3	-	0.8	V
$V_{CC}$	$V_{CC}$ Power Supply Voltage	5.75	6.0	6.25	V
$V_{PP}$	$V_{PP}$ Power Supply Voltage	12.0	12.5	13.0	V

D.C. AND OPERATING CHARACTERISTICS ( $T_a=25\pm 5^\circ\text{C}$ ,  $V_{CC}=6V\pm 0.25V$ ,  $V_{PP}=12.5V\pm 0.5V$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$I_{LI}$	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	$\pm 10$	$\mu\text{A}$
$V_{OH}$	Output High Voltage	$I_{OH}=-400\mu\text{A}$	2.4	-	-	V
$V_{OL}$	Output Low Voltage	$I_{OL}=2.1\text{mA}$	-	-	0.4	V
$I_{CC}$	$V_{CC}$ Supply Current	-	-	-	120	mA
$I_{PP2}$	$V_{PP}$ Supply Current	$V_{PP}=13.0V$	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS ( $T_a=25\pm 5^\circ\text{C}$ ,  $V_{CC}=6V\pm 0.25V$ ,  $V_{PP}=12.5V\pm 0.5V$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$t_{AS}$	Address Setup Time	-	2	-	-	$\mu\text{s}$
$t_{AH}$	Address Hold Time	-	2	-	-	$\mu\text{s}$
$t_{CES}$	$\overline{CE}$ Setup Time	-	0	-	-	ns
$t_{CEH}$	$\overline{CE}$ Hold Time	-	0	-	-	ns
$t_{OES}$	$\overline{OE}$ Setup Time	-	2	-	-	$\mu\text{s}$
$t_{DS}$	Data Setup Time	-	2	-	-	$\mu\text{s}$
$t_{DH}$	Data Hold Time	-	2	-	-	$\mu\text{s}$
$t_{VPS}$	$V_{PP}$ Setup Time	-	2	-	-	$\mu\text{s}$
$t_{VCS}$	$V_{CC}$ Setup Time	-	2	-	-	$\mu\text{s}$
$t_{PW}$	Initial Program Pulse Width	$\overline{CE}=V_{IL}$ , $\overline{OE}=V_{IH}$	0.95	1.0	1.05	ms
$t_{OPW}$	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
$t_{OE}$	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
$t_{DFP}$	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and  $C_L$  (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

# TMM27256BDI-15, TMM27256BDI-20

## PROGRAM OPERATION (HIGH SPEED PROGRAMMING MODE II)

### D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	6.0	6.25	6.5	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.5	12.75	13.0	V

### D.C. AND OPERATING CHARACTERISTICS (T<sub>a</sub>=25±5°C, V<sub>CC</sub>=6.25V±0.25V, V<sub>PP</sub>=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0 ~ V <sub>CC</sub>	-	-	±10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	-	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	-	-	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	-	-	-	120	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> =13.0V	-	-	50	mA

### A.C. PROGRAMMING CHARACTERISTICS (T<sub>a</sub>=25±5°C, V<sub>CC</sub>=6.25V±0.25V, V<sub>PP</sub>=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	-	2	-	-	μs
t <sub>AH</sub>	Address Hold Time	-	2	-	-	μs
t <sub>CES</sub>	$\overline{CE}$ Setup Time	-	0	-	-	ns
t <sub>CEH</sub>	$\overline{CE}$ Hold Time	-	0	-	-	ns
t <sub>OES</sub>	$\overline{OE}$ Setup Time	-	2	-	-	μs
t <sub>DS</sub>	Data Setup Time	-	2	-	-	μs
t <sub>DH</sub>	Data Hold Time	-	2	-	-	μs
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	-	2	-	-	μs
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	-	2	-	-	μs
t <sub>PW</sub>	Program Pulse Width	$\overline{CE}=V_{IL}$ , $\overline{OE}=V_{IH}$	0.095	0.1	0.105	ms
t <sub>OE</sub>	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t <sub>DFP</sub>	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

### A.C. TEST CONDITIONS

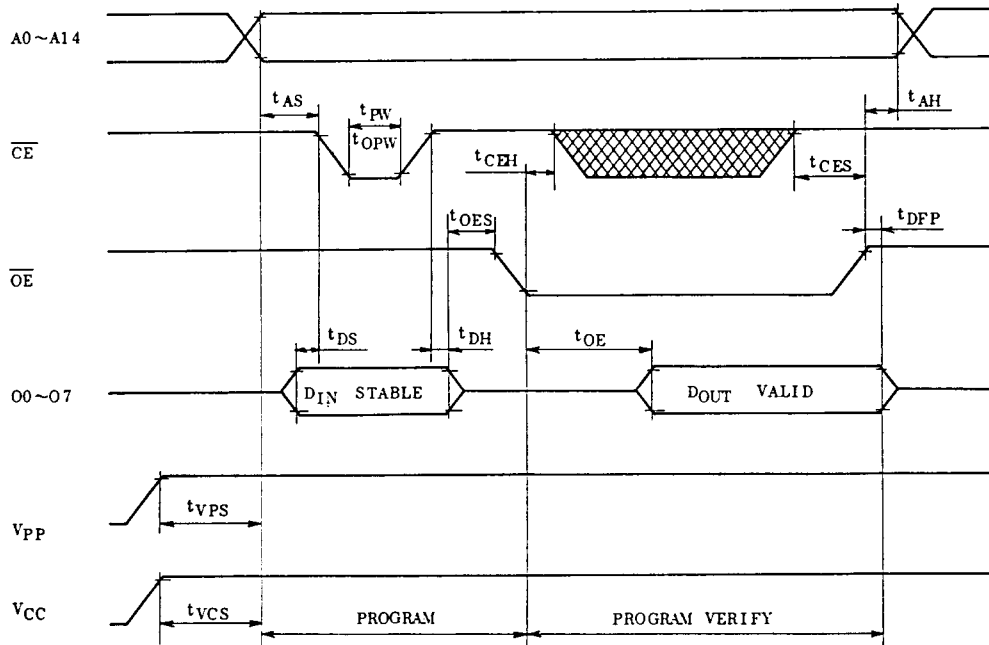
- Output Load : 1 TTL Gate and C<sub>L</sub> (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

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## TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAMMING MODE I ( $V_{CC}=6V\pm 0.25V$ ,  $V_{PP}=12.5V\pm 0.5V$ )

HIGH SPEED PROGRAMMING MODE II ( $V_{CC}=6.25V\pm 0.25V$ ,  $V_{PP}=12.75V\pm 0.25V$ )



Note 1.  $V_{CC}$  must be applied simultaneously or before  $V_{pp}$  and cut off simultaneously or after  $V_{pp}$ .

2. Removing the device from socket and setting the device in socket with  $V_{pp}=12.5V \pm 0.5V$  or  $V_{pp}=12.75V \pm 0.25V$  may cause permanent damage to the device.

3. The  $V_{pp}$  supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the  $V_{pp}$  terminal. When the switching pulse voltage is applied to the  $V_{pp}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

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## ERASURE CHARACTERISTICS

The TMM27256BDI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (ultraviolet light intensity [ $\text{w}/\text{cm}^2$ ]  $\times$  exposure time [sec.]) for erasure should be a minimum of 15 [ $\text{w}\cdot\text{sec}/\text{cm}^2$ ].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [ $\mu\text{w}/\text{cm}^2$ ] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [ $\mu\text{w}/\text{cm}^2$ ]  $\times$  (20  $\times$  60) [sec]  $\approx$  15 [ $\text{w}\cdot\text{sec}/\text{cm}^2$ ].)

The TMM27256BDI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the florescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals -Toshiba EPROM Protect Seal AC901- are available.

## OPERATION INFORMATION

The TMM27256BDI's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

PIN NAMES (NUMBER)		$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}$ (22)	Vpp (1)	VCC (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read Operation ( $T_a=0 \sim 70^\circ\text{C}$ )	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation ( $T_a=25\pm 5^\circ\text{C}$ )	Program	L	H	12.5V <sup>1)</sup>	6V <sup>1)</sup>	Data In	Active
	Program Inhibit	H	H	12.75V <sup>2)</sup>	6.25V <sup>2)</sup>	High Impedance	
	Program Verify	*	L			Data Out	

Note: H;  $V_{IH}$ , L;  $V_{IL}$ , \*;  $V_{IH}$  or  $V_{IL}$

1); HIGH SPEED PROGRAMMING MODE I

2); HIGH SPEED PROGRAMMING MODE II

## READ MODE

The TMM27256BDI has two control functions. The chip enable ( $\overline{\text{CE}}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{\text{OE}}$ ) controls the output buffers, independent of device selection. Assuming that  $\overline{\text{CE}}=\overline{\text{OE}}=V_{IL}$ , the output data is valid at the outputs after address access time from stabilizing of all addresses.

The  $\overline{\text{CE}}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{\text{CE}}=V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{\text{OE}}$ .

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### OUTPUT DESELECT MODE

Assuming that  $\overline{CE}=V_{IH}$  or  $\overline{OE}=V_{IH}$ , the outputs will be in a high impedance state. So two or more TMM27256BDI's can be connected together on a common bus line. When  $\overline{CE}$  is decoded for device selection, all deselected devices are in a low power standby mode.

### STANDBY MODE

The TMM27256BDI has a low power standby mode controlled by the  $\overline{CE}$  signal. By applying a high level to the  $\overline{CE}$  input, the TMM27256BDI is placed in the standby mode which reduce 70% of the operating current by applying TTL-high level and then the outputs are in a high impedance state, independent of the  $\overline{OE}$  inputs.

### PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256BDI are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TMM27256BDI is in the programming mode when the  $V_{pp}$  input is at 12.5V or 12.75V and  $\overline{CE}$  is at TTL-Low level under  $\overline{OE}=V_{IH}$ .

The TMM27256BDI can be programmed any location at anytime either individually, sequentially, or at random.

### PROGRAM VERIFY MODE

The verify mode is to check if desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}$  at  $V_{IL}$  and  $\overline{CE}$  at  $V_{IH}$  or  $V_{IL}$ .

### PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.5V or 12.75V) is applied to  $V_{pp}$  terminal, a TTL high level  $\overline{CE}$  input inhibits the TMM27256BDI from being programmed. Programming of two or more TMM27256BDI's in parallel with different data is easily accomplished. That is, all inputs except for  $\overline{CE}$  and  $\overline{OE}$  may be commonly connected, and a TTL Low level program pulse is applied to the  $\overline{CE}$  of the desired device only and TTL high level signal is applied to the other devices.

## HIGH SPEED PROGRAMMING MODE I

This high speed programming mode I is performed at  $V_{CC}=6.0V$  and  $V_{pp}=12.5V$ .

The programming is achieved by applying a single TTL low level 1ms pulse to the  $\overline{CE}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with pulse width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{pp}=5V$ .

## HIGH SPEED PROGRAMMING MODE II

The program time can be greatly decreased by using this high speed programming mode II. This high speed programming mode II is performed at  $V_{CC}=6.25V$  and  $V_{pp}=12.75V$ .

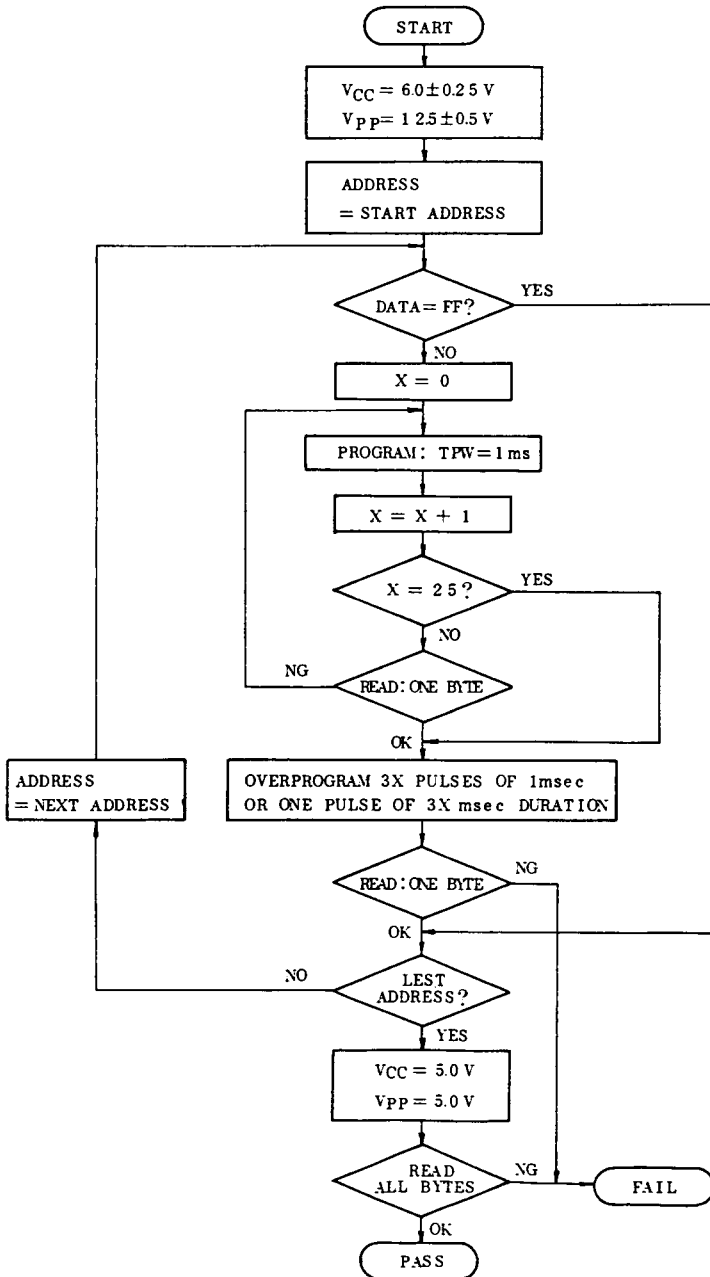
The programming is achieved by applying a single TTL low level 0.1ms pulse to the CE input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{pp}=5V$ .

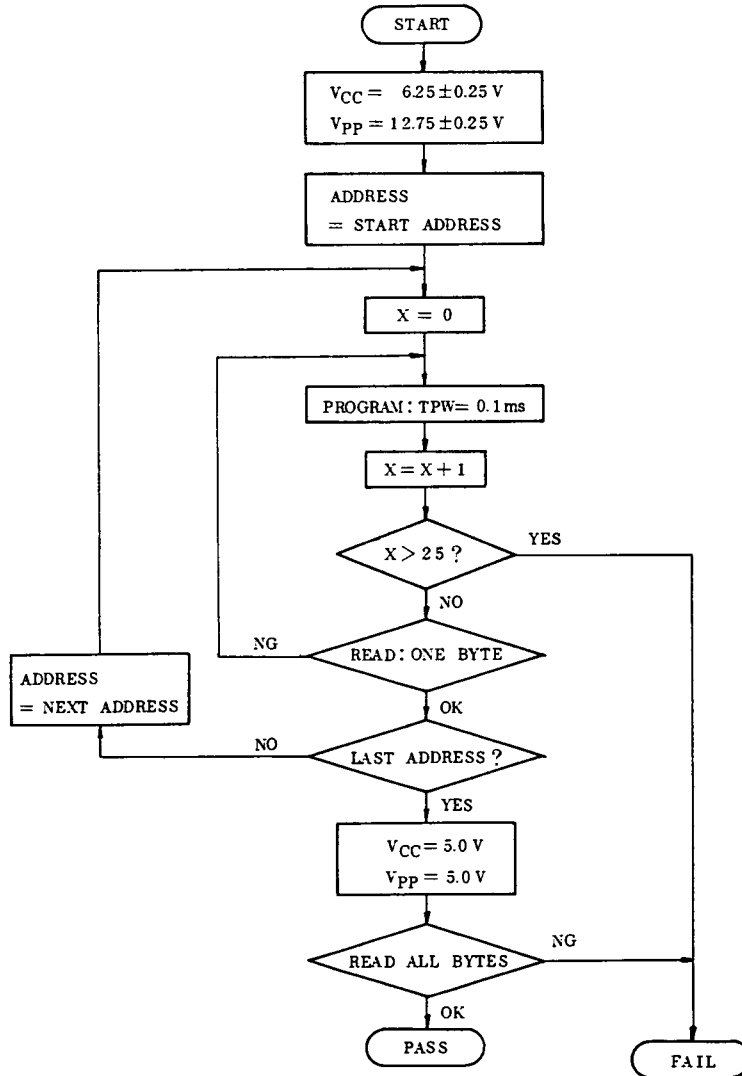
# TMM27256BDI-15, TMM27256BDI-20

## HIGH SPEED PROGRAMMING MODE I FLOW CHART



# TMM27256BDI-15, TMM27256BDI-20

## HIGH SPEED PROGRAMMING MODE II FLOW CHART



# TMM27256BDI-15, TMM27256BDI-20

## ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM27256BDI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TMM27256BDI by using this mode before program operation and automatically set program voltage ( $V_{pp}$ ) and algorithm.

Electric Signature mode is set up when  $12V$  is applied to address line A9 and the rest of address lines is set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TMM27256BDI.

SIGNATURE \ PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	$V_{IL}$	1	0	0	1	1	0	0	0	98
Device Code	$V_{IH}$	0	1	0	1	0	1	0	0	54

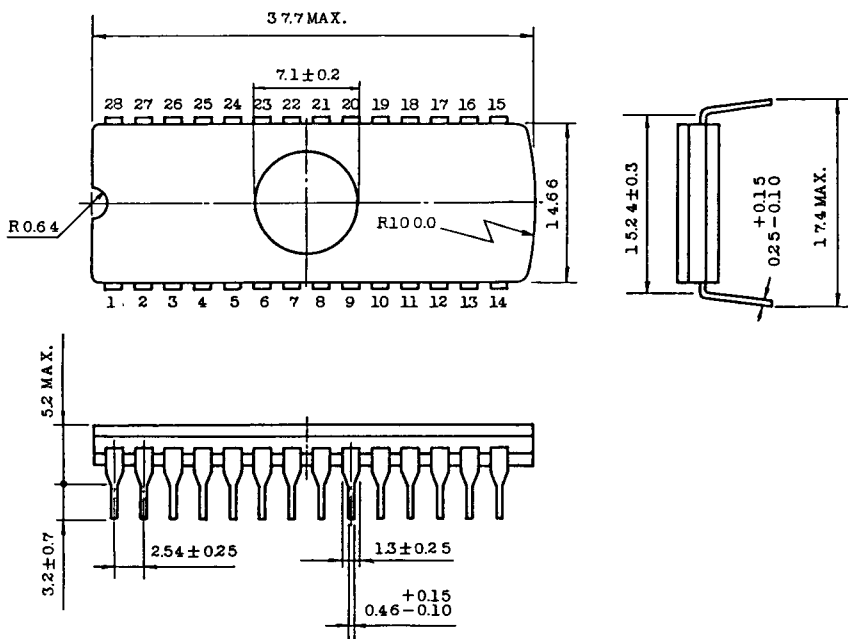
Notes: A9=12V±0.5V

A1 ~ A8, A10 ~ A14,  $\overline{CE}$ ,  $\overline{OE}$ = $V_{IL}$

# TMM27256BDI-15, TMM27256BDI-20

## OUTLINE DRAWINGS

Unit in mm



Note 2

Note 1

- Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.