TOSHIBA MOS MEMORY PRODUCTS

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

TMM27128AD-15, TMM27128AD-150
TMM27128AD 20, TMM27128AD-200

DESCRIPTION

The TMM27128AD is a 16,384 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM 27128AD's access time is 150ns/200ns, and the TMM27128AD operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the program is achieved by using the high speed programming mode.

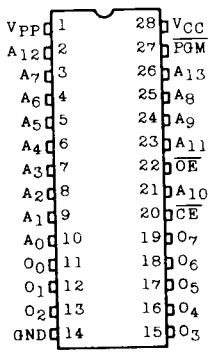
The TMM27128AD is fabricated with the N-channel silicon double layer gate MOS technolgy.

FEATURES

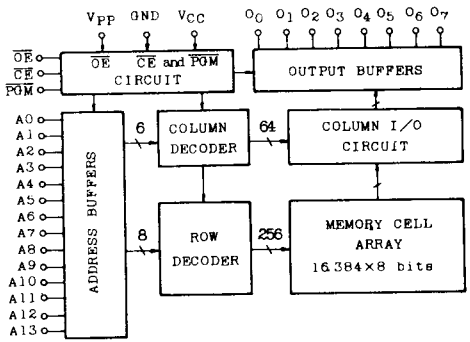
	−15	−20	−150	−200
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA		120mA	
I_{CC1}	30mA		35mA	

- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{13}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STRG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27128AD-15/20	TMM27128AD-150/200
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}±0.6V	2.0~V_{CC}+0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−15/20	—	—	30	mA
			−150/200	—	—	35	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−15/20	—	—	100	mA
			−150/200	—	—	120	
V_{IH}	Input High Voltage	—		2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6		—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27128AD-15/150		TMM27128AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

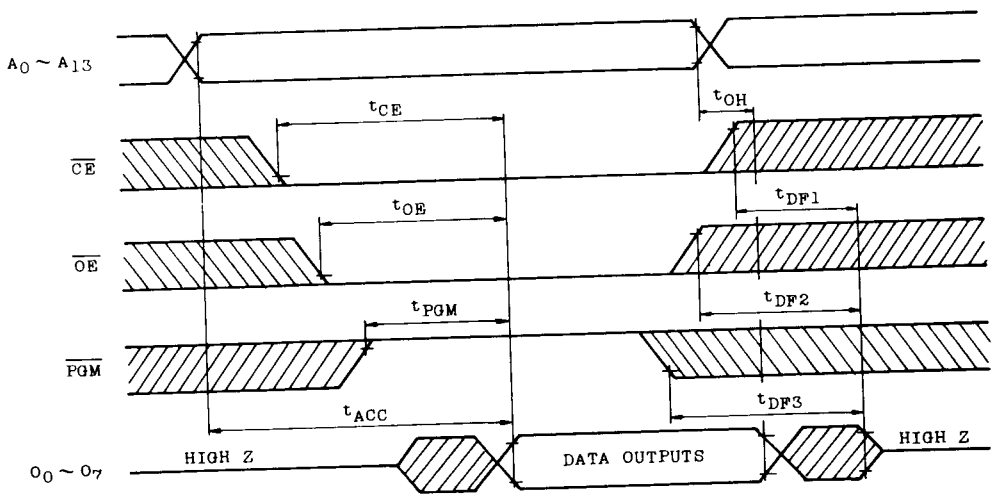
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	—	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	—	8	12	pF

* This paramater is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

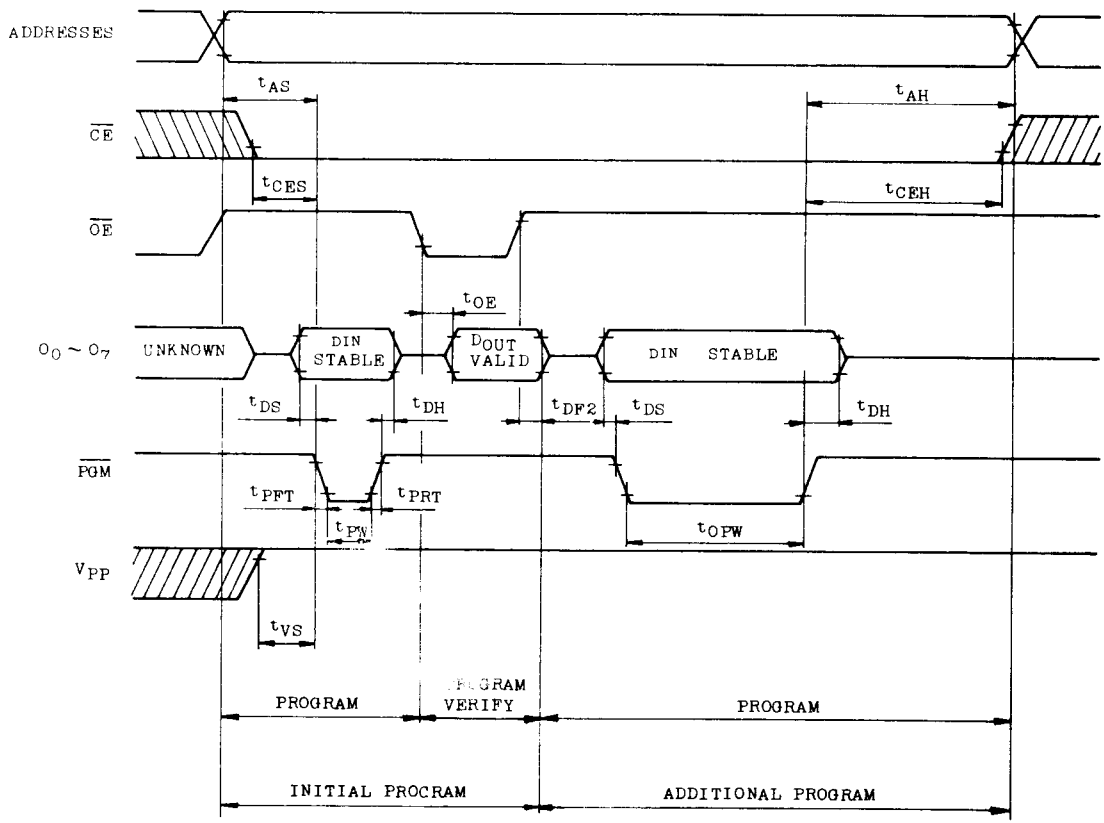
($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3	78.75	ms
t_{PRT}	Program pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output is High-Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27128AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W.sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27128AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27128AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES (NUMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
READ OPERATION (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27128AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in high impedance state.

Thus, two or more TMM27128AD's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128AD has a low power standby mode conntrolled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM27128AD is placed in the standby mode which reduces 70% of operating current. The outputs are in a high impedence state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128AD are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The levels required for all inputs are TTL.

The TMM27128AD can be programmed at any location, anytime — either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM27128AD from being programmed.

Programming of two or more TMM27128AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

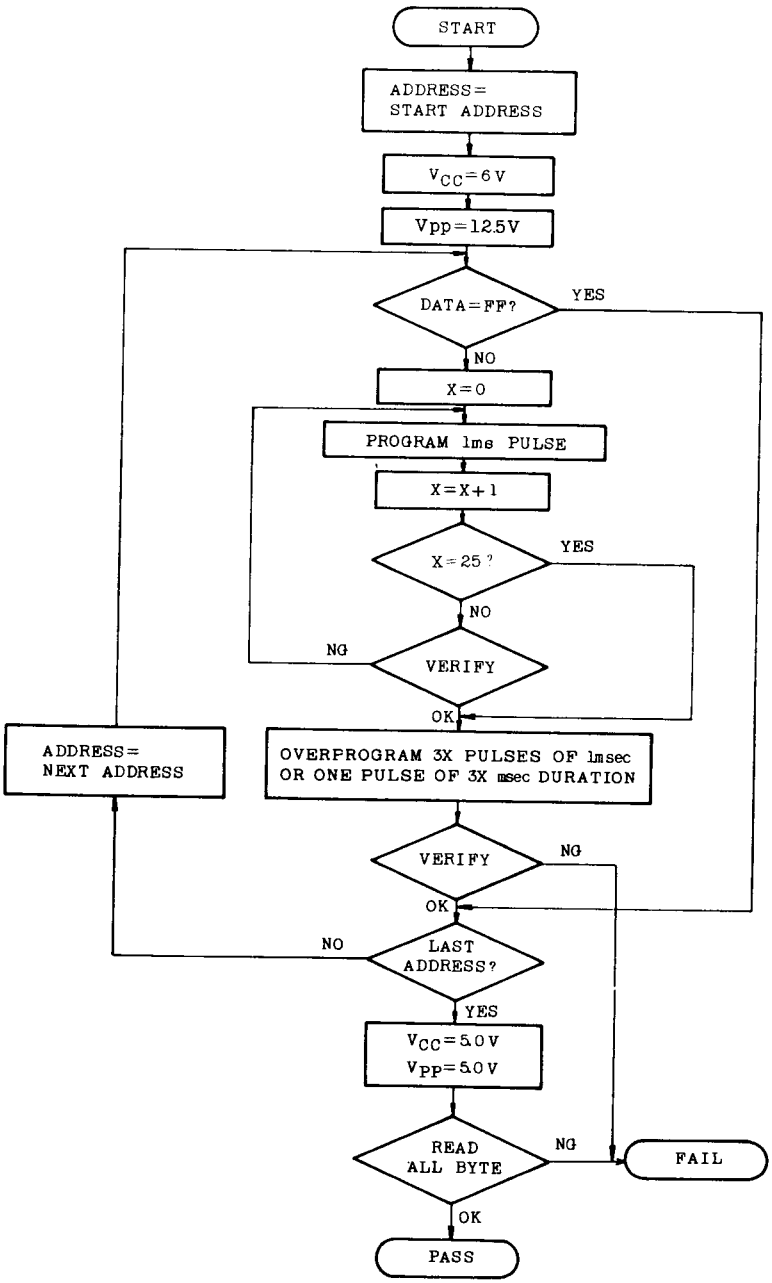
If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

The High Speed Program II Algorithm (shown in figure 2, page G-5) may also be used to reduce the programming time further.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27128AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM2764AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output is this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

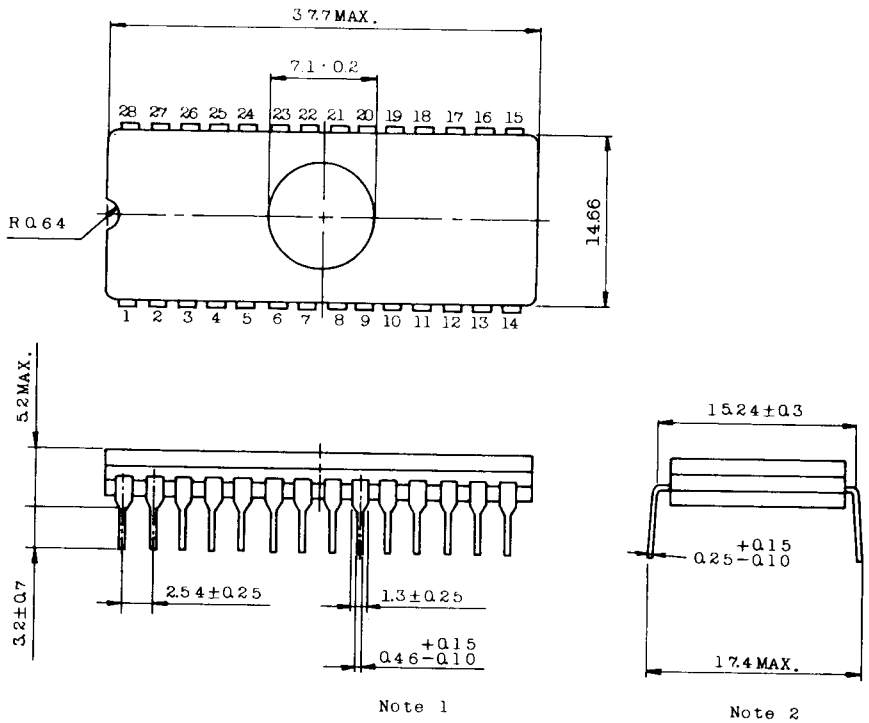
The following table shows electric signature of the TMM27128AD.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	1	0	0	1	1	D3

Notes : A9 = 12V±0.5V
A1 ~ A8, A10 ~ A13, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.