TL7702A, TL7705A, TL7709A, TL7712A, TL7715A
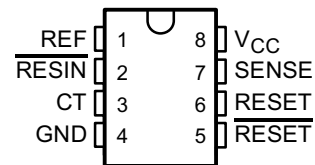# SUPPLY-VOLTAGE SUPERVISORS

SLVS028E – APRIL 1983 – REVISED JULY 1999

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Wide Supply-Voltage Range**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

D OR P PACKAGE
(TOP VIEW)

REF	1	8 V_{CC}
$\overline{RESIN}$	2	7 SENSE
CT	3	6 $\overline{RESET}$
GND	4	5 RESET

description

The TL77xxA family of integrated-circuit supply-voltage supervisors is specifically designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{RESET}$ output becomes active (low) when V_{CC} attains a value approaching 3.6 V. At this point (assuming that SENSE is above V_{IT+}), the delay timer function activates a time delay, after which outputs $\overline{RESET}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{RESET}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d = 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

During power down (assuming that SENSE is below V_{IT-}), the outputs remain active until the V_{CC} falls below a maximum of 2 V. After this, the outputs are undefined.

An external capacitor (typically 0.1 μF for the TL77xxAC and TL77xxAI) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL77xxAC series is characterized for operation from 0°C to 70°C. The TL77xxAI series is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	TL7702ACD TL7705ACD TL7709ACD TL7712ACD TL7715ACD	TL7702ACP TL7705ACP TL7709ACP TL7712ACP TL7715ACP	TL7702ACY TL7705ACY TL7709ACY TL7712ACY TL7715ACY
−40°C to 85°C	TL7702AID TL7705AID TL7709AID TL7712AID TL7715AID	TL7702AIP TL7705AIP TL7709AIP TL7712AIP TL7715AIP	— — — — —

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL7702ACDR). Chip forms are tested at 25°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TL7702A, TL7705A, TL7709A, TL7712A, TL7715A
SUPPLY-VOLTAGE SUPERVISORS

functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.
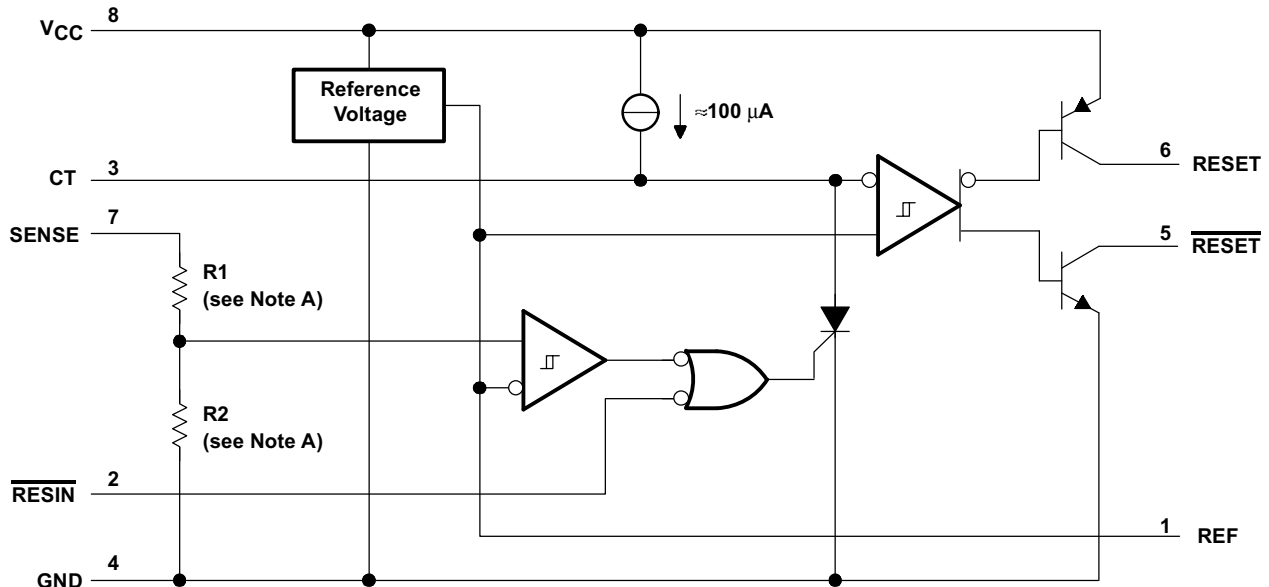
NOTES: A. TL7702A: R1 = 0 Ω, R2 = open
TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ
B. Resistor values shown are nominal.

timing diagram
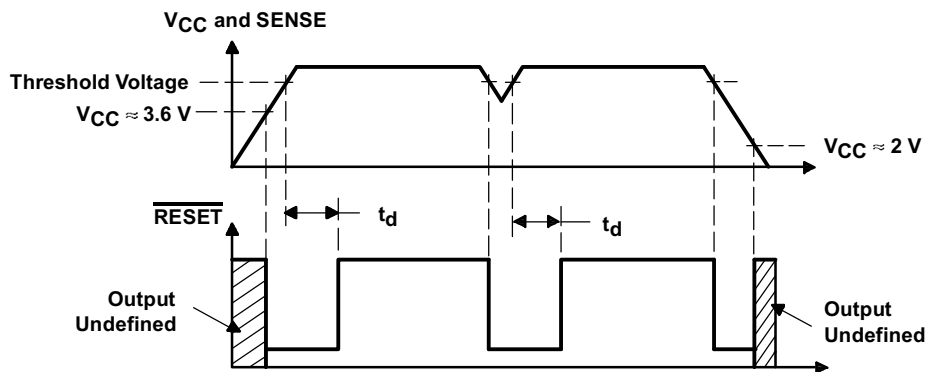
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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	20 V
Input voltage range, V_I, $\overline{RESIN}$	–0.3 V to 20 V
Input voltage range, V_I, SENSE: TL7702A (see Note 2)	–0.3 V to 6 V
TL7705A	–0.3 V to 20 V
TL7709A	–0.3 V to 20 V
TL7712A, TL7715A	–0.3 V to 20 V
High-level output current, I_{OH}, $\overline{RESET}$	–30 mA
Low-level output current, I_{OL}, $\overline{RESET}$	30 mA
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package	97°C/W
P package	127°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} – 1 V or 6 V, whichever is less.
3. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
4. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
High-level input voltage at $\overline{RESIN}$, V_{IH}		2		V
Low-level input voltage at $\overline{RESIN}$, V_{IL}			0.6	V
Input voltage, SENSE, V_I	TL7702A	0	See Note 2	V
	TL7705A	0	10	
	TL7709A	0	15	
	TL7712A	0	20	
	TL7715A	0	20	
High-level output current, RESET, I_{OH}			–16	mA
Low-level output current, $\overline{RESET}$, I_{OL}			16	mA
Timing capacitor, C_T			10	µF
Operating free-air temperature range, T_A	TL77xxAC	0	70	°C
	TL77xxAI	–40	85	

NOTE 2: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} – 1 V or 6 V, whichever is less.

![Texas Instruments logo]

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL77xxAC TL77xxAI			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		I_{OH} = −16 mA	V_{CC}−1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage		T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702A	T_A = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11	
		TL7715A		13.2	13.5	13.8	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702A	T_A = 25°C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 2.4 V to V_{CC}			20	μA
			V_I = 0.4 V			−100	
		SENSE TL7702A	$V_{ref} < V_I < V_{CC}$ − 1.5 V		0.5	2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V			50	μA
I_{OL}	Low-level output current, RESET		V_O = 0			−50	μA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

† All electrical characteristics are measured with 0.1-μF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡	TL77xxAC TL77xxAI			UNIT
				MIN	TYP	MAX	
	Output pulse duration		C_T = 0.1 μF	0.65	1.2	2.6	μs
	Input pulse duration at $\overline{\text{RESIN}}$			0.4			μs
$t_{w(S)}$	Pulse duration at SENSE input to switch outputs		V_{IH} = V_{IT-} +200 mV, V_{IL} = V_{IT-} −200 mV	2			μs
t_{pd}	Propagation delay time, $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$		V_{CC} = 5 V			1	μs
t_r	Rise time	RESET	V_{CC} = 5 V, See Note 5			0.2	μs
		$\overline{\text{RESET}}$				3.5	
t_f	Fall time	RESET	V_{CC} = 5 V, See Note 5			3.5	μs
		$\overline{\text{RESET}}$				0.2	

‡ All switching characteristics are measured with 0.1-μF capacitors connected at REF and V_{CC} to GND.
NOTE 5:   The rise and fall times are measured with a 4.7-kΩ load resistor at RESET and $\overline{\text{RESET}}$.

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electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL77xxAY MIN	TL77xxAY TYP	TL77xxAY MAX	UNIT
V_{ref} Reference voltage				2.53		V
V_{IT-} Negative-going input threshold voltage, SENSE	TL7702A			2.53		V
	TL7705A			4.55		
	TL7709A			7.6		
	TL7712A			10.8		
	TL7715A			13.5		
V_{hys} Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702A			10		mV
	TL7705A			15		
	TL7709A			20		
	TL7712A			35		
	TL7715A			45		
I_I Input current, SENSE	TL7702A	$V_{ref} < V_I < V_{CC} - 1.5$ V		0.5		µA
I_{CC} Supply current		All inputs and outputs open		1.8		mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TL77xxAY MIN	TL77xxAY TYP	TL77xxAY MAX	UNIT
t_d Output pulse time delay	C_T = 0.1 µF		1.2		µs

‡ All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.

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PARAMETER MEASUREMENT INFORMATION

Figure 1. Voltage Waveforms

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TYPICAL CHARACTERISTICS†

ASSERTION TIME
vs
LOAD RESISTANCE

$V_{CC} = 5\ V$
$C_T = 0.1\ \mu F$
$C_L = 10\ pF$
$T_A = 25°C$

RESET t_r

$\overline{RESET}$ t_f

t – Assertion Time – ns

R_L – Load Resistance – kΩ

Figure 2

DEASSERTION TIME
vs
LOAD RESISTANCE

$V_{CC} = 5\ V$
$C_T = 0.1\ \mu F$
$C_L = 10\ pF$
$T_A = 25°C$

RESET t_f

$\overline{RESET}$ t_r

t – Deassertion Time – μ s

R_L – Load Resistance – kΩ

Figure 3

ASSERTION TIME
vs
LOAD CAPACITANCE

$V_{CC} = 5\ V$
$C_T = 0.1\ \mu F$
$R_L = 4.7\ k\Omega$
$T_A = 25°C$

RESET t_r

$\overline{RESET}$ t_f

t – Assertion Time – ns

C_L – Load Capacitance – pF

Figure 4

DEASSERTION TIME
vs
LOAD CAPACITANCE

$V_{CC} = 5\ V$
$C_T = 0.1\ \mu F$
$R_L = 4.7\ k\Omega$
$T_A = 25°C$

RESET t_f

$\overline{RESET}$ t_r

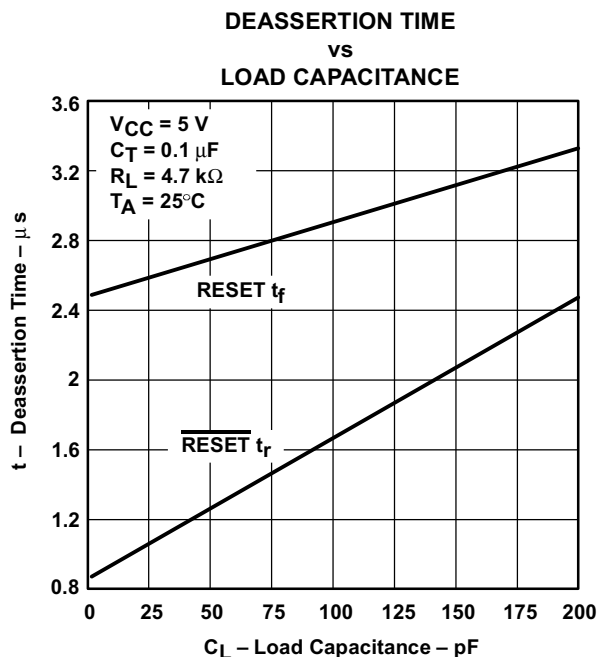t – Deassertion Time – μ s

C_L – Load Capacitance – pF
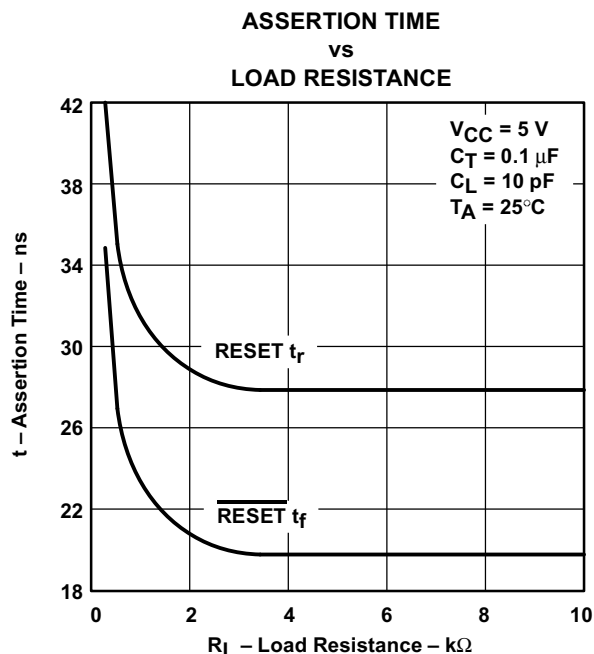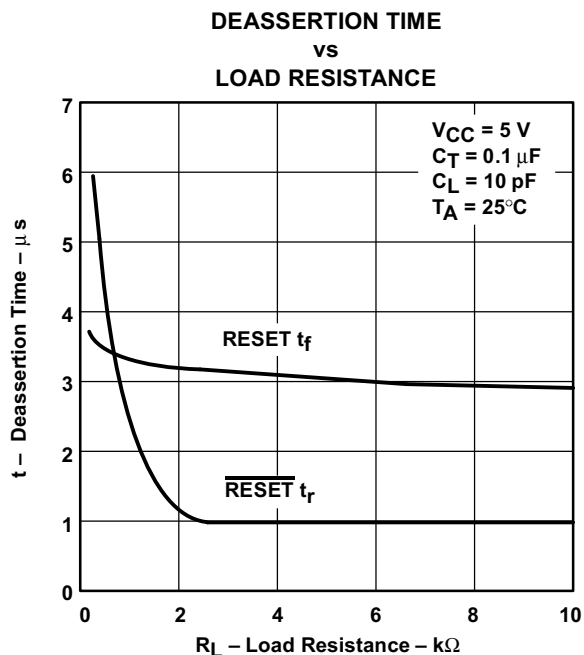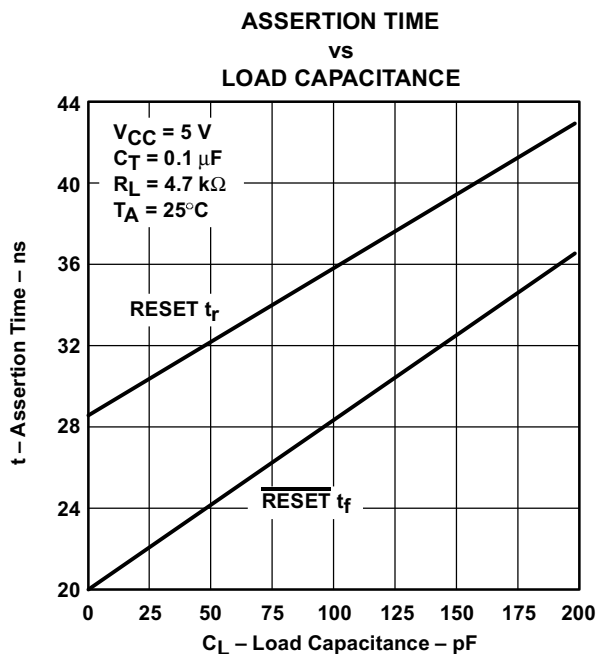
Figure 5

† For proper operation, both RESET and $\overline{RESET}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

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APPLICATION INFORMATION

$$C_T(F) = \frac{t_{d(s)}}{1.3 \times 10^4}$$
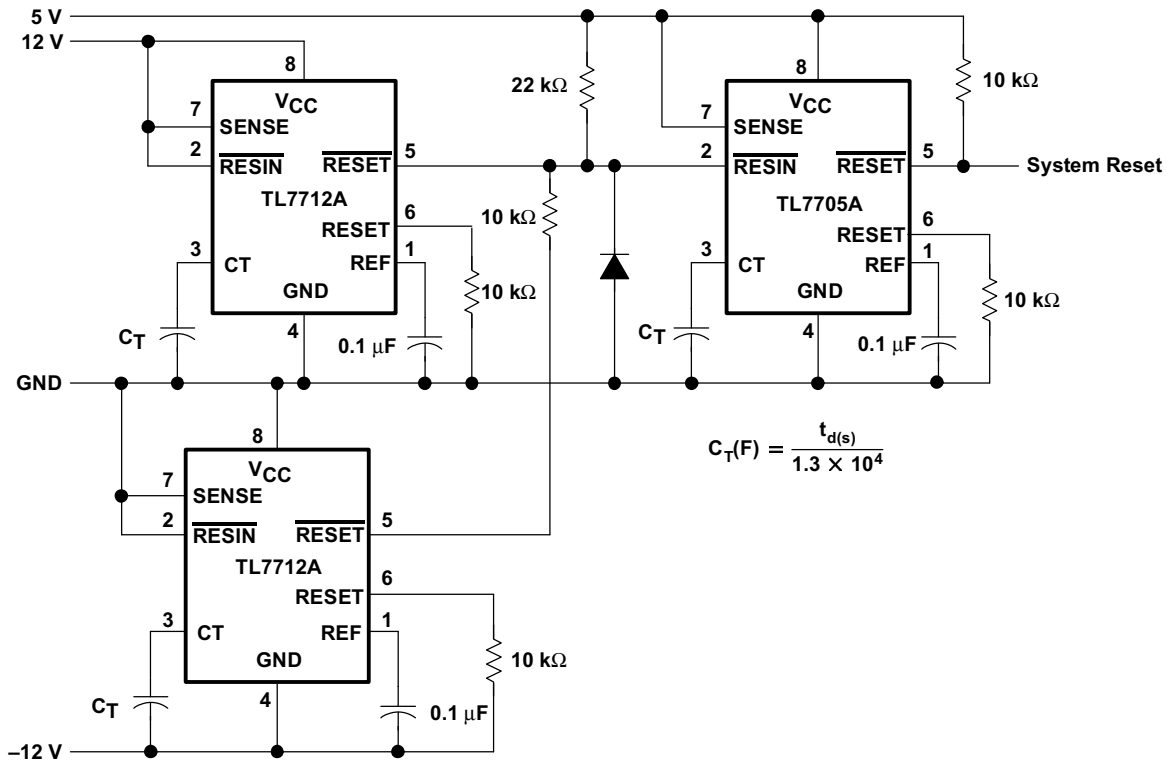
Figure 6. Multiple Power-Supply System Reset Generation

$$C_T(F) = \frac{t_{d(s)}}{1.3 \times 10^4}$$
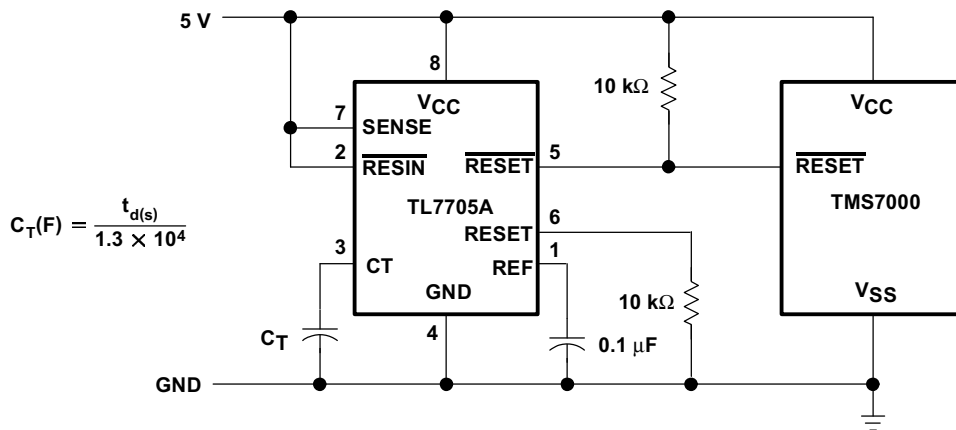
Figure 7. Reset Controller for TMS7000 System

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APPLICATION INFORMATION
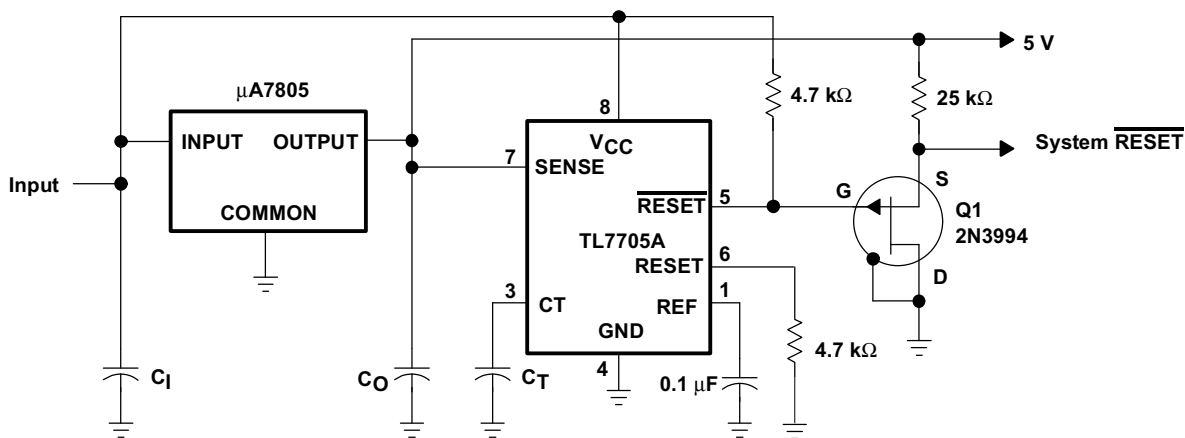
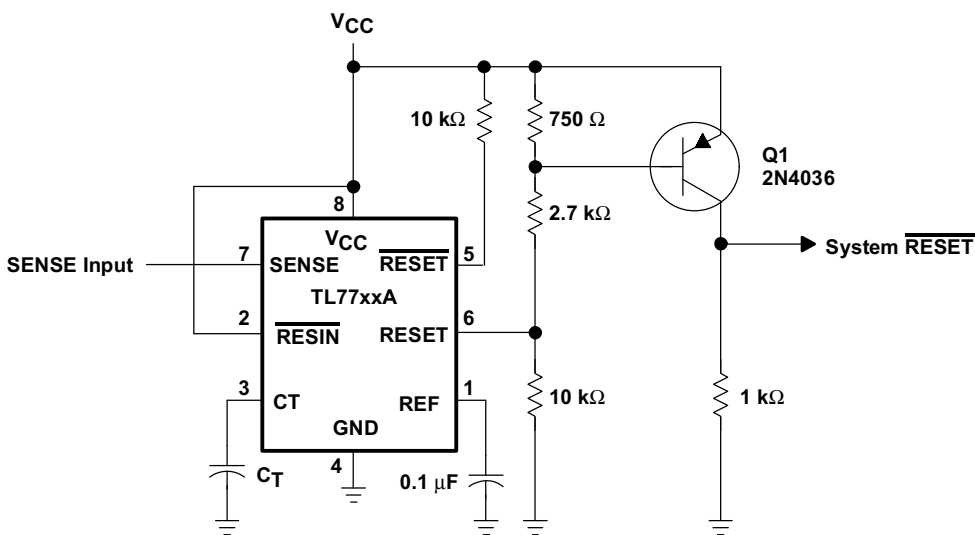**Figure 8. Eliminating Undefined States Using a P-Channel JFET**

Figure 9. Eliminating Undefined States Using a pnp Transistor

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