RELEASE 1.22, OCTOBER 1990

- Two Arrays with up to 2000 Usable Equivalent Gates
- TI Action Logic™ System (TI ALS) Software Provides Resident TPC10 Series Library for:
  - *ViewLogic* ®
  - Mentor
  - OrCAD/SDT III ®
  - Valid Logic
- Flip-Flop Toggle Rates up to 70 MHz
- Reliable Antifuse Interconnect
- Built-in Clock Distribution Network
- 1.2-µm Silicon-Gate CMOS Technology
- Desktop Action Logic System Creates Design Files for:
  - I/O Pin Assignment
  - Design Validation
  - Place and Route
  - Circuit Timing Analysis
  - Array Antifuse Programming
  - Test and Debug
- Fully Supported by TI ASIC Design Centers

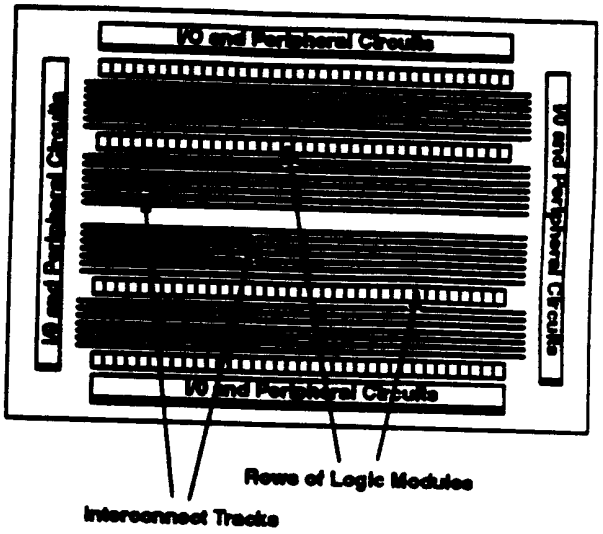

Figure 1. TPC10 Series FPGA Die Architecture

description

The Texas Instruments TPC10 Series is comprised of two field-programmable gate arrays (FPGAs). The TPC1010A and TPC1020A FPGAs are fabricated using TI's 1.2-µm silicon-gate CMOS process. The process features two levels of copper-doped-aluminum metallization, and polysilicon gate, source, and drain elements to reduce internal resistance and enhance performance. The two field-programmable arrays, with their cell and bond-pad configurations and production packages, are shown in Table 1. Typical die architecture is illustrated in Figure 1.

These field-programmable devices combine gate-array flexibility with desktop programmability. This combination allows the ASIC designer to avoid fabrication cycle times and nonrecurring engineering charges associated with conventional mask-programmed gate arrays. The FPGAs are unique in that the arrays are tested, fabricated, and shipped to the user for programmation. The FPGA contains user-configurable inputs, outputs, logic modules, and minimum-skew clock driver with hardwired distribution network. The FPGA also includes on-chip diagnostic probe capabilities and security fuses to protect the proprietary design.

Table 1. TPC10 Series Complexity and Packaging Summary

FPGA TYPE	LOGIC MODULES	EQUIVALENT 2-INPUT NAND GATES	PRODUCTION PACKAGES			
			44-PIN	68-PIN	84-PIN	
			PLCC	PLCC	PLCC	PGA
TPC1010A	295	1200	√	√	NA	√
TPC1020A	547	2000	√	√	√	√
SIGNAL BOND PADS†			34	57	69	57/69

† Includes diagnostic pins.

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action logic system and Activator ™

TPC10 Series FPGAs are supported by TI's Action Logic System Software and Activator programming hardware. The combination facilitates logic design and FPGA programming on popular CAE workstations with a minimum of redirected effort. The Action Logic System (ALS) interfaces to the resident CAE system providing a complete library of TPC10 Series functions. The ALS system then extends the workstation capability to include automatic place and route, timing verification, and FPGA device programming. The TI Action Logic System and Activator are available for ViewLogic or OrCAD(SDT III) 386-based PC systems, Mentor-equipped Apollo workstations, and ViewLogic- or Valid-equipped Sun3 or Sun4 workstations. Table 2 displays the Action Logic System configurations.

library functions

The TPC10 Series FPGA library includes basic gates, Booleans, latches, flip-flops, multiplexers, adder slices, and MSI-complexity software macros. Of the 275 macros offered, 224 are hardwired and 51 are software macros. The hardwired macros provide a broad selection of predesigned, fully characterized functions. The software macros provide popular MSI functions that can be called into the design. Additional user-defined software macros can be created using the TPC10 library macros. Library release 3.3 contains the following classes of macros:

- 98 Primitive Gates, Booleans, and Buffers
- 6 CMOS, TTL, and Clock Buffer Inputs and Totem-Pole, 3-State, and I/O Output Buffers
- 16 Adders and Multiplexers
- 57 D-Type Flip-Flops
- 12 J-$\overline{K}$ Flip-Flops
- 35 Latches
- 51 MSI Complexity Software Macros

design flow

Custom logic functions, designed using an engineering workstation in conjunction with TI's TPC10 Series FPGA library, can be simulated and verified prior to creating the Action Logic System design database and programming files. Figure 2 provides an overview of the design flow.

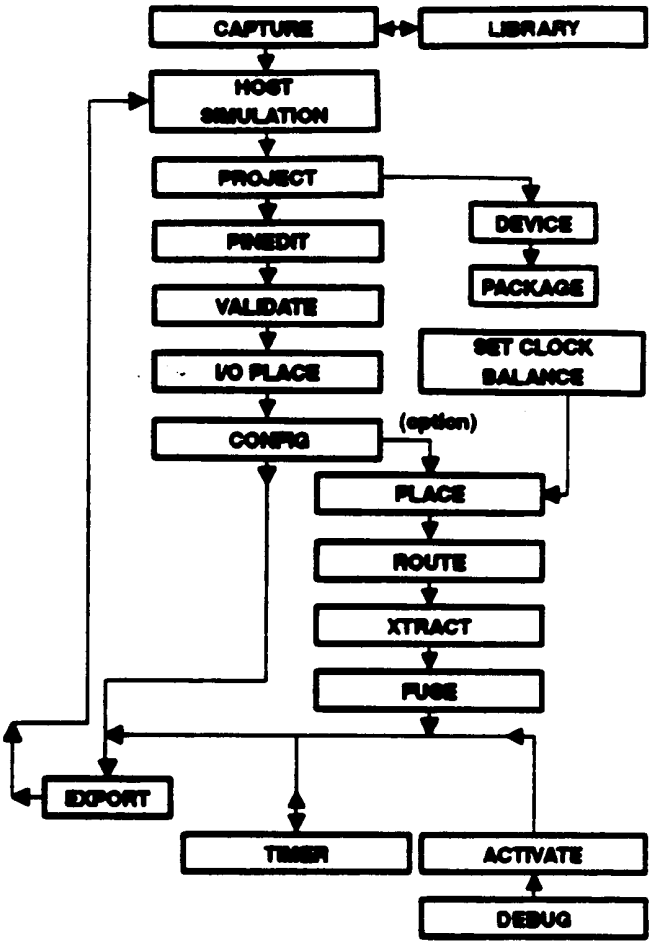

Figure 2. Design Flow

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Table 2. Action Logic System Configurations

HARDWARE PLATFORM	CAE HOST ENVIRONMENT	TI PART NUMBER	SOFTWARE SUPPLIED		HARDWARE SUPPLIED	
			CAPTURE	LIBRARY	PROGRAM	TEST/DEBUG
PC 386-AT	ViewLogic/OrCAD	TPC–ALS-110	Viewdraw	ViewLogic/OrCAD	ACT1	√
PC 386-AT	ViewLogic/OrCAD	TPC–ALS-113	Viewdraw	ViewLogic/OrCAD	ACT1	
Apollo	Mentor	TPC–ALS-031		Mentor	ACT1	√
Apollo	Mentor	TPC–ALS-035		Mentor		
Sun3	Valid	TPC–ALS-041-S3		Valid	ACT1	√
Sun4	Valid	TPC–ALS-041-S4		Valid	ACT1	√
Sun3	Valid	TPC–ALS-045-S3		Valid		
Sun4	Valid	TPC–ALS-045-S4		Valid		
Sun3	ViewLogic	TPC–ALS-051-S3		ViewLogic	ACT1	√
Sun4	ViewLogic	TPC–ALS-051-S4		ViewLogic	ACT1	√
Sun3	ViewLogic	TPC–ALS-055-S3		ViewLogic		
Sun4	ViewLogic	TPC–ALS-055-S4		ViewLogic		

NOTE: 1. Simulation and other software and hardware options are available. Consult your local salesperson for details.

ARCHITECTURE

device organization

Each FPGA consists of a matrix of logic modules arranged in rows separated by channels containing interconnect tracks. The matrix is surrounded with peripheral inputs, outputs, I/Os, and diagnostic circuits. A partial view of the FPGA logic modules and examples of interconnections are illustrated in Figure 3.

logic module

Each core logic module has the equivalent complexity of four 2-input NAND gates. The module is an 8-input, 1-output gate cluster that can implement hardwired primitive gates, Booleans, latches, flip-flops, multiplexers, half or full adder slices, or multiplexed-input flip-flops. The ALS library contains a full spectrum of 2-, 3-, and 4-input AND, NAND, OR, and NOR gate macros covering all derivatives of true and/or complement input combinations. Similar modular implementations, covering the spectrum of true and/or complement input combinations, are included for each functional category of macros in the library. The macros are captured, simulated, placed, analyzed, and programmed using the workstation TPC10 design library.

Interconnect tracks

The channeled interconnect tracks consist of isolated metal segments that can be connected by addressing and programming antifuses. Each channel has a minimum of 22 signal tracks and each array has about 340 antifuses per logic module. This produces a network capable of interconnecting up to 90 percent of the equivalent gates. Based on the placement of macros, the programming process selects and activates antifuses that both create the logic module macros and I/Os, and interconnect the entire array.

I/O buffers

Each I/O pin is configurable as an input or an output that can be defined as totem-pole, 3-state, or bidirectional I/O. Inputs can be driven by CMOS or TTL levels and output levels are compatible with standard CMOS and TTL specifications. Outputs sink or source a current of 4 mA at TTL output levels. See the dc characteristics for additional I/O buffer specifications. The I/Os can be manually assigned to any available package pin, or the ALS software can place the I/Os in the optimum configuration.

extended output sink-current operation

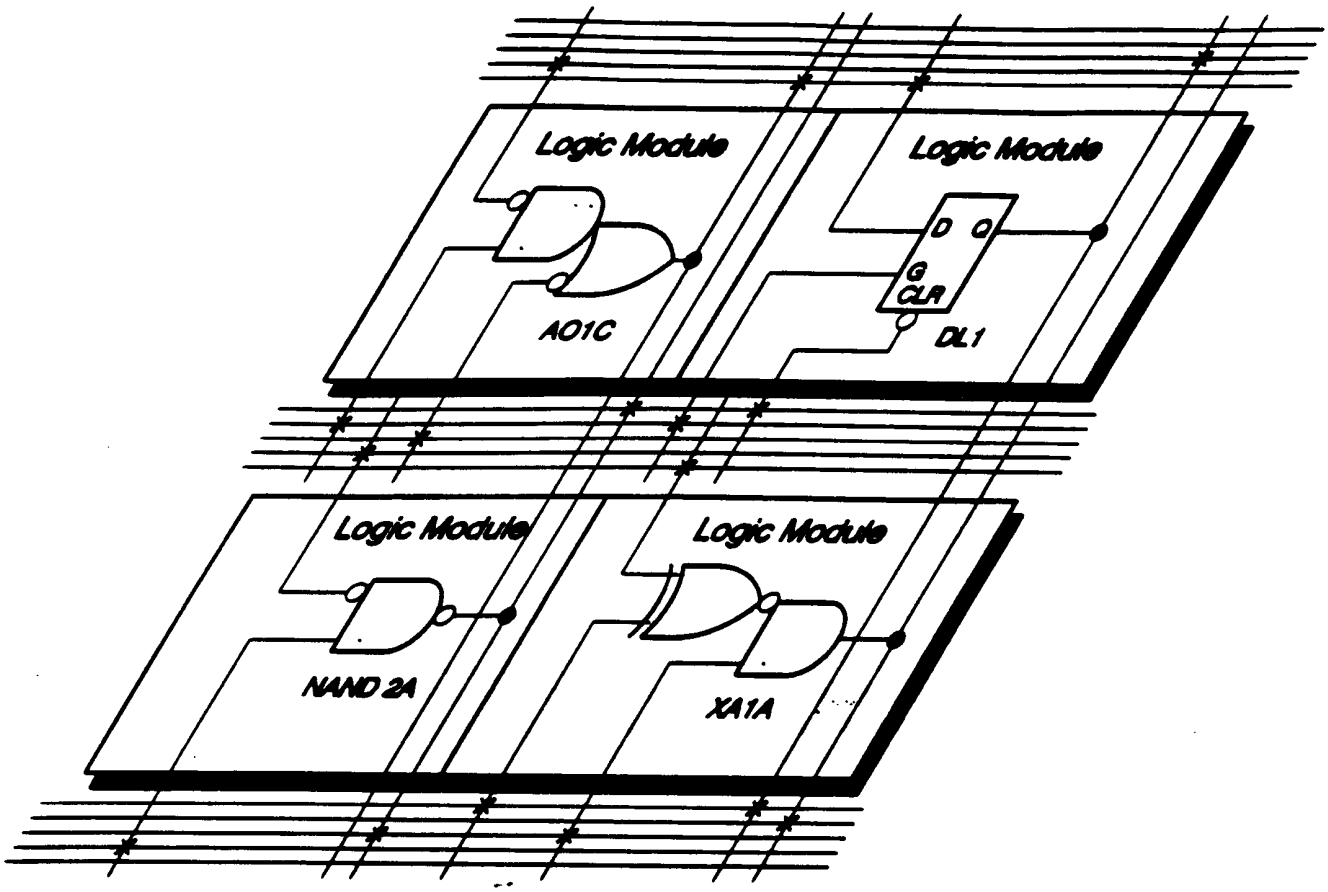

Figure 3. Partial View of TPC10 Series Interconnection Capability

diagnostic probe pins

TPC10 Series devices have two independent diagnostic probe pins. The pins allow the user to observe any two internal output signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on an oscilloscope, logic analyzer, or with the workstation diagnostics. The probe pins can also be used as user-defined I/Os, depending on the level of the mode control pin. When configured as user-defined I/Os, the pins have the same characteristics as other I/O pins.

security fuses

The TPC10 Series security fuses can be used to permanently disable further diagnostics, and testing. After the security fuses are programmed, access to the architecture is not available. This makes the FPGA design difficult to copy.

FPGA ARRAY PERFORMANCE

logic module size

A mask-programmed gate array cell with four transistors usually implements only one logic level. The TPC10 Series array logic module is more complex and typically implements the equivalent of a mask-programmed gate array macro that contains multiple logic levels within a single module. This reduces intercell wiring and associated RC delays. In effect, the TPC10 logic module implements the equivalent of a net compression that enhances performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . – 0.5 V to 7 V
Supply voltage, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage, V_I . . . . . – 0.5 to V_{CC} + 0.5 V
Output voltage, V_O . . . . . – 0.5 to V_{CC} + 0.5 V
Input clamp current‡, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current§, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 20 mA
Continuous output current§, (V_O = 0 to V_{CC}) . . . . . ± 25 mA
Operating free-air temperature: Military temperature range (M) . . . . . – 55°C to 125°C
Industrial temperature range (I) . . . . . – 40°C to 85°C
Commercial temperature range: (C) . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Applies for input and bidirectional buffers

§ Applies for bidirectional and output buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Military	4.5	5	5.5	V
		Industrial	4.5	5	5.5	
		Commercial	4.75	5	5.25	
V_{PP}	Program pin voltage (while not programming)		V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage		2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		– 0.3		0.8	V
T_A	Operating temperature	Military range	– 55		125	°C
		Industrial range	– 40		85	
		Commercial range	0		70	

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			−40°C to 85°C			0°C to 70°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage (See Note 2)	I_{OH} = −4 mA							3.84			V
		I_{OH} = −3.2 mA	3.7			3.7						
V_{OL}	Low-level output voltage (See Note 2)	I_{OL} = 4 mA			0.4			0.4			0.33	V
I_I	Input current	$V_I = V_{CC}$ or 0			± 10			± 10			± 10	μA
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			± 10			± 10			± 10	μA
I_{OS}	Output short-circuit current (see Note 3)	V_O = 0	20		140	20		140	20		140	mA
		$V_O = V_{CC}$	−10		−100	−10		−100	−10		−100	
I_{CC}	Standby supply current	$V_I = V_{CC}$ or 0, Outputs are open		3	25		3	20		3	10	mA
C_{io}	Input or output capacitance (See Note 4)	V_O = 0, f = 1 MHz		7			7			7		pF

NOTES: 2. These limits apply when all other outputs are open.
3. An unloaded logic module propagation delay time is 4 ns. All delays shown include the module delay time and statistical estimates for wiring delays based on 85% to 95% FPGA logic module utilization.
4. These limits apply for each user I/O pin.

TPC10 Series devices are capable of driving larger sink current loads by derating the low level output voltage to 0.5 V. The derating factors for commercial, industrial, and military devices are illustrated in Figure 4. The commercial devices are derated for up to 8 mA of sink current, and industrial and military devices are derated for up to 6 mA of sink current.

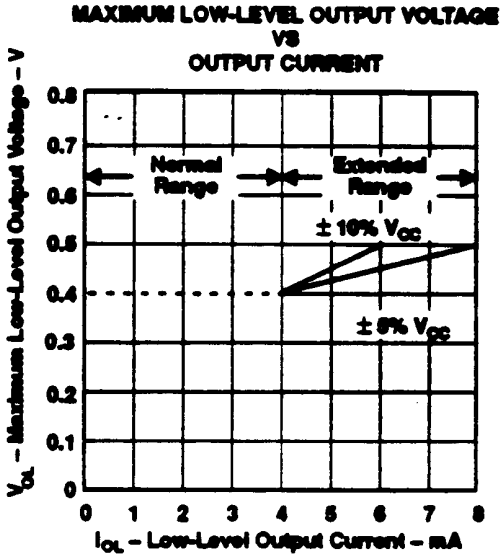

Figure 4. Low-Level Output Voltage Derating Factor

slow input transition (rise and fall) times

Slow signal transitions are a condition which commonly occur, even in today's high performance systems. A typical example is the signal degradation encountered with signals coming off of a highly capacitive bus. These slow signal transitions can cause undesireable results when traveling through the threshold region of a CMOS input. Texas Instruments recommends that input signal transitions be limited to 500 ns or less to ensure device integrity.

switching characteristics

The following tables summarize switching characteristics of various classes of TPC10 Series logic module hardwired macros. An unloaded logic module propagation delay time is 4 ns. All other delays shown include the module delay time and statistical estimates for wiring delays based on 85% to 95% FPGA logic module utilization. Module utilization above 95% can result in performance degradation. Actual delay values are determined after place-and-route is accomplished using the TI Action Logic System. TI's ALS provides for assigning criticality to nets, automatic balancing of clock buffer loads, and utilizing long horizontal or vertical nets for connecting noncritical functions. For specific timing parameters pertaining to a hardwired logic module, refer to the individual macro library specification.

TI's Action Logic System provides a capability to assign one of four levels of criticality to logic module output nets. The switching characteristics reflect the delay time differences for nets with criticality and without criticality assigned. Nets assigned as critical will be limited to a fanout of 6 loads by TI's ALS. Clock load balancing, selectable by the designer, can be specified as moderate, strong, or very strong to control clock skew.

worst-case delay time

Unlike mask-programmed gate arrays, performance variations of TPC10 Series arrays due to voltage and temperature changes are due primarily to the changes in the active elements. As a result, the total delay time factor from typical to worst case for a TPC10 Series array is only 1.18 to 1 compared to 2 to 1 for a mask-programmed gate array. Typical macro symbols and voltage waveform characteristics are illustrated in Figure 5. Voltage and temperature delay time factors are shown in Figure 6.

delay time curves

Logic module and storage element delay factors are shown in Table 3. The delay factors may be used in conjuction with the delay values shown on pages 9 and 10 for estimating performance. Temperature and voltage variations are measured according to the curves in the graphs shown in Figure 6. The ALS timing analyzer can be used to provide actual post-layout timing specifications for each circuit implementation.

Table 3. Worst-Case Delay Time Factors

DEVICES	SUPPLY VOLTAGE		TEMPERATURE		TOTAL FACTOR
	VALUE	FACTOR	VALUE	FACTOR	
Commercial (0°C to 70°C)	4.75 V	1.04	70°C	1.14	1.18
Industrial (– 40°C to 85°C)	4.75 V	1.1	85°C	1.17	1.27
Military (– 55°C to 125°C)	4.75 V	1.1	125°C	1.28	1.38

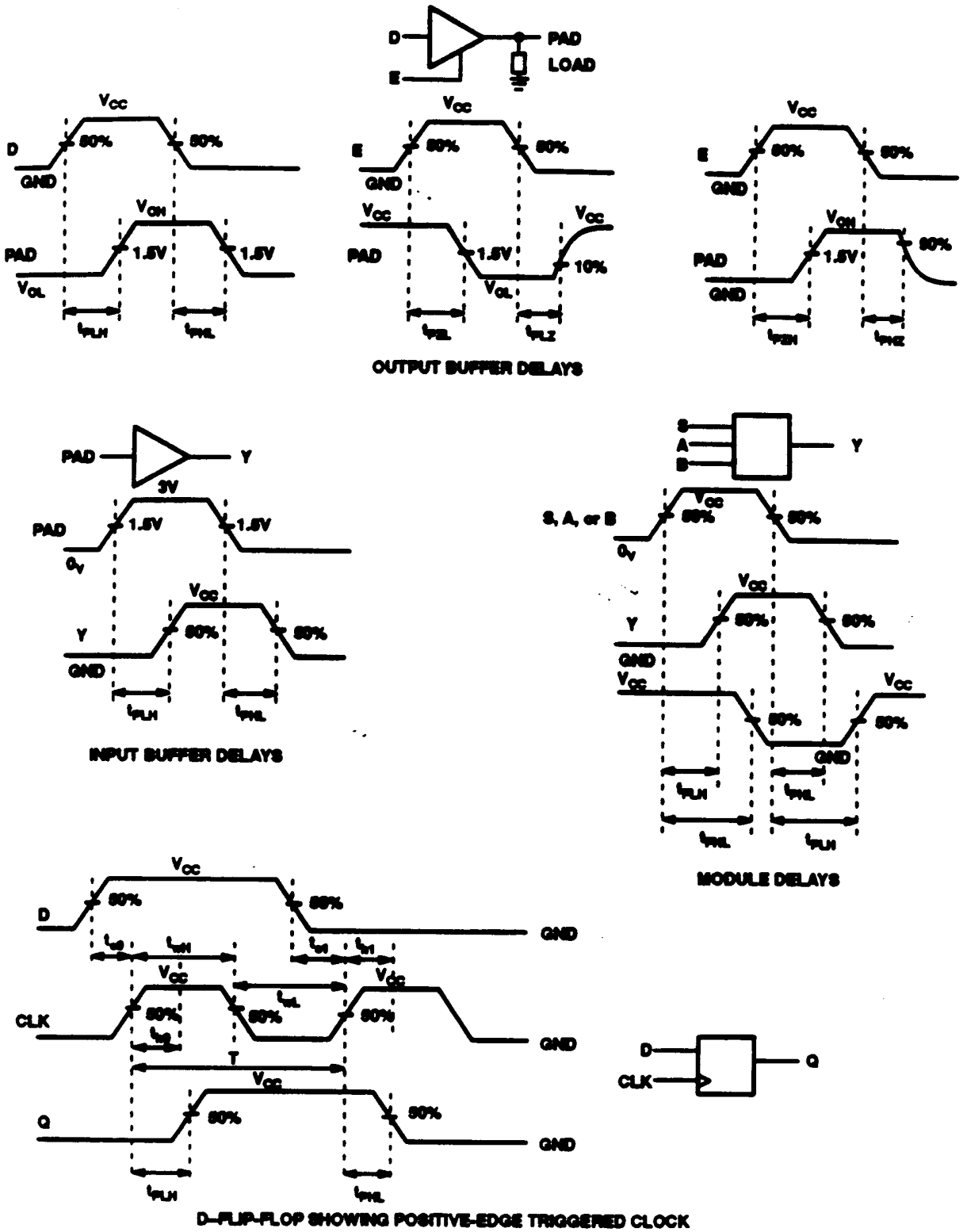

Figure 5. Voltage Waveforms

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timing requirements over recommended ranges of supply voltage and operating free air temperature

				MIN	MAX	UNIT
f_{clock}	Internal toggle frequency				70	MHz
t_w	Pulse duration	CLK, PRE, or CLR		10		ns
t_{su}	Setup time (flip-flop)	All synchronous inputs before clock transition		5		ns
t_{su}	Setup time (latch)	All synchronous inputs before clock transition	fanout = 1	4.6		ns
			fanout = 2	5		
			fanout = 3	5.4		
			fanout > 3	5.8		
t_h	Hold time (flip-flop or latch)	All synchronous inputs after clock transition		0		ns

TIMING REQUIREMENTS

single-level logic module hardwired macro switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	OUTPUT-NET CRITICALITY	DELAY TIME					UNIT
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{pd}	Critical	7	7.5	8	11	See Note 6	ns
t_{pd}	Not critical	8.2	8.7	10	11.2	14	ns

NOTE: 5. An unloaded logic module propagation delay time is 4 ns. All other delays shown include the module delay time and statistical estimates for wiring delays based on 85% to 95% FPGA logic module utilization.

2-level logic module hardwired macro switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	OUTPUT-NET CRITICALITY	DELAY TIME					UNIT
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{pd}	Critical	12	12.5	13	16	See Note 6	ns
t_{pd}	Not critical	13.2	13.7	15	16.2	19	ns

flip-flop and latch (hardwired macro) switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	OUTPUT-NET CRITICALITY	DELAY TIME					UNIT
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{pd}	Critical	7	7.5	8	11	See Note 6	ns
t_{pd}	Not critical	8.2	8.7	10	11.2	14	ns

long net switching characteristics, V_{CC} = 5 V, T_A = 25°C

Long nets include long horizontal and vertical routing resources used for noncritical signals and interconnecting logic macros separated by large distances. Long nets are used by the autorouter when no other means exists to complete the interconnection. Delays due to the use of long nets range from 15 to 30 ns. Typically less than one percent of all nets in a design require the use of a long net.

PARAMETER	LONG NET	DELAY TIME	UNIT
t_{pd}	Horizontal or vertical	35	ns

input-buffer and bidirectional-input buffer switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	DELAY TIME					UNIT
			FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{PHL}	Pad	Y	9	9.9	11.6	13.9	18.6	ns
t_{PLH}			7.7	8.4	10	10.9	16.1	ns

NOTE: 6. Critical nets are limited to a fanout of 6 loads.

output-buffer switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	DELAY TIME		UNIT
				DRIVING CMOS LOADS	DRIVING TTL LOADS	
t_{PHL}	D	Pad	C_L = 50 pF	5.1	6.4	ns
t_{PLH}				9.4	7.4	
Δt_{PHL}	D	Pad		0.04	0.06	ns/pF
Δt_{PLH}				0.09	0.05	

The BIBUF macro's output section exhibits the same delays as the OUTBUF macro. The delta numbers can be extrapolated down to 15 pF minimum.

Example: Delay for an OUTBUF output buffer driving a 100 pF TTL load.

T_{PHL} = 6.4 + (0.06 • (100 – 50) = 6.4 + 3.0 = 9.4 ns

T_{PLH} = 7.4 + (0.05 • (100 – 50) = 7.4 + 2.5 = 9.9 ns

three state and bidirectional output-buffer switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	DELAY TIME		UNIT
				DRIVING CMOS LOADS	DRIVING TTL LOADS	
t_{PHL}	D	Pad	C_L = 50 pF	5.1	6.4	ns
t_{PLH}				9.4	7.4	
Δt_{PHL}	D	Pad		0.04	0.06	ns/pF
Δt_{PLH}				0.09	0.05	
t_{PHZ}	E	Pad		6.7	4.4	ns
t_{PZH}				8.4	6.3	
Δt_{PHZ}	E	Pad		0.10	0.06	ns/pF
Δt_{PZH}				0.09	0.05	
t_{PLZ}	E	Pad		8.9	6.7	ns
t_{PZL}				6.4	7.7	
Δt_{PLZ}	E	Pad		0.09	0.05	ns/pF
Δt_{PZL}				0.04	0.05	

clock-buffer switching characteristics, V_{CC} = 5 V, T_A = 25°C (See Note 7)

PARAMETER	FROM	TO	TEST CONDITIONS	DELAY TIME			UNIT
				MIN	TYP	MAX	
t_{PHL}	Pad	Y	Any number of CLK or G inputs	12	16	25	ns
t_{PLH}				11	15	25	

NOTE: 7. The TI ALS software provides user-selectable options for choosing four levels of automatic clock load balancing. There is no limit to the number of loads that may be connected to the clock buffer (CLKBUF) macro.

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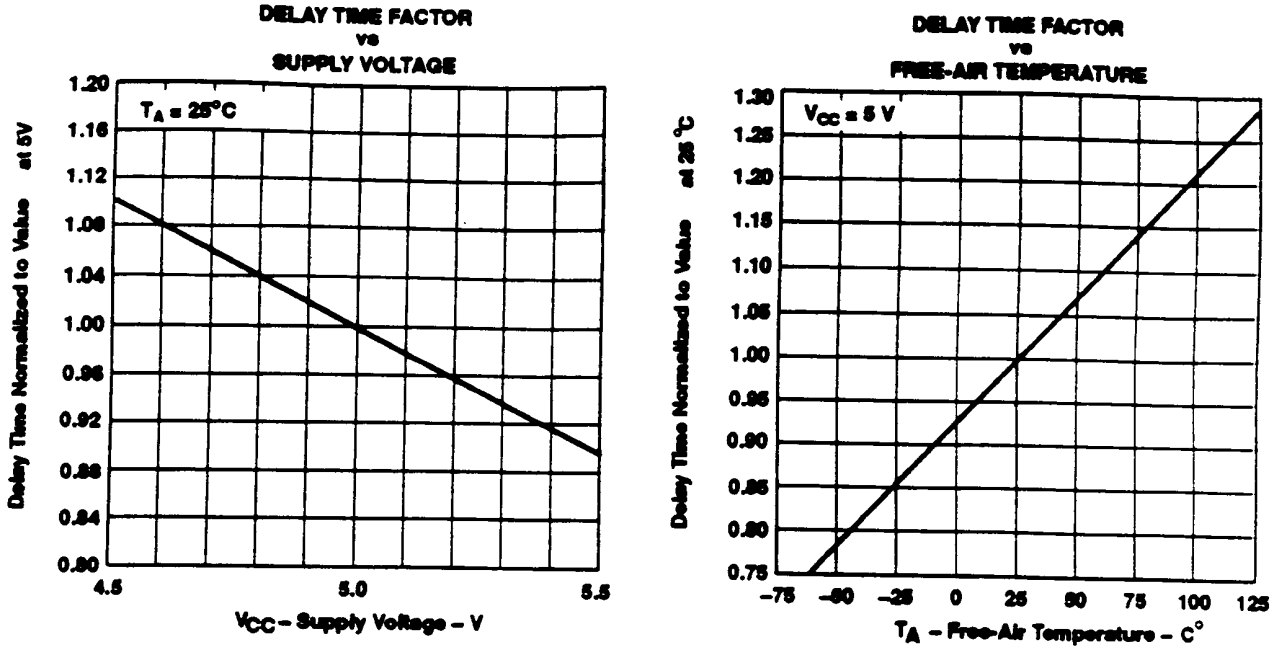

Figure 6. Delay Time Factor vs Supply Voltage and Temperature

dynamic power calculations

The formula for calculating typical dynamic die power consumption in mW is:

Total Die Power = 0.41N • f1 + 0.17M • f2 + 1.62P • f3

where:

f1 = Average logic module switching rate in MHz
f2 = Average clock pin switching rate in MHz (See Note 8)
f3 = Average I/O switching rate in MHz
M = Number of logic modules connected to the clock pin (See Note 8)
N = Number of logic modules used on the chip (including M)
P = Number of I/Os used with 50 pF load

NOTE: 8. The F2 and M factors can be ignored if the CLKBUF macro is not used.

For example, if an ACT1010 design has 200 logic modules used, 40 of which are connected to the high fan-out clock buffer running at 20 MHz and the rest running at 4 MHz, plus 50 I/Os (25 outputs, 25 inputs) running at an average of 4 MHz, it will dissipate the following amount of power:

Total Die Power = 0.41N • f1 + 0.17M • f2 + 1.62P • f3
= 0.41(200 • 4) + 0.17(40 • 20) + 1.62(25 • 4)
= 626 mW

package selection

The following classes of conventional packages are offered for TPC10 Series FPGAs:

- Plastic leaded chip carrier (PLCC), suffix FN
- Ceramic pin grid array (PGA), suffix PB
- Pin assignments for the TPC10 Series FPGAs are diagrammed in Figures 7 through 10.
- Mechanical outline dimensions are shown in Figures 41 and 42.

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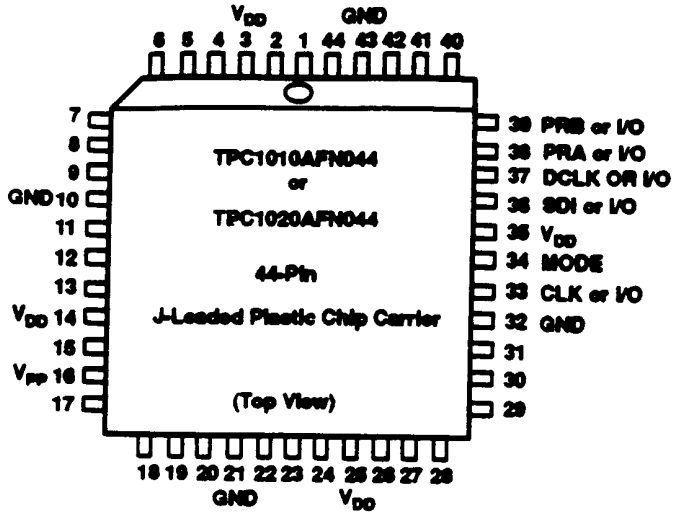

Figure 7. TPC1010A and TPC1020A 44-Pin PLCC Pin Assignment

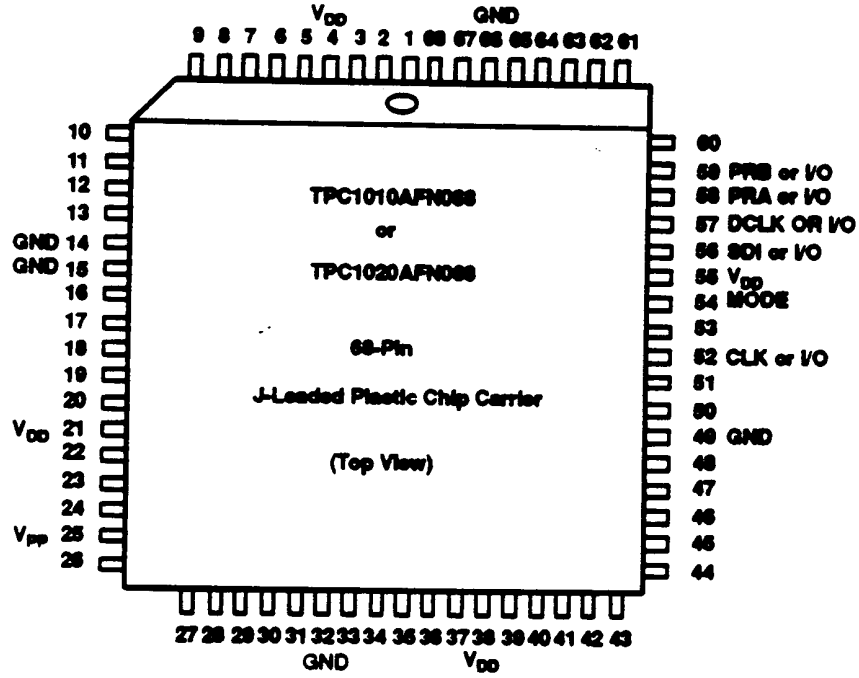

Figure 8. TPC1010A and TPC1020A 68-Pin PLCC Pin Assignment

NOTES: 9. All pins marked GND are ground connections and must be connected to circuit ground.
10. V_{PP} must be terminated to V_{CC} except during programming.
11. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
12. MODE must be terminated to circuit ground except during programming.†
13. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
14. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
15. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10 kΩ (or greater) resistor. They can be tied to ground if not debugging.

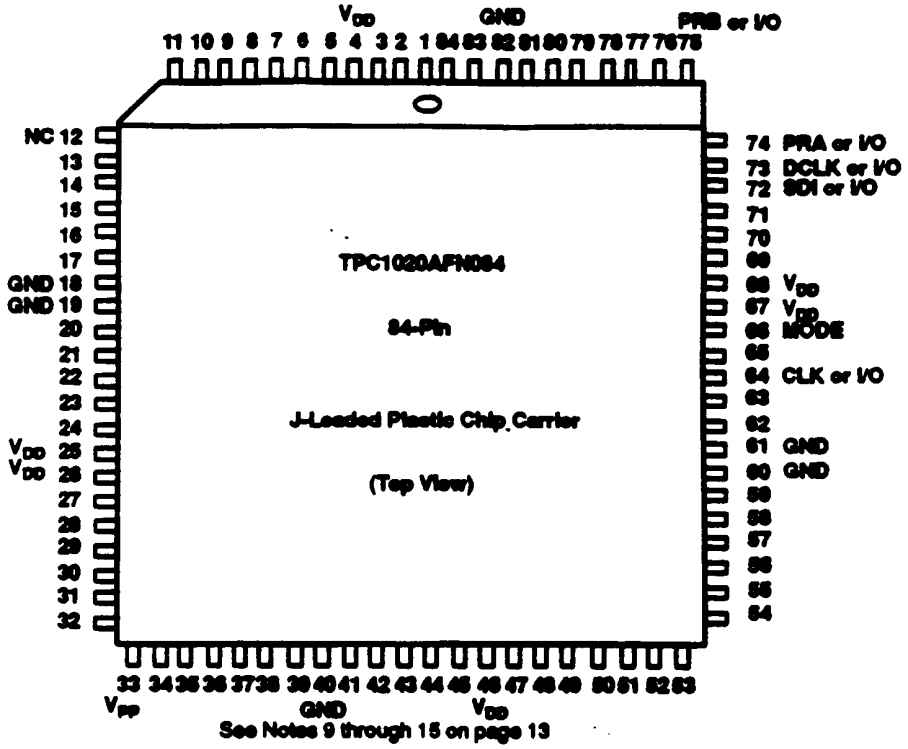

Figure 9. TPC1020A 84-Pin PLCC Pin Assignment

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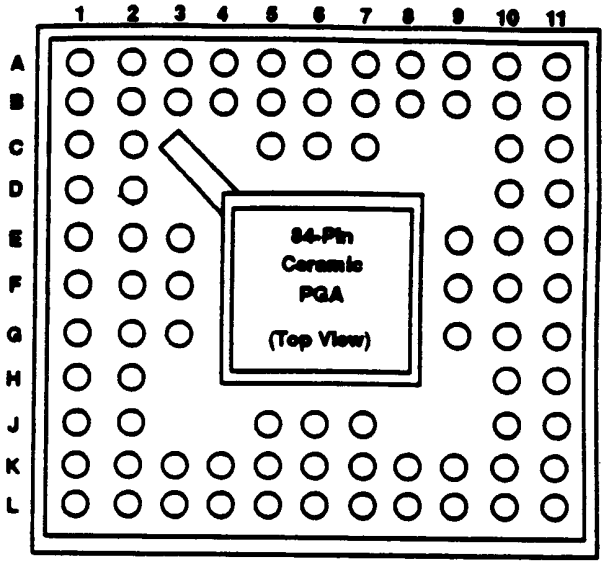


See Notes 9 through 15 on page 13

I/O Pin Assignments for the 84-Pin Ceramic Pin Grid Array Package

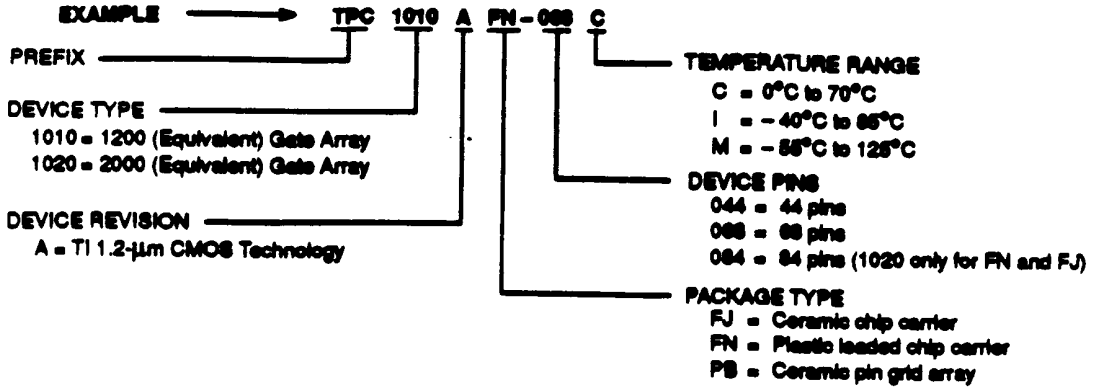
SIGNAL	TPC1010A	TPC1020A
PRA	A11	A11
PRB	B10	B10
MODE	E11	E11
SDI	B11	B11
DCLK	C10	C10
V_{PP}	K2	K2
CLK or I/O	F9	F9
GND	B7, E2, E3, K5, F10, G10	B7, E2, E3, K5, F10, G10
V_{DD}	B5, F1, G2, K7, E9, E10	B5, F1, G2, K7, E9, E10
NC (No Internal Connection)	B1, B2, C1, C2, K1, J2, L1, J10, K10, K11, C11, D10, D11	B2

All other package pins are available for use as I/Os.

Figure 10. TPC1010A and TPC1020A 84-Pin PGA Pin Assignment

ordering information

Various configurations of the TPC1010A and TPC1020A can be ordered using part numbers developed to indicate available versions of the following combinations:



macro library

The TPC10 Series is supported by a macro library of 224 hardwired and 51 software macro functions. The macros range from primitive logic gates to MSI-level complex functions such as counters, decoders, and comparators. The hardwired macro characteristics are provided in the electrical and switching characteristics. The software macros have characteristics similar to the components of the macro but need the place and route data back-annotated into the design to establish actual performance.

The FPGA logic module implements logic functions with inverted inputs as efficiently as noninverted inputs, without an increase in propagation delay. By taking advantage of the various combinations of input polarity, the use of separate inverters can be virtually eliminated.

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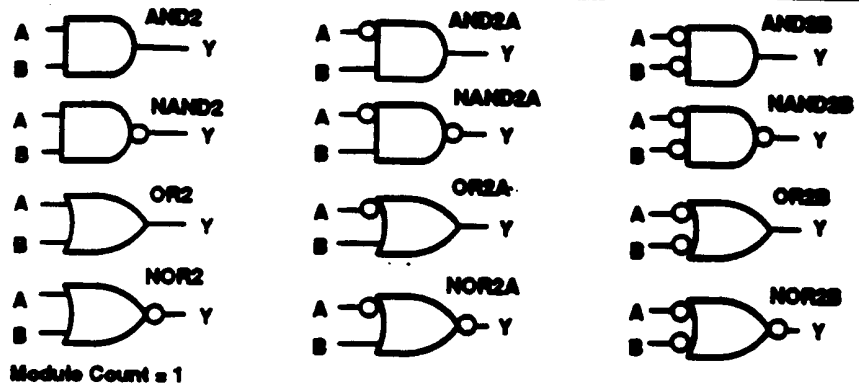
TPC10 SERIES SOFTWARE MACROS

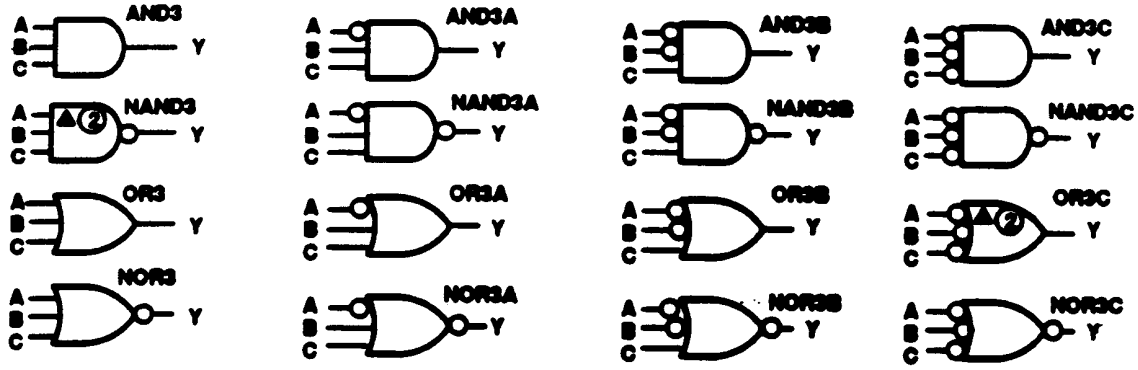
MACRO NAME	DESCRIPTION	MODULE COUNT	LOGIC LEVELS
CNT4A	4-Bit Binary Counter with Preset and Clear	18	4
CNT4B	4-Bit Presettable Binary Counter with Preset and Clear	15	4
DEC2X4	2-Line to 4-Line Decoder	4	1
DEC2X4A	2-Line to 4-Line Inverting Decoder	4	1
DECE2X4	2-Line to 4-Line Decoder with Enable	4	1
DECE2X4A	2-Line to 4-Line Inverting Decoder with Enable	5	1
DEC3X8	3-Line to 8-Line Decoder	8	1
DEC3X8A	3-Line to 8-Line Inverting Decoder	9	1
DECE3X8	3-Line to 8-Line Decoder with Enable	11	2
DECE3X8A	3-Line to 8-Line Inverting Decoder with Enable	11	2
DEC4X16A	4-Line to 16-Line Inverting Decoder	20	2
DLE8	Octal D-Type Latch with Enable	8	1
DLM8	Octal D-Type Latch with Multiplexed Inputs	8	1
DLC8A	Octal D-Type Latch with Clear	8	1
FA1	One-Bit Full Adder	3	3
FADD8	8-Bit Fast Adder	37	4
FADD12	12-Bit Fast Adder	58	5
FADD16	16-Bit Fast Adder	79	5
FADD24	24-Bit Fast Adder	120	6
FADD32	32-Bit Fast Adder	160	7
ICMP4	4-Bit Identity Comparator	5	2
ICMP8	8-Bit Identity Comparator	9	3
MCMPC2	2-Bit Magnitude Comparator with Enables	9	3
MCMPC4	4-Bit Magnitude Comparator with Enables	18	4
MCMPC8	8-Bit Magnitude Comparator with Enables	36	6
MCMP16	16-Bit Magnitude Comparator	93	5
MX8	8-Line to 1-Line Multiplexer	3	2
MX8A	8-Line to 1-Line Inverting Multiplexer	3	2
MX16	16-Line to 1-Line Multiplexer	5	2
REGE8A	Octal Register with Preset and Clear	20	2
REGE8B	Octal Inverting Register with Preset and Clear	20	2
SMULT8	8 x 8 Twos Complement Multiplier	241	–
SREG4A	4-Bit Shift Register with Clear	8	2
SREG8A	8-Bit Shift Register with Clear	18	2
TA138	3-Line to 8-Line Decoder/Demultiplexer	12	2
TA139	2-Line to 4-Line Decoder/Demultiplexer	4	1
TA151	8-Line to 1-Line Multiplexer	5	3
TA153†	4-Line to 1-Line Multiplexer	2	2
TA157†	2-Line to 1-Line Multiplexer	1	1
TA161	Synchronous 4-Bit Counter with Direct Clear	22	3
TA164	8-Bit Parallel-Out Shift Register	18	1
TA169	4-Bit Up/Down Counter	25	6
TA181	4-Bit Arithmetic Logic Unit/Function Generator	37	4
TA194	4-Bit Bidirectional Universal Shift Register	14	1
TA195	4-Bit Parallel-Access Shift Register	11	1
TA269	8-Bit Up/Down Counter	50	8
TA273	Octal D-Type Flip-Flop	18	1
TA280	9-Bit Odd/Even Parity Generator/Checker	9	4
TA377	Octal D-Type Flip-Flop with Clock Enable	16	1
UDCNT4A	4-Bit Up/Down Counter with Sync Load and Carry	24	6
UART	Universal Asynchronous Receiver/Transmitter	189	4/7

† These MSI functions are hardwired.



Module Count = 1

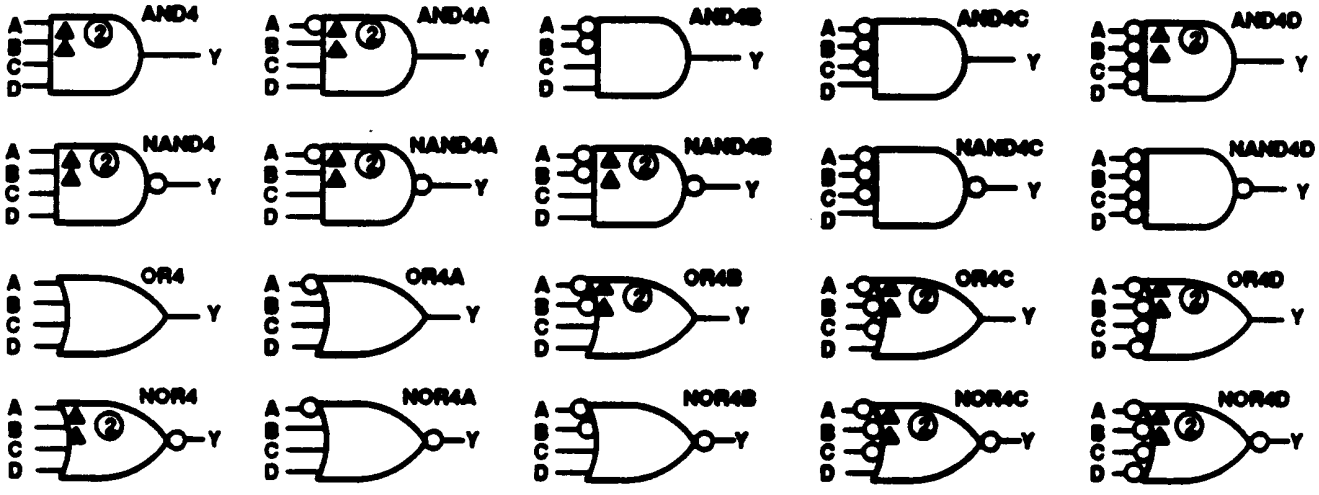
Figure 11. 2-Input Gates



Module Count = 1 (unless otherwise noted)

② Indicates 2-level module macro ▲ Indicates extra delay input

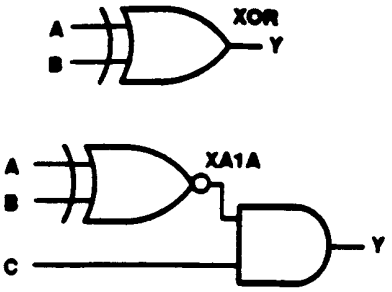
Figure 12. 3-Input Gates



Module Count = 1 (unless otherwise noted)

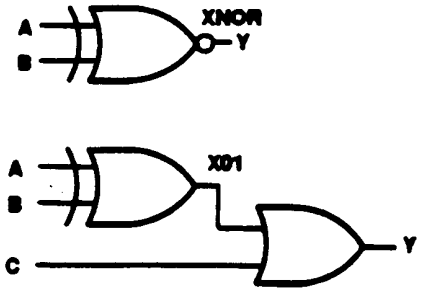
② Indicates 2-level module macro ▲ Indicates extra delay input

Figure 13. 4-Input Gates



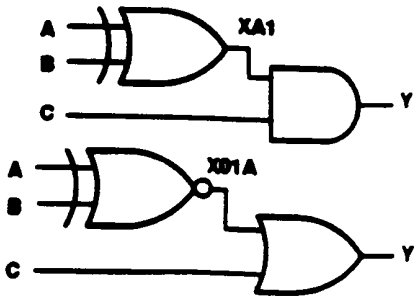
Module Count = 1

Figure 14. XOR/XNOR Gates



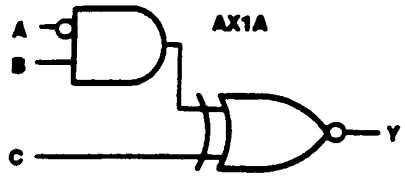
Module Count = 1

Figure 15. XOR-OR/XNOR-OR Gates

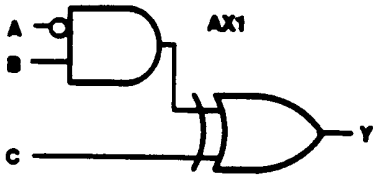


Module Count = 1

Figure 16. XOR-AND/XNOR-AND Gates



Module Count = 1



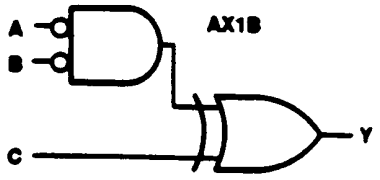


Figure 17. AND-XOR Gates

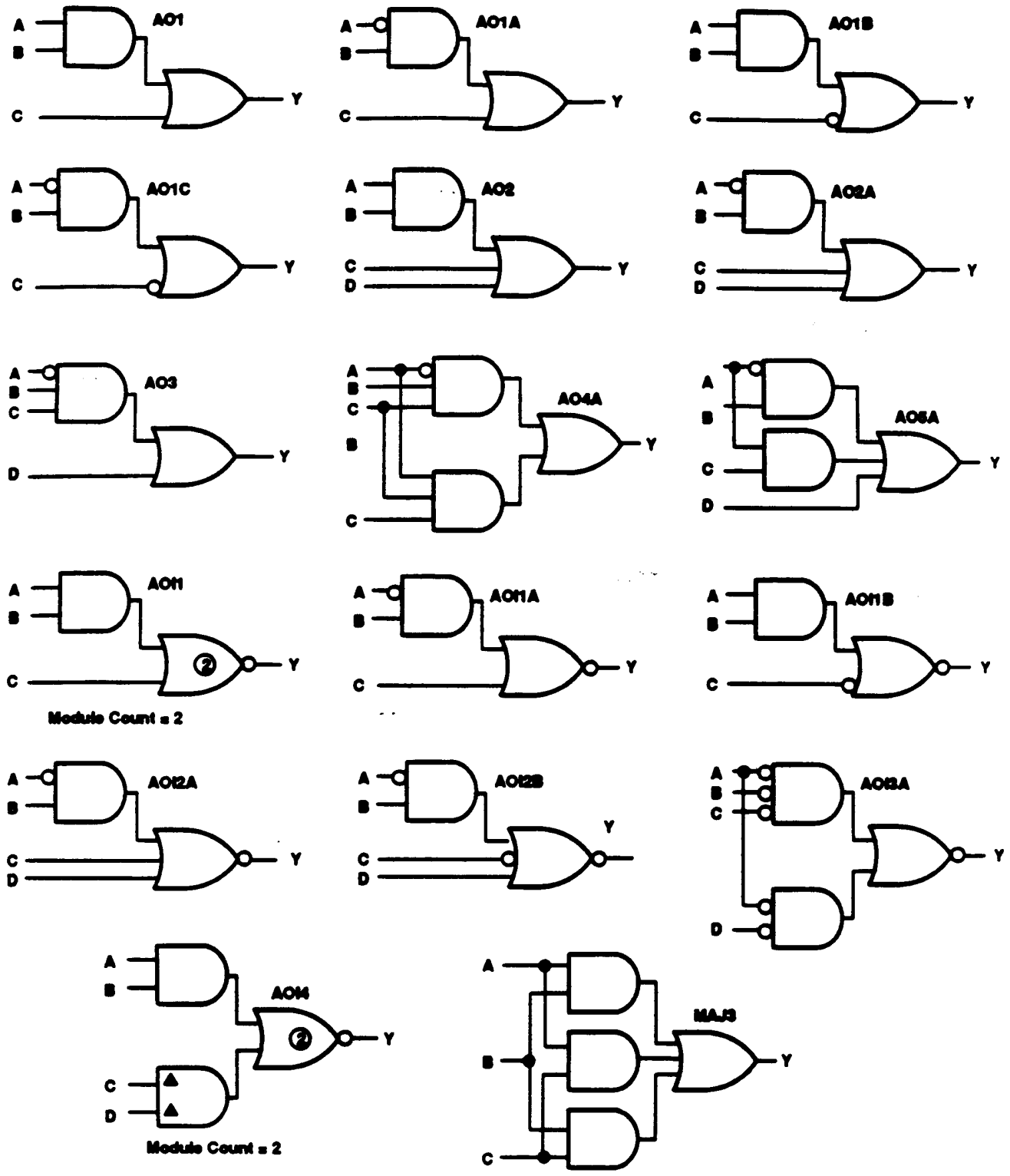


Figure 18. AND OR/AND-NOR Gates

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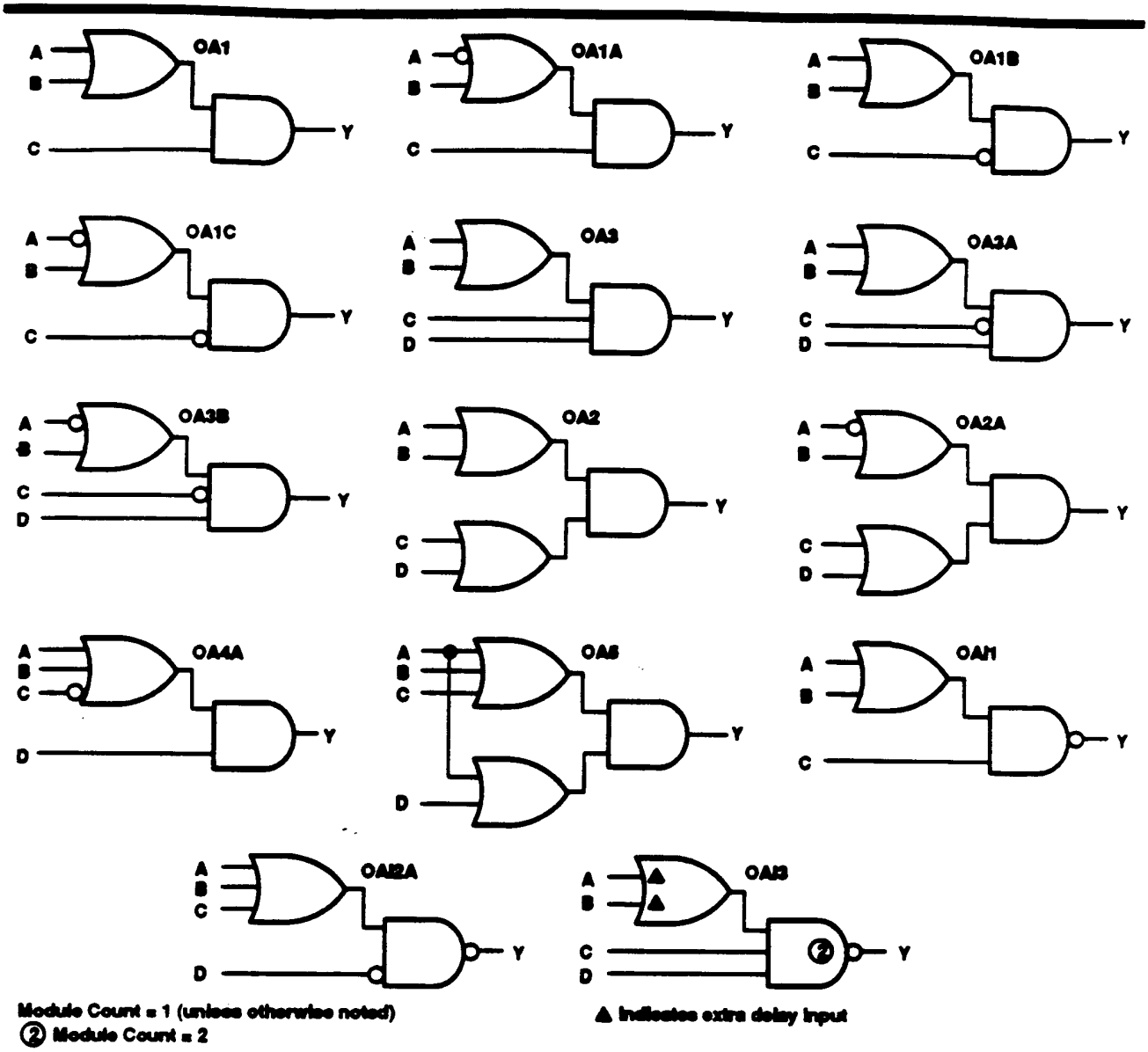

Module Count = 1 (unless otherwise noted)
② Module Count = 2
▲ Indicates extra delay input

Figure 19. OR-AND/OR-NAND Gates

Module Count = 1

Figure 20. Buffers

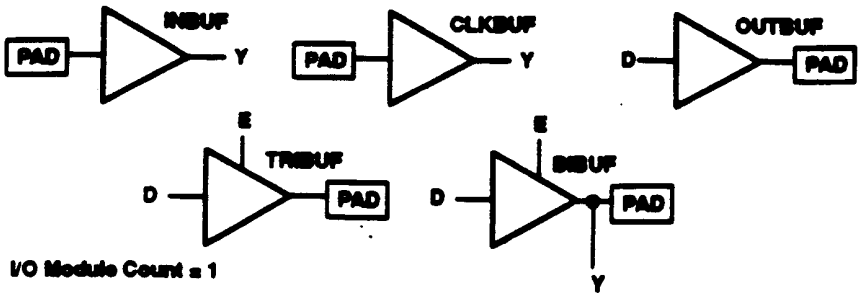

Figure 21. I/O Buffers

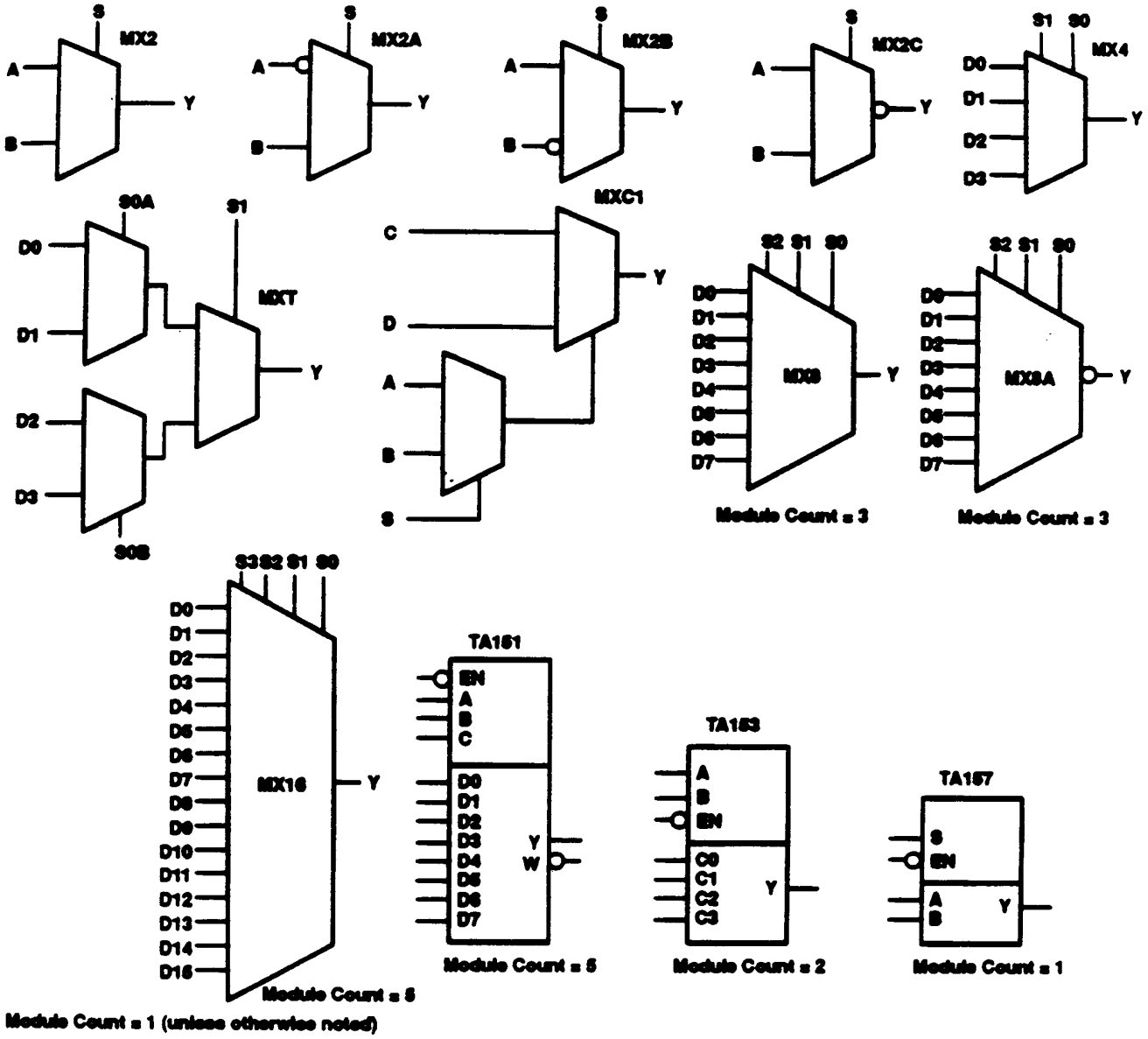

Figure 22. Multiplexers

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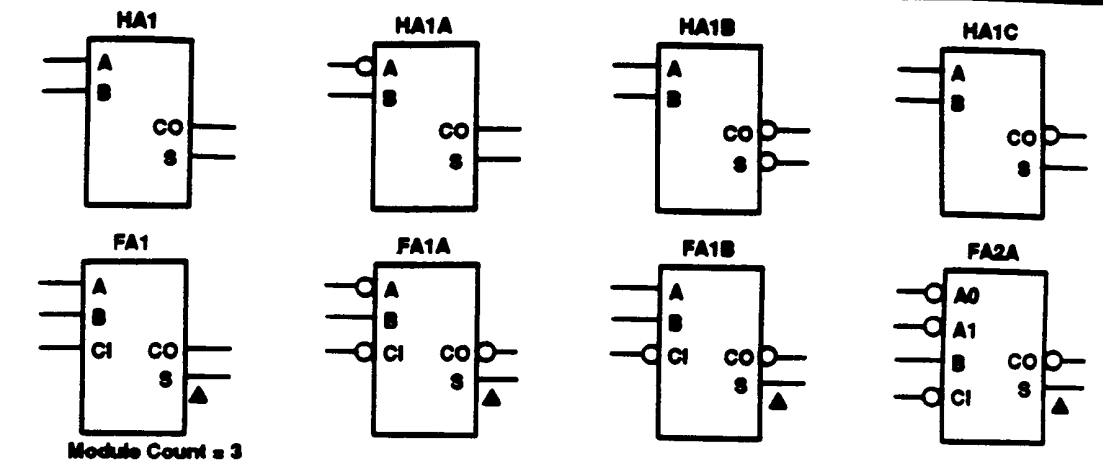

Module Count = 2 (unless otherwise noted)
▲ Indicates two logic module delay path

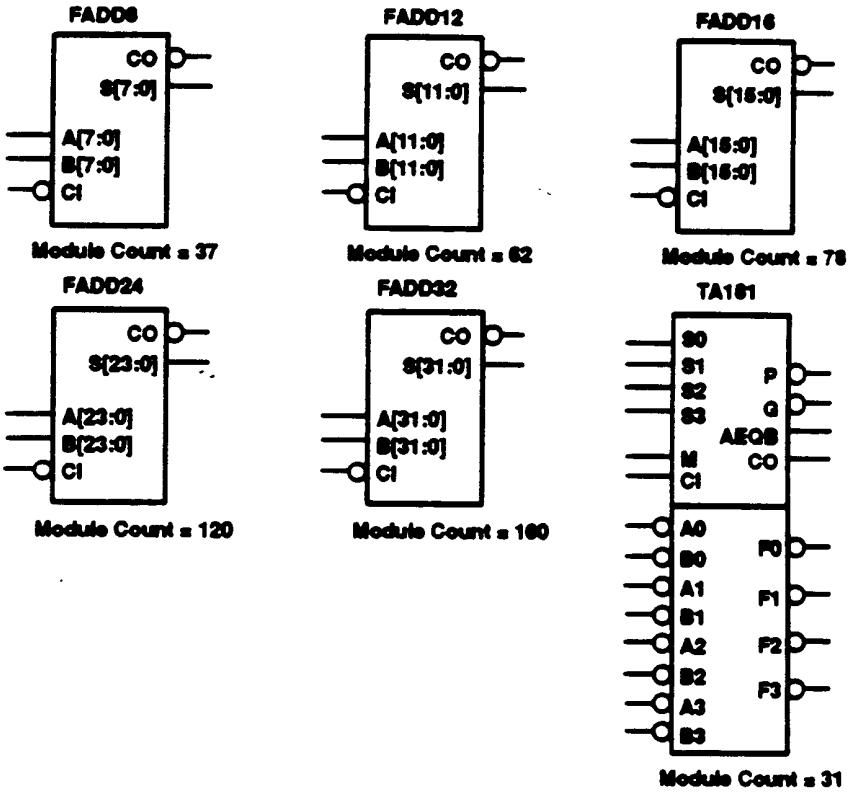

Figure 23. Adders

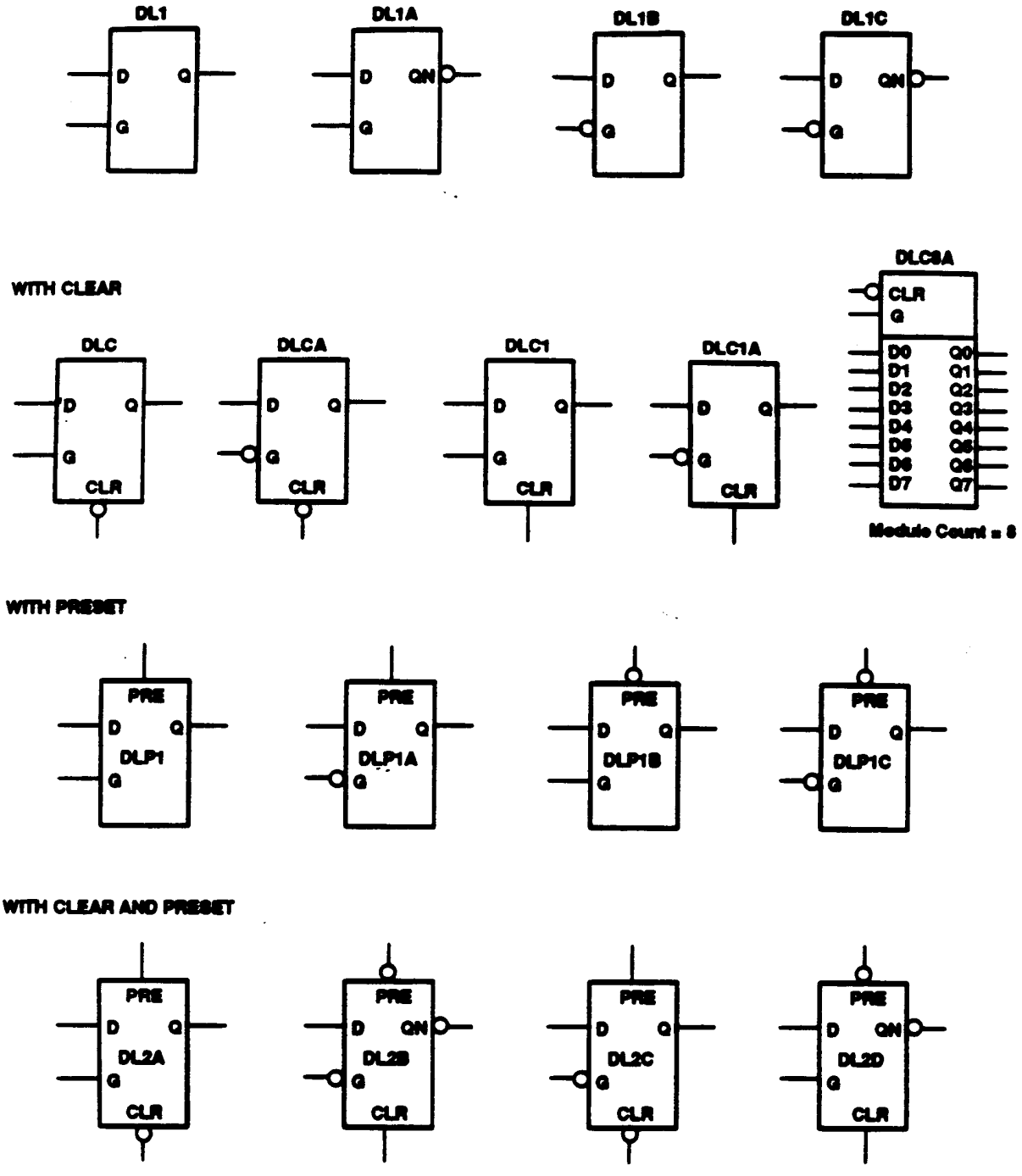

Figure 24. D-Type Latches

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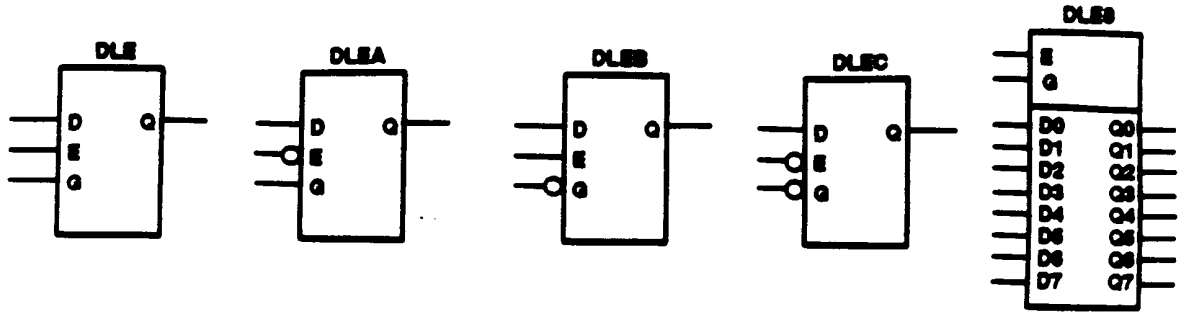
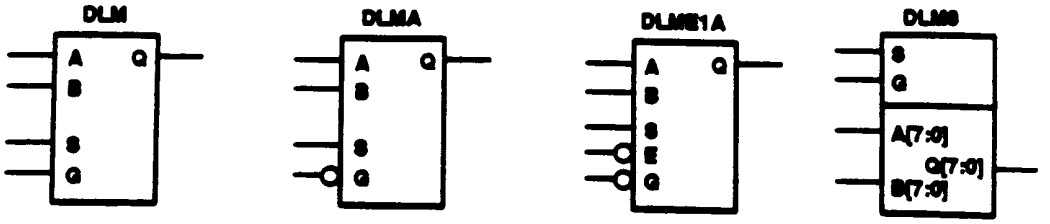
WITH ENABLE



Module Count = 8

WITH MULTIPLEXED INPUTS



Module Count = 1 (unless otherwise noted)

Module Count = 8

Figure 24. D-Type Latches (continued)

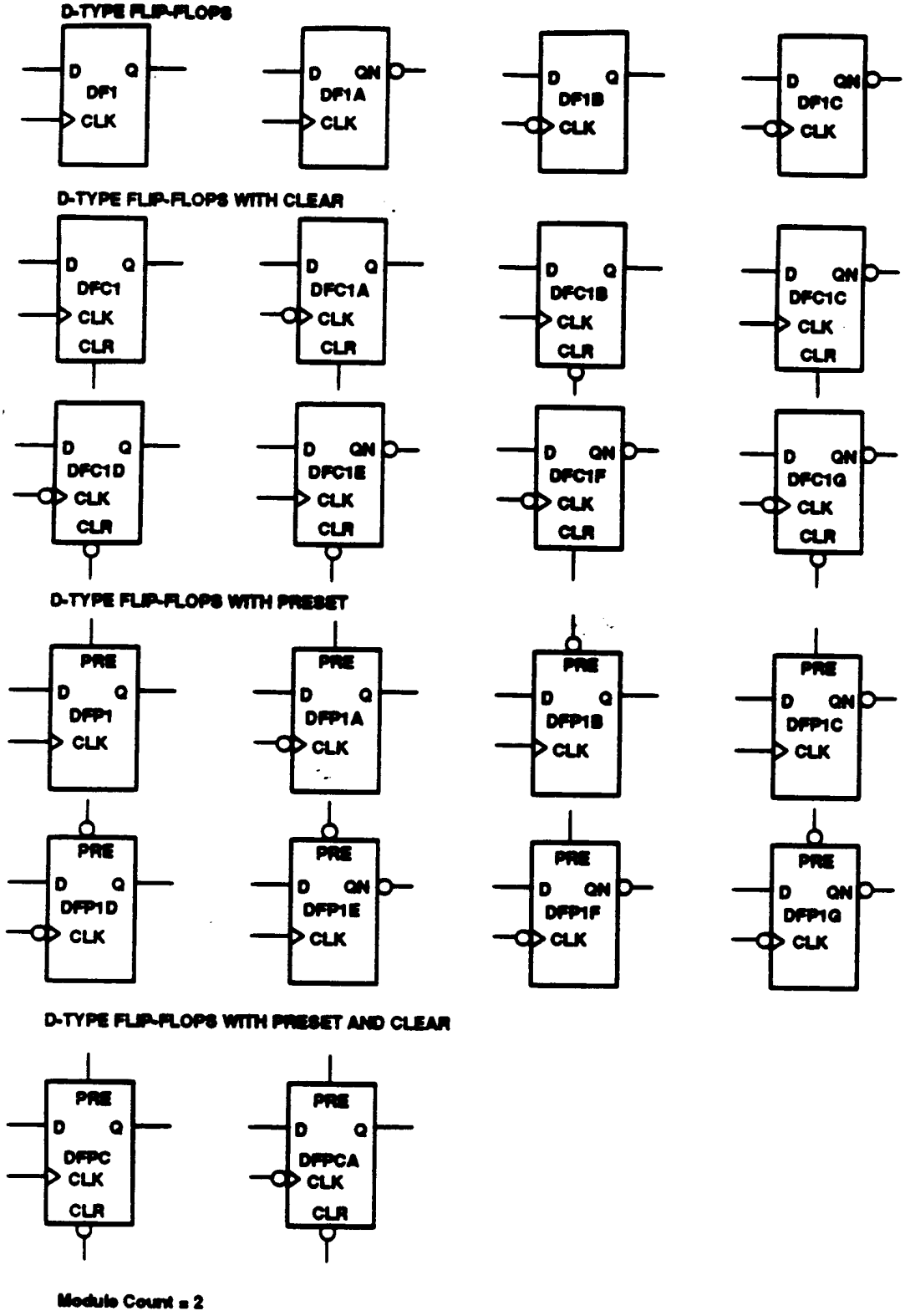


Figure 25. D-Type Flip-Flops

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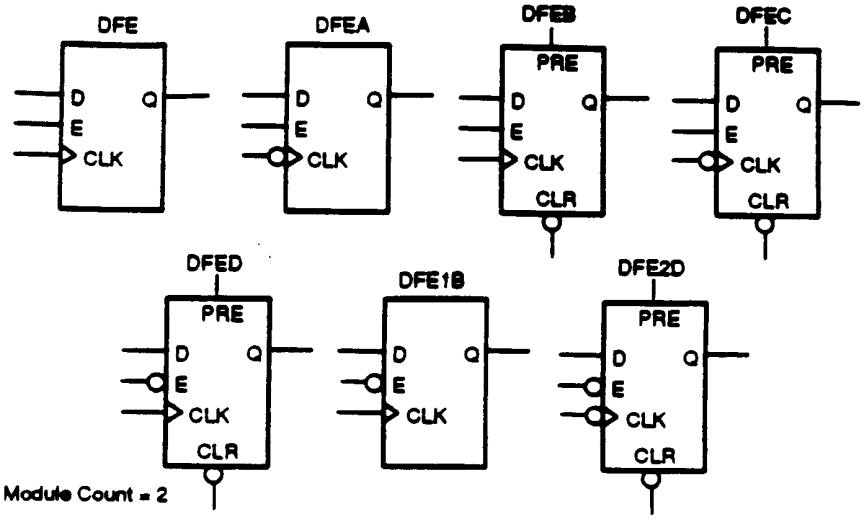

Figure 26. D-Type Flip-Flops with Enable

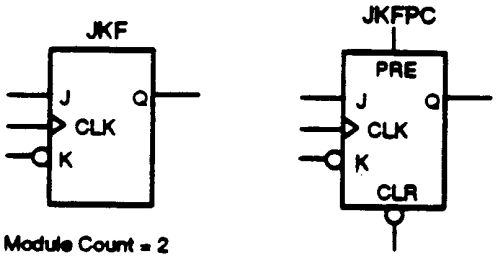

Figure 27. J-$\overline{K}$ Flip-Flops

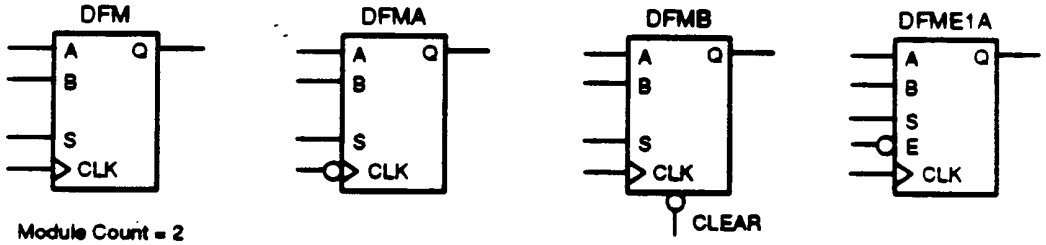

Figure 28. Multiplexed-Input Flip-Flops

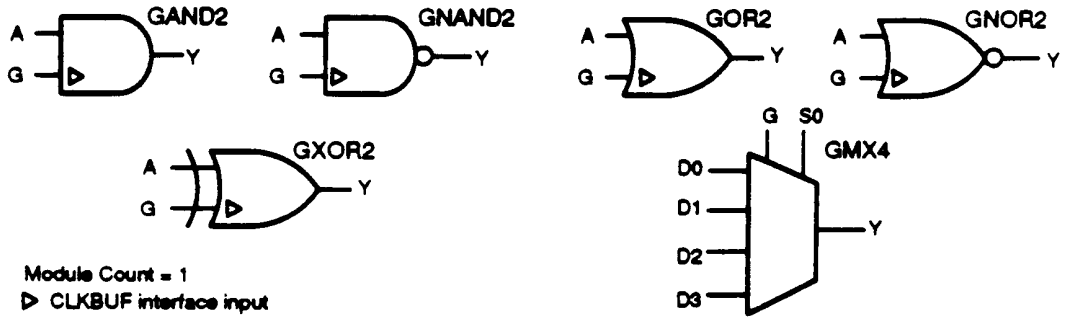

Figure 29. Clock Buffer (CLKBUF) Interface

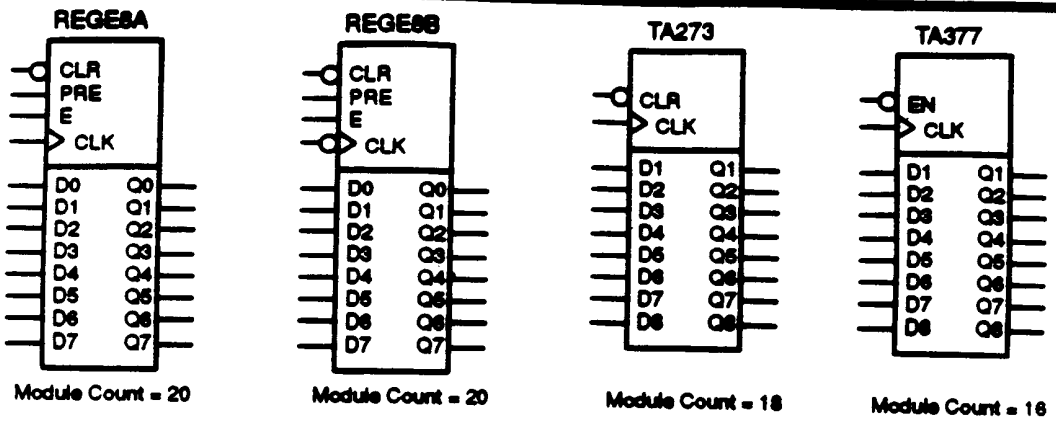

Figure 30. Octal D-Type Flip-Flops and Registers

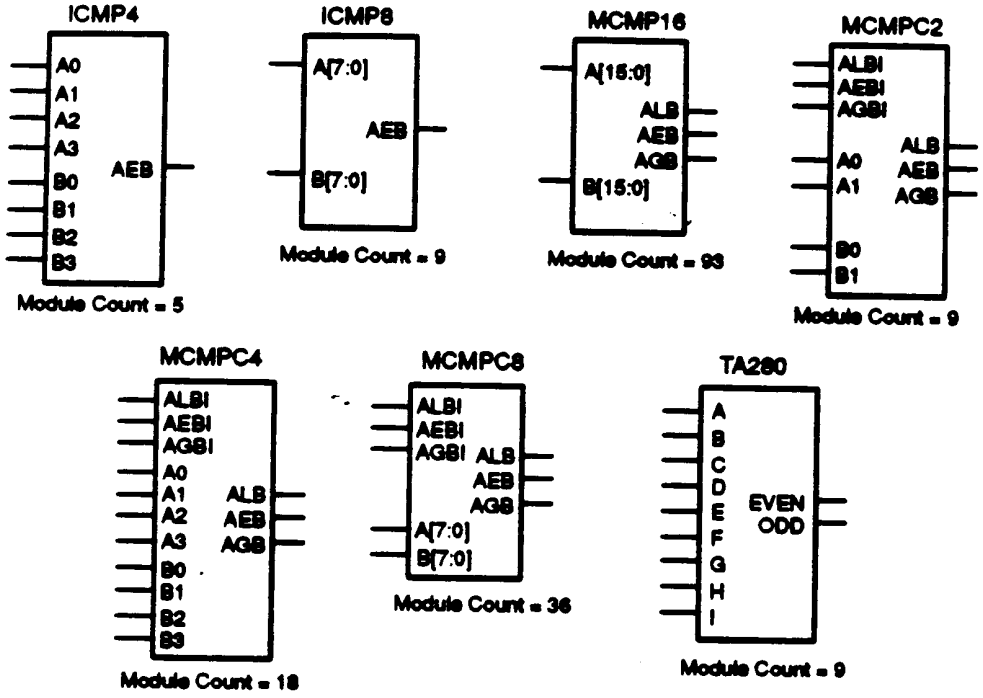

Figure 31. Comparators/Parity Checker

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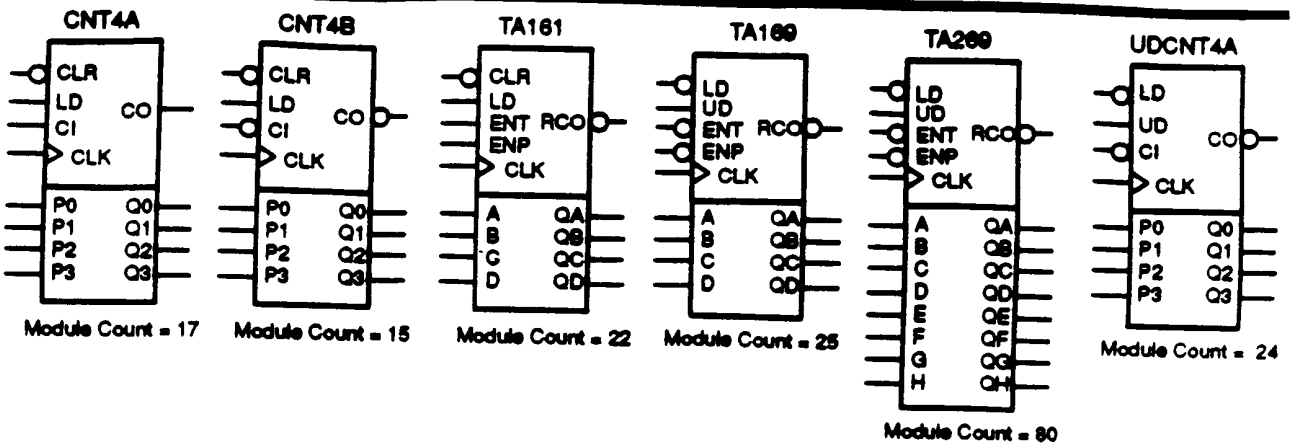

Figure 32. Counters

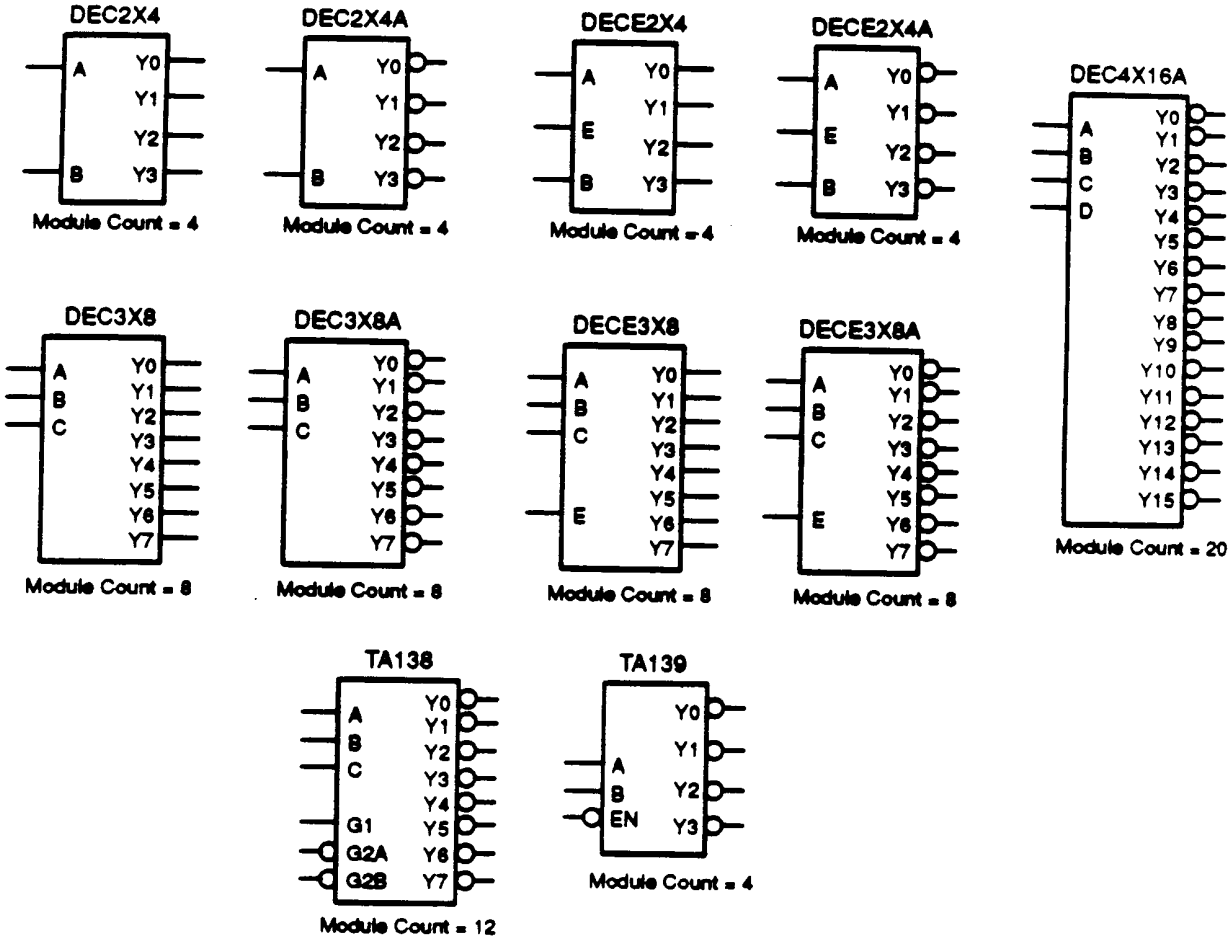

Figure 33. Decoders

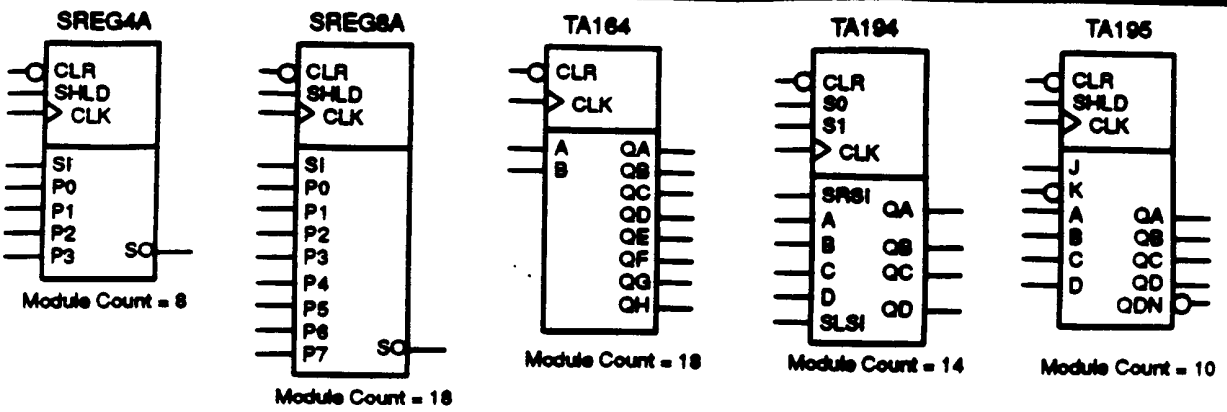

Figure 34. Shift Registers

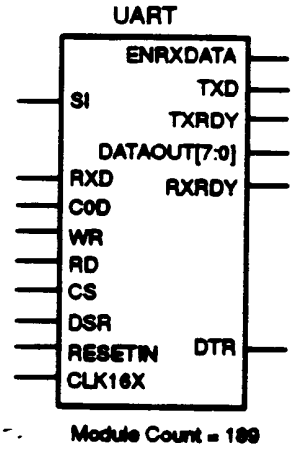

Figure 35. Universal Asynchronous Receiver/Transmitter (UART)

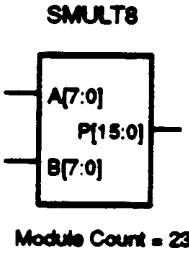

Figure 36. 8-Bit Multiplier

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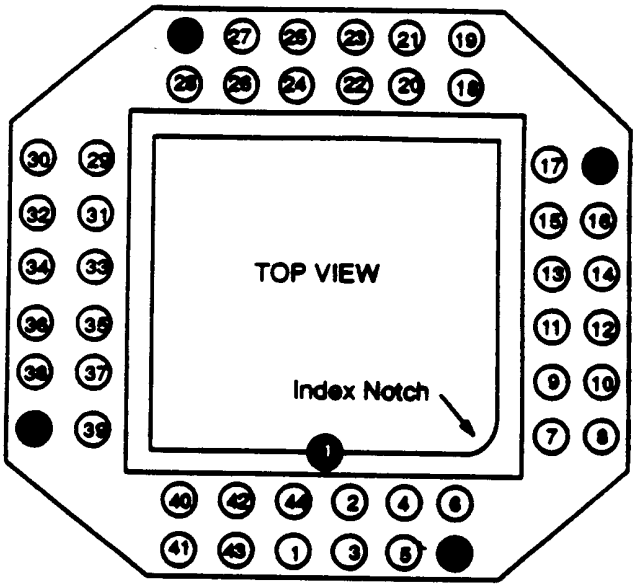
actionprobes

There are four types of Actionprobes available: 44-, 68-, and 84-pin LCC and an 84-pin PGA. At the time your order is placed, please specify which Actionprobe you need.

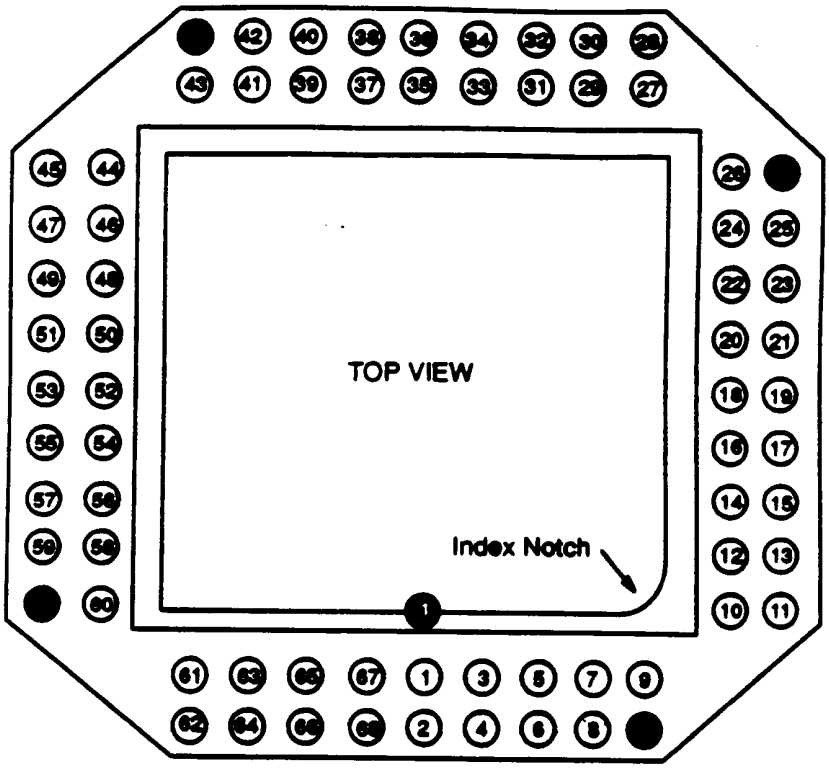
The Actionprobes are detailed in Figures 37 through 40.



● Indicates no connection

NOTE: The view shown is from the TOP, with pin 1 of the device facing down.

Figure 37. 44-Pin PLCC Actionprobe



● Indicates no connection

NOTE: The view shown is from the TOP, with pin 1 of the device facing down.

Figure 38. 68-Pin PLCC Actionprobe

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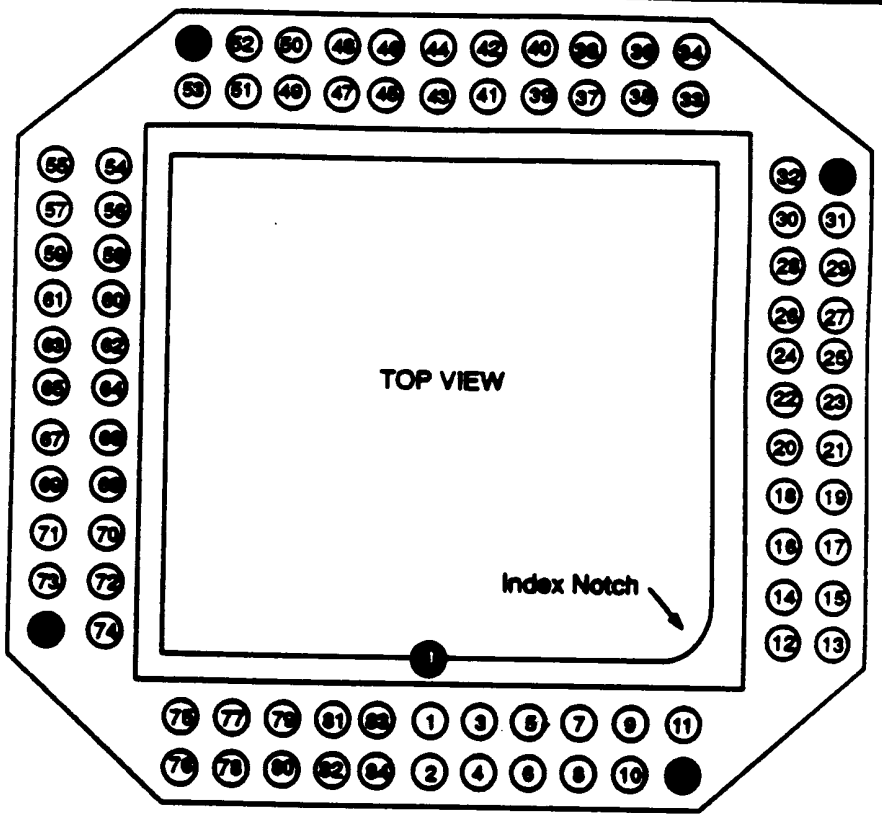

● Indicates no connection

NOTE: The view shown is from the TOP, with pin 1 of the device facing down.

Figure 39. 84-Pin PLCC Actionprobe

the 84-pin, PGA actionprobe

The 84-Pin, Pin Grid Array Actionprobe has a number of pins around the socket connected to the device pins. The exact ordering of these pins is not obvious.

Figure 40 shows the Actionprobe with the top view up, which is how the device sits in the socket. Pin A1 is at the top left. Looking at the Actionprobe, pin A1 appears on the circuit board for reference.

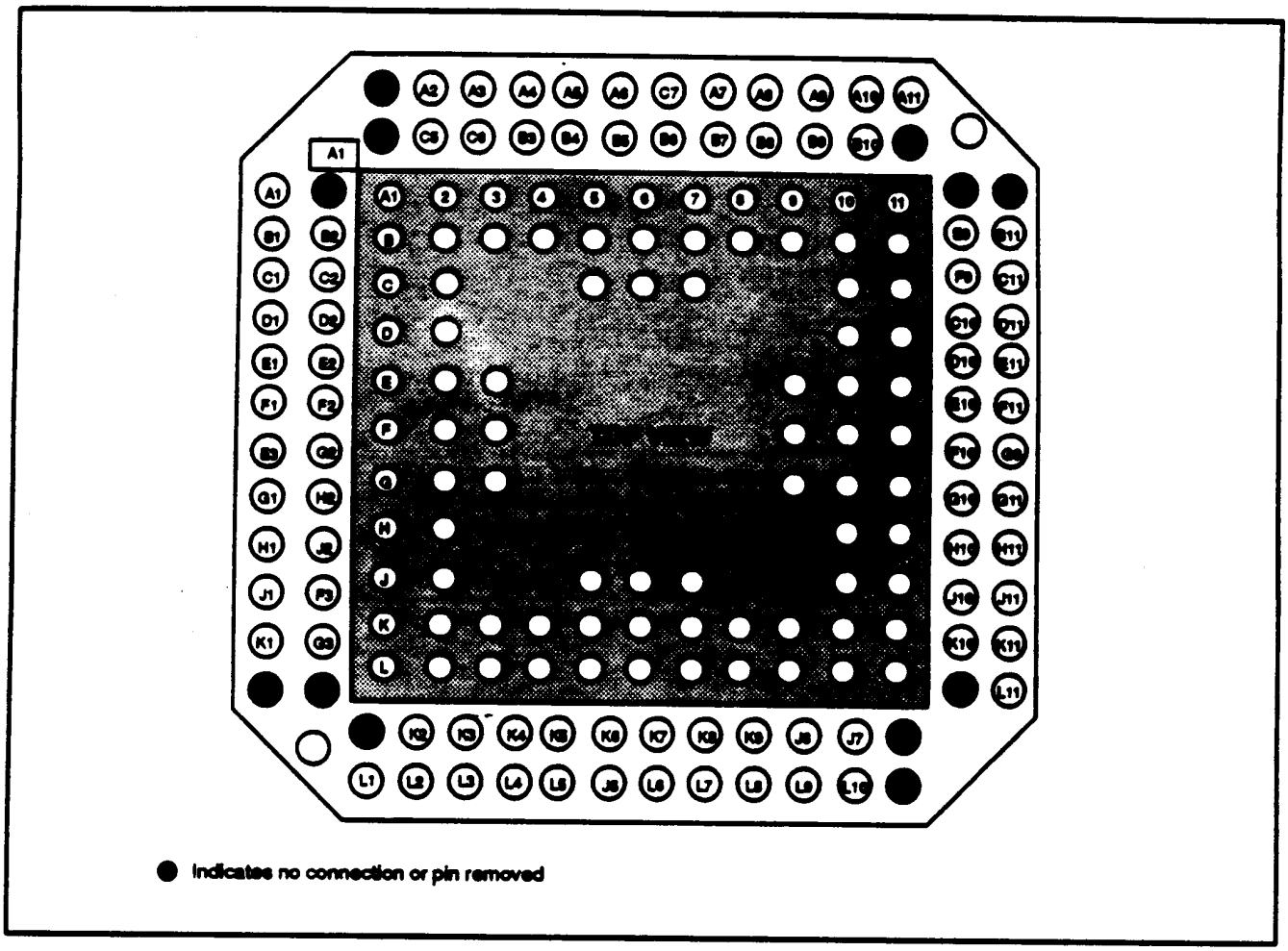

Figure 40. 84-Pin, PGA Actionprobe

FN044, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. Figure 41 gives a 20-pin package example. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

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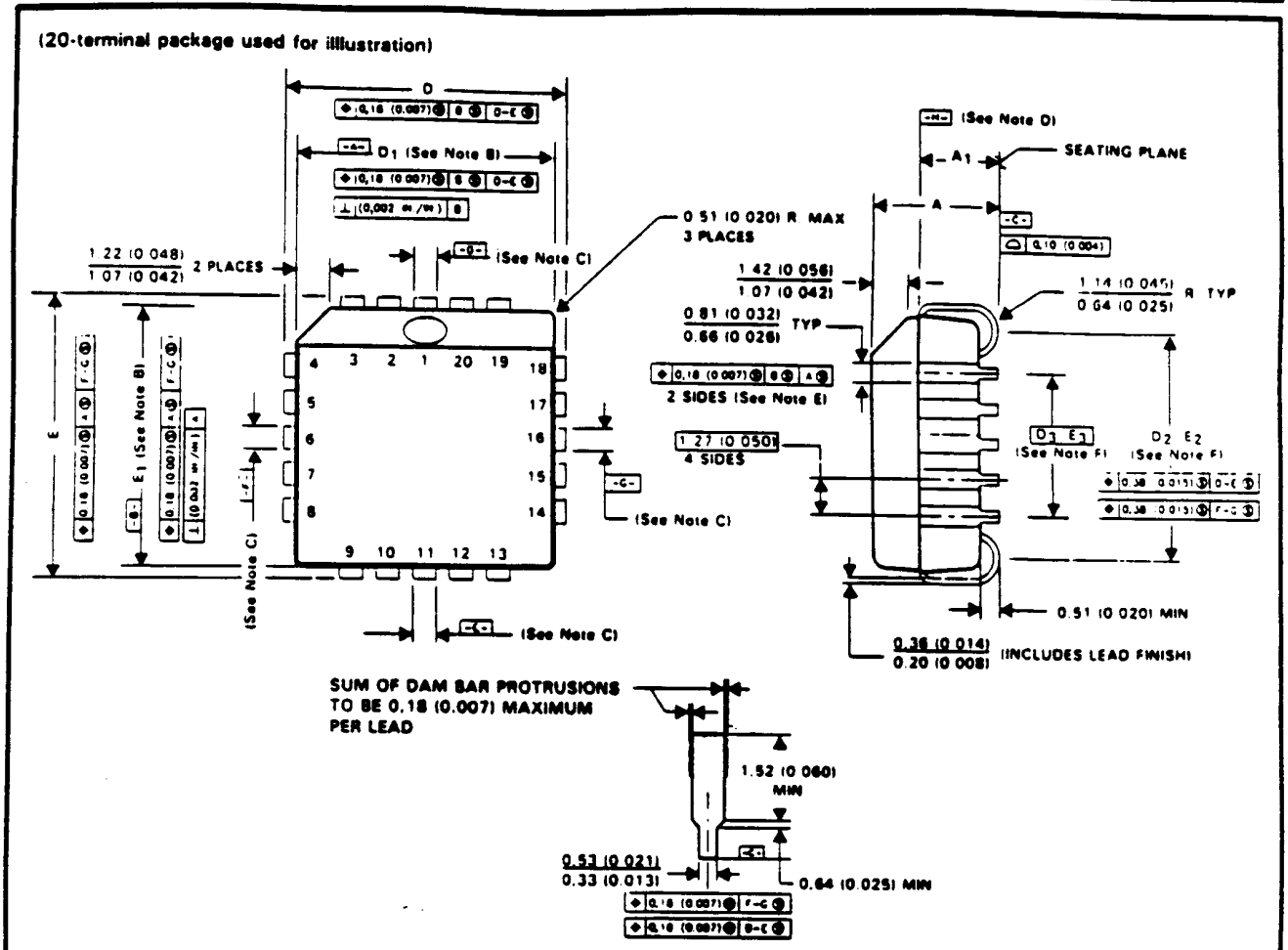


JEDEC OUTLINE	DIMS / PINS	A MIN	A MAX	A1 MIN	A1 MAX	D, E MIN	D, E MAX	D1, E1 MIN	D1, E1 MAX	D2, E2 MIN	D2, E2 MAX	D3, E3 BASIC
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AE	68	4,19 (0.165)	5.08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5.08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

B. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0.25 (0.010) on any side.

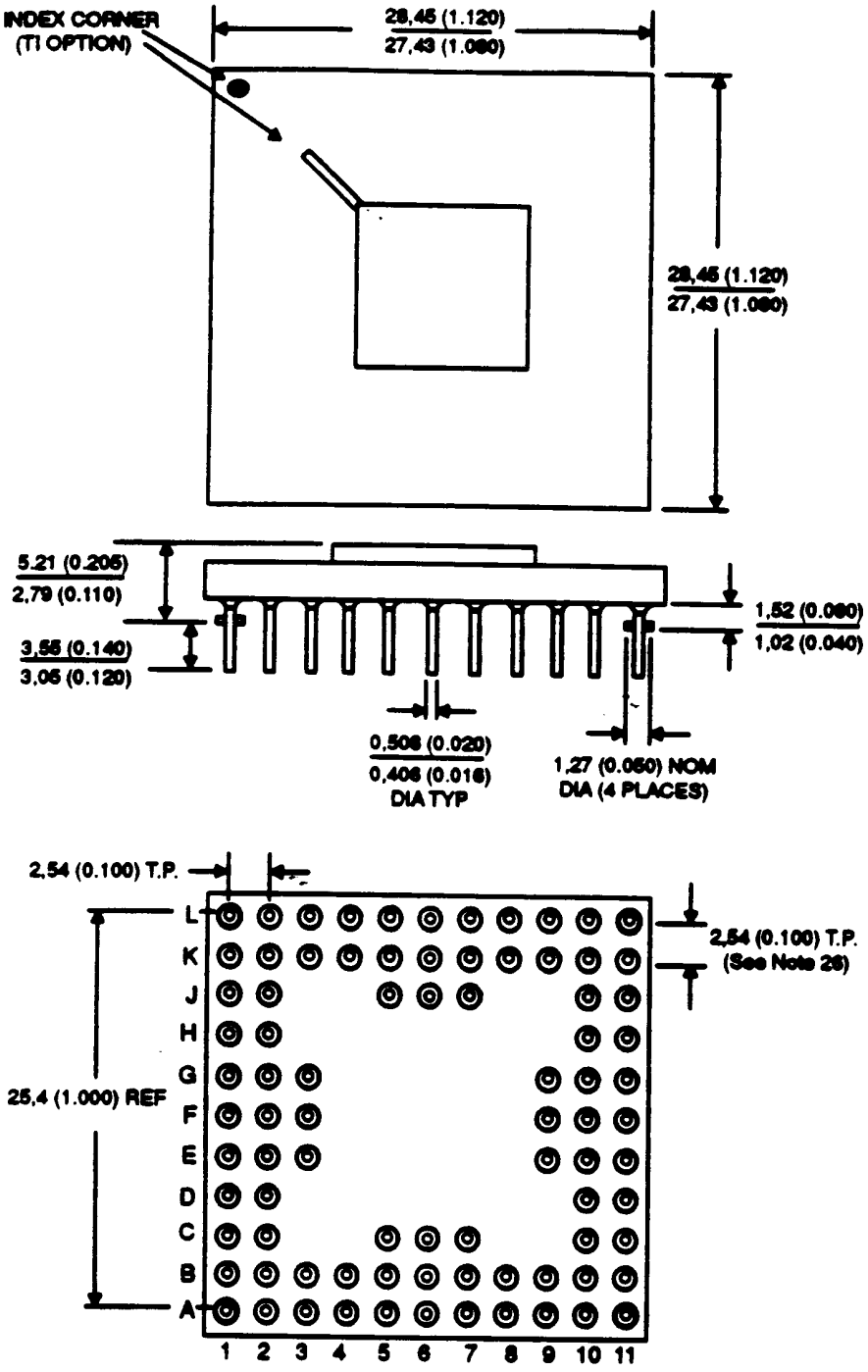
C. Datums [D–E] and [F–G] for center leads are determined at datum [–H–]

D. Datum [–H–] is located at top of leads where they exit plastic body.

E. Location to datums [–A–] and [–B–] to be determined at datum [–H–]

F. Determined at seating plane [–C–]

Figure 41. Plastic Leaded Chip Carriers



NOTE 1. Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,381 (0.051) radius relative to the center of the ceramic.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

Figure 42. 84-Pin, Pin Grid Array Ceramic Package