

TMS320DM368

Digital Media System-on-Chip (DMSoC)

Check for Samples: [TMS320DM368](#)

1 TMS320DM368 Digital Media System-on-Chip (DMSoC)

1.1 Features

- **Highlights**
 - High-Performance Digital Media System-on-Chip (DMSoC)
 - 432-MHz ARM926EJ-S Clock Rate
 - Two Video Image Co-processors (HDVICP, MJCP) Engines
 - Supports a Range of Encode, Decode, and Video Quality Operations
 - Video Processing Subsystem
 - HW Face Detect Engine
 - Resize Engine from 1/16x to 8x
 - 16-Bit Parallel AFE (Analog Front-End) Interface Up to 120 MHz
 - 4:2:2 (8-/16-bit) Interface
 - 8-/16-bit YCC and Up to 24-Bit RGB888 Digital Output
 - 3 DACs for HD Analog Video Output
 - Hardware On-Screen Display (OSD)
 - Capable of 1080p 30fps H.264 video processing
 - Peripherals include EMAC, USB 2.0 OTG, DDR2/NAND, 5 SPIs, 2 UARTs, 2 MMC/SD/SDIO, Key Scan
 - 8 Different Boot Modes and Configurable Power-Saving Modes
 - Pin-to-pin and software compatible with DM365
 - Extended temperature (-40°C – 85°C) available
 - 3.3-V and 1.8-V I/O, 1.35-V Core
 - 338-Pin Ball Grid Array at 65nm Process Technology
- High-Performance Digital Media System-on-Chip (DMSoC)
 - 432-MHz ARM926EJ-S Clock Rate
 - 4:2:2 (8-/16-Bit) Interface
 - Capable of 1080p 30fps H.264 video processing
 - Pin compatible with DM365 processors
 - Fully Software-Compatible With ARM9™
 - Extended temperature available for 432-MHz device
- ARM926EJ-S™ Core
 - Support for 32-Bit and 16-Bit (Thumb® Mode) Instruction Sets
 - DSP Instruction Extensions and Single Cycle MAC
 - ARM® Jazelle® Technology
 - Embedded ICE-RT Logic for Real-Time Debug
- ARM9 Memory Architecture
 - 16K-Byte Instruction Cache
 - 8K-Byte Data Cache
 - 32K-Byte RAM
 - 16K-Byte ROM
 - Little Endian
- Two Video Image Co-processors (HDVICP, MJCP) Engines
 - Support a Range of Encode and Decode Operations
 - H.264, MPEG4, MPEG2, MJPEG, JPEG, WMV9/VC1
- Video Processing Subsystem
 - Front End Provides:
 - HW Face Detect Engine
 - Hardware IPIPE for Real-Time Image Processing
 - Resize Engine
 - Resize Images From 1/16x to 8x
 - Separate Horizontal/Vertical Control
 - Two Simultaneous Output Paths
 - IPIPE Interface (IPIPEIF)
 - Image Sensor Interface (ISIF) and CMOS Imager Interface
 - 16-Bit Parallel AFE (Analog Front End) Interface Up to 120 MHz
 - Glueless Interface to Common Video Decoders
 - BT.601/BT.656/BT.1120 Digital YCbCr 4:2:2 (8-/16-Bit) Interface
 - Histogram Module



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- Lens distortion correction module (LDC)
- Back End Provides:
 - Hardware On-Screen Display (OSD)
 - Composite NTSC/PAL video encoder output
 - 8-/16-bit YCC and Up to 24-Bit RGB888 Digital Output
 - 3 DACs for HD Analog Video Output
 - LCD Controller
 - BT.601/BT.656 Digital YCbCr 4:2:2 (8-/16-Bit) Interface
- Analog-to-Digital Convertor (ADC)
- Power Management and Real Time Clock Subsystem (PRTCSS)
 - Real Time Clock
- 16-Bit Host-Port Interface (HPI)
- 10/100 Mb/s Ethernet Media Access Controller (EMAC) - Digital Media
 - IEEE 802.3 Compliant
 - Supports Media Independent Interface (MII)
 - Management Data I/O (MDIO) Module
- Key Scan
- Voice Codec
- External Memory Interfaces (EMIFs)
 - DDR2 and mDDR SDRAM 16-bit wide EMIF With 256 MByte Address Space (1.8-V I/O)
 - Asynchronous 16-/8-bit Wide EMIF (AEMIF)
 - Flash Memory Interfaces
 - NAND (8-/16-bit Wide Data)
 - 16 MB NOR Flash, SRAM
 - OneNAND(16-bit Wide Data)
- Flash Card Interfaces
 - Two Multimedia Card (MMC) / Secure Digital (SD/SDIO)
 - SmartMedia/xD
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- USB Port with Integrated 2.0 High-Speed PHY that Supports
 - USB 2.0 High-Speed Device
 - USB 2.0 High-Speed Host (mini-host, supporting one external device)
 - USB On The Go (HS-USB OTG)
- Four 64-Bit General-Purpose Timers (each configurable as two 32-bit timers)
- One 64-Bit Watch Dog Timer
- Two UARTs (One fast UART with RTS and CTS Flow Control)
- Five Serial Port Interfaces (SPI) each with two Chip-Selects
- One Master/Slave Inter-Integrated Circuit (I²C) Bus™
- One Multi-Channel Buffered Serial Port (McBSP)
 - I2S
 - AC97 Audio Codec Interface
 - S/PDIF via Software
 - Standard Voice Codec Interface (AIC12)
 - SPI Protocol (Master Mode Only)
 - Direct Interface to T1/E1 Framers
 - Time Division Multiplexed Mode (TDM)
 - 128 Channel Mode
- Four Pulse Width Modulator (PWM) Outputs
- Four RTO (Real Time Out) Outputs
- Up to 104 General-Purpose I/O (GPIO) Pins (Multiplexed with Other Device Functions)
- Boot Modes
 - On-Chip ARM ROM Bootloader (RBL) to Boot From NAND Flash, MMC/SD, UART, USB, SPI, EMAC, or HPI
 - AEMIF (NOR and OneNAND)
- Configurable Power-Saving Modes
- Crystal or External Clock Input (typically 19.2 MHz, 24 MHz, 27 MHz or 36 MHz)
- Flexible PLL Clock Generators
- Debug Interface Support
 - IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
 - ETB (Embedded Trace Buffer) with 4K-Bytes Trace Buffer memory
 - Device Revision ID Readable by ARM
- 338-Pin Ball Grid Array (BGA) Package (ZCE Suffix), 0.65-mm Ball Pitch
- 65nm Process Technology
- 3.3-V and 1.8-V I/O, 1.35-V Internal
- Community Resources
 - [TI E2E Community](#)
 - [TI Embedded Processors Wiki](#)

1.2 Description

Developers can now deliver crystal clear multi-format video at up to 1080p H.264 at 30fps (encode and closed-looped decode) in their digital video designs without concerns of video format support, constrained network bandwidth, limited system storage capacity or cost with the new TMS320DM368 DaVinci™ video processors from Texas Instruments Incorporated (TI).

The DM368 is capable of achieving HD video processing at 1080p 30fps H.264 and is completely pin-to-pin compatible with the DM365 processors, using the same ARM926EJ-S core running at 432 MHz. This ARM9-based DM368 device supports production-qualified H.264BP/MP/HP, MPEG-4, MPEG-2, MJPEG and VC1/WMV9 codecs providing customers with the flexibility to select the right video codec for their application. These codecs run on independent coprocessors (HDVICP and MJCP) offloading all compression needs from the main ARM core. This allows developers to obtain optimal performance from the ARM for their applications, including their multi-channel, multi-stream and multi-format needs.

Video surveillance designers achieve greater compression efficiency to provide more storage without straining the network bandwidth. Developers of media playback and camera-driven applications, such as video doorbells, digital signage, digital video recorders, portable media players and more can take advantage of the low power consumption and can ensure interoperability, as well as product scalability by taking advantage of the full suite of codecs supported on the DM368.

Along with multi-format HD video, the DM368 also features a suite of peripherals saving developers on system cost and complexity to enable a seamless interface to most additional external devices required for video applications. The image sensor interface is flexible enough to support CCD, CMOS, and various other interfaces such as BT.656, BT1120. The DM368 also offers a high level of integration with HD display support, including three built-in 10-bit HD analog video digital-to-analog converters (DACs), DDR2/mDDR, Ethernet MAC, USB 2.0, integrated audio, host port interface (HPI), analog-to-digital converter and many more features saving developers on overall system costs, as well as real estate on their circuit boards allowing for a slimmer, sleeker design.

1.3 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the TMS320DM368 device.

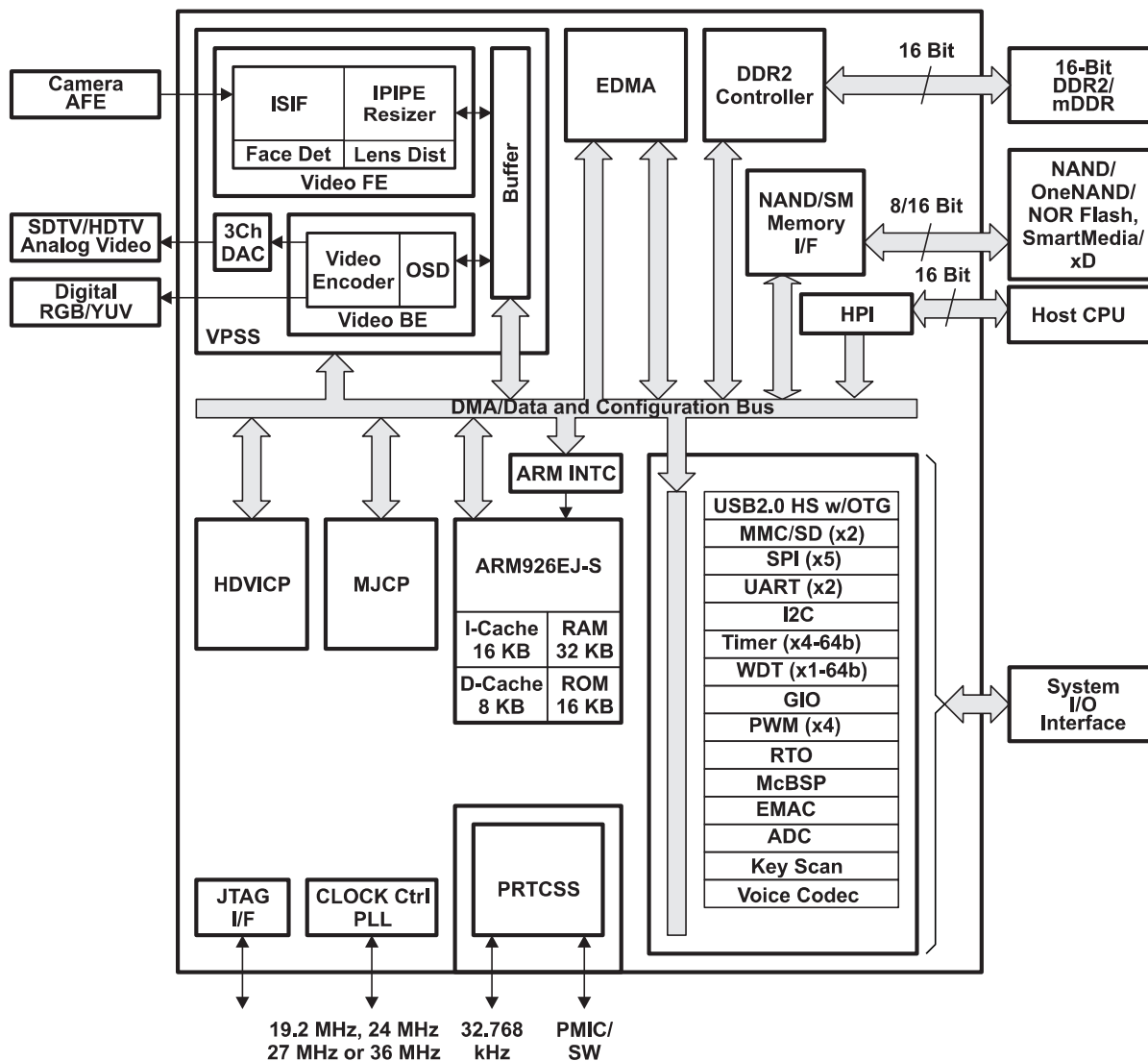


Figure 1-1. Functional Block Diagram