8,192 WORD×9 BIT CMOS
STATIC RAM

# TC5589P/J-20, TC5589P/J-25, TC5589P/J-35

## DESCRIPTION

The TC5589P/J is a 65,536 bit high speed static random access memory organized as 8,192 words by 9bits

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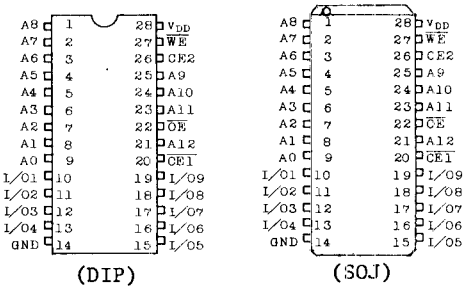
The TC5589P/J is a 65,536 bit high speed static random access memory organized as 8,192 words by 9bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 20ns/25ns/35ns and maximum operating current of 120mA at maximum cycle time. The TC5589P/J also features an automatic stand-by mode. The TC5589P/J is suitable for use ir cache memory and high speed storage, where high speed/ high density are required. The TC5589P/J is moulded in a 28 pin standard plastic DIP and a 28 pin plastic SOJ, with 0.3 inch width for high density assembly. The TC5589P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

## FEATURES

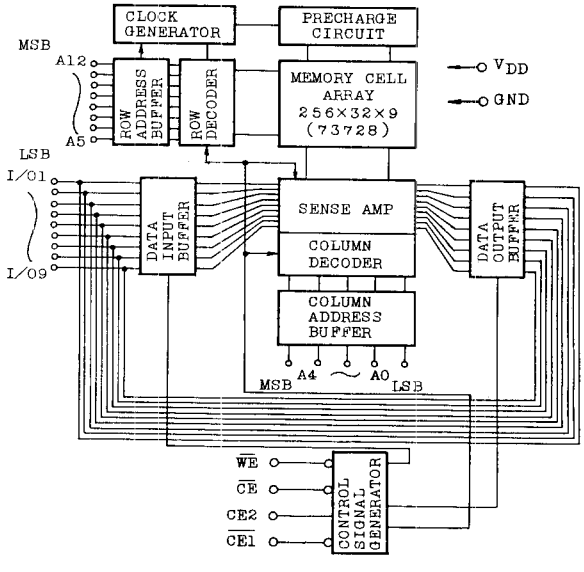
- Fast access time:
  - TC5589P/J-20 20ns (MAX.)
  - TC5589P/J-25 25ns (MAX.)
  - TC5589P/J-35 35ns (MAX.)
- Power dissipation: Operation 120mA (MAX.)
  Stand by 20mA (MAX.)
- 5V single power supply
- Full static operation
- Directly TTL compatible: All input and output
- Package: 28 pin plastic 300 mil DIP (TC5589P)
  28 pin plastic 300 mil SOJ (TC5589J)

## PIN CONNECTION




(DIP) (SOJ)

## BLOCK DIAGRAM




## PIN NAMES

| | |
|---|---|
| A0 ~ A13 | Address Inputs |
| I/01 ~ I/04 | Data Input/Output |
| CE1, CE2 | Chip Enable Input |
| WE | Write Enable Input |
| OE | Output Enable Input |
| $V_{DD}$ | Power (+5V) |
| GND | Ground |