

TOSHIBA

SYSTEM CATALOG

**FOR
FACSIMILES**

Facsimile System Block Diagrams

G3/B4 Facsimiles

Mechanical Block Diagram

Compatibility of Toshiba Semiconductors for Facsimile Use

Facsimile use can be divided into business use, in which facsimiles have become indispensable in the offices of numerous corporations, and personal or home use, in which facsimiles have exhibited significant proliferation in shops and in the home. The facsimile market is exhibiting an increasing number of products that use plain paper and new products are starting to appear featuring color reproduction. The operating speeds of high-performance business models are also becoming faster. In addition to incorporating answering telephone functions and cordless telephone functions, medium-performance models for personal and home use are now integrating photocopying functions and printer functions, demonstrating a growing trend towards multifunctional use. Toshiba is taking aggressive steps to accommodate the field of facsimile semiconductors in the future as well by attempting to expand its product lineup to accommodate these multifunctional applications.

Power Device

Power Devices

- Power supply devices
- Three-terminal/switching regulators
 - System power supplies
 - Photocouplers

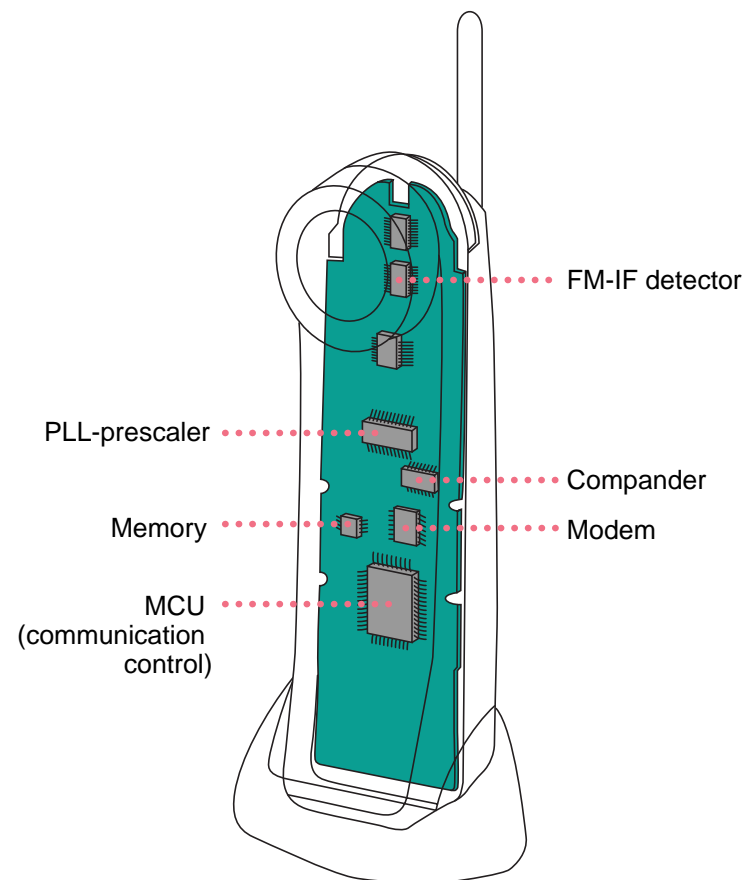
Please refer to the "Toshiba Product Guide for Power Supply ICs".

Display

Display Devices

- Various types of display devices
- LCD drivers/controllers

Please refer to the "Toshiba Product Guide for LCD Driver / Controller LSIs".

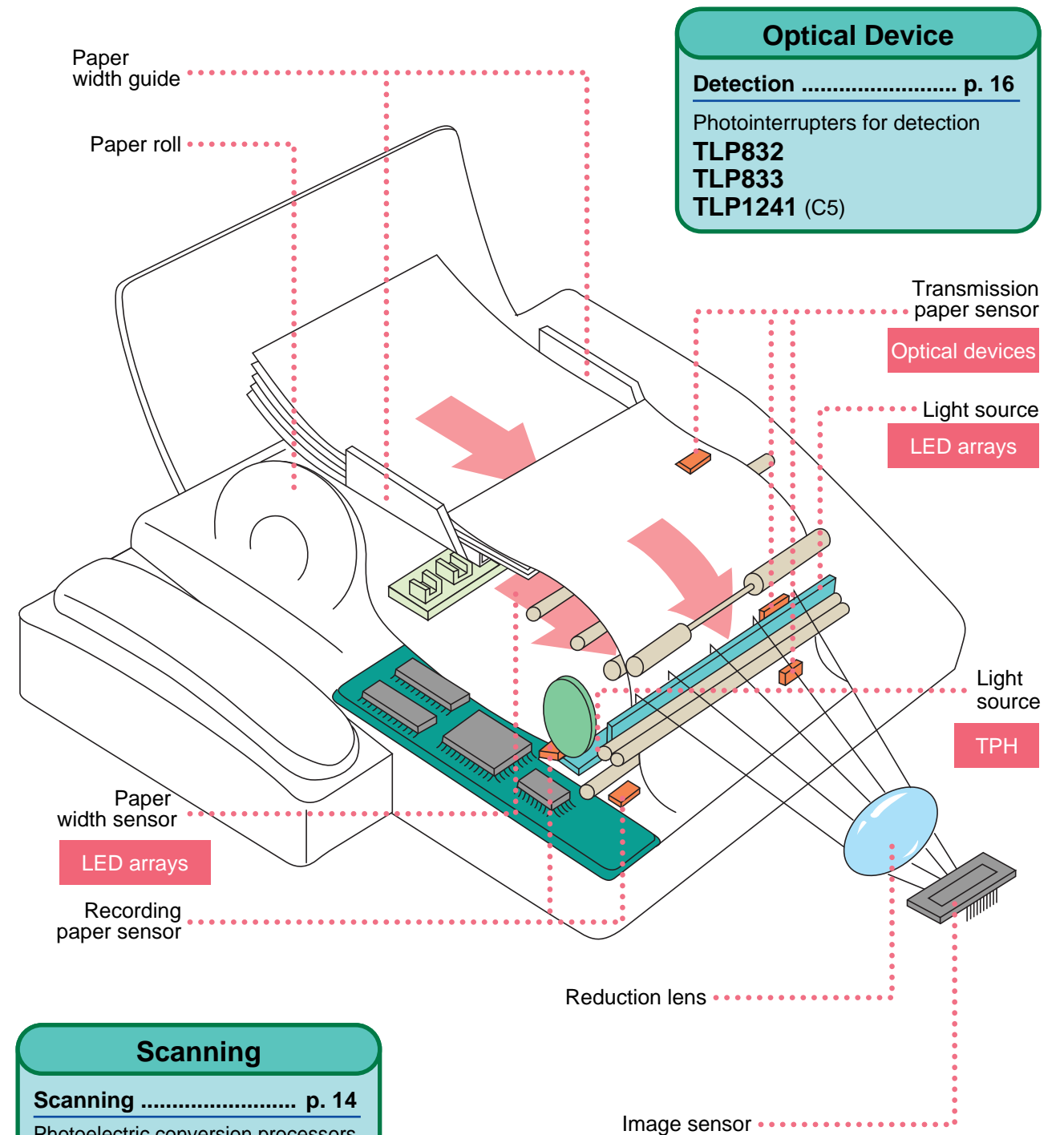


Motor Control

Motor Control p. 16

Motor control for driving mechanical systems

TB62201AF



Scanning

Scanning p. 14

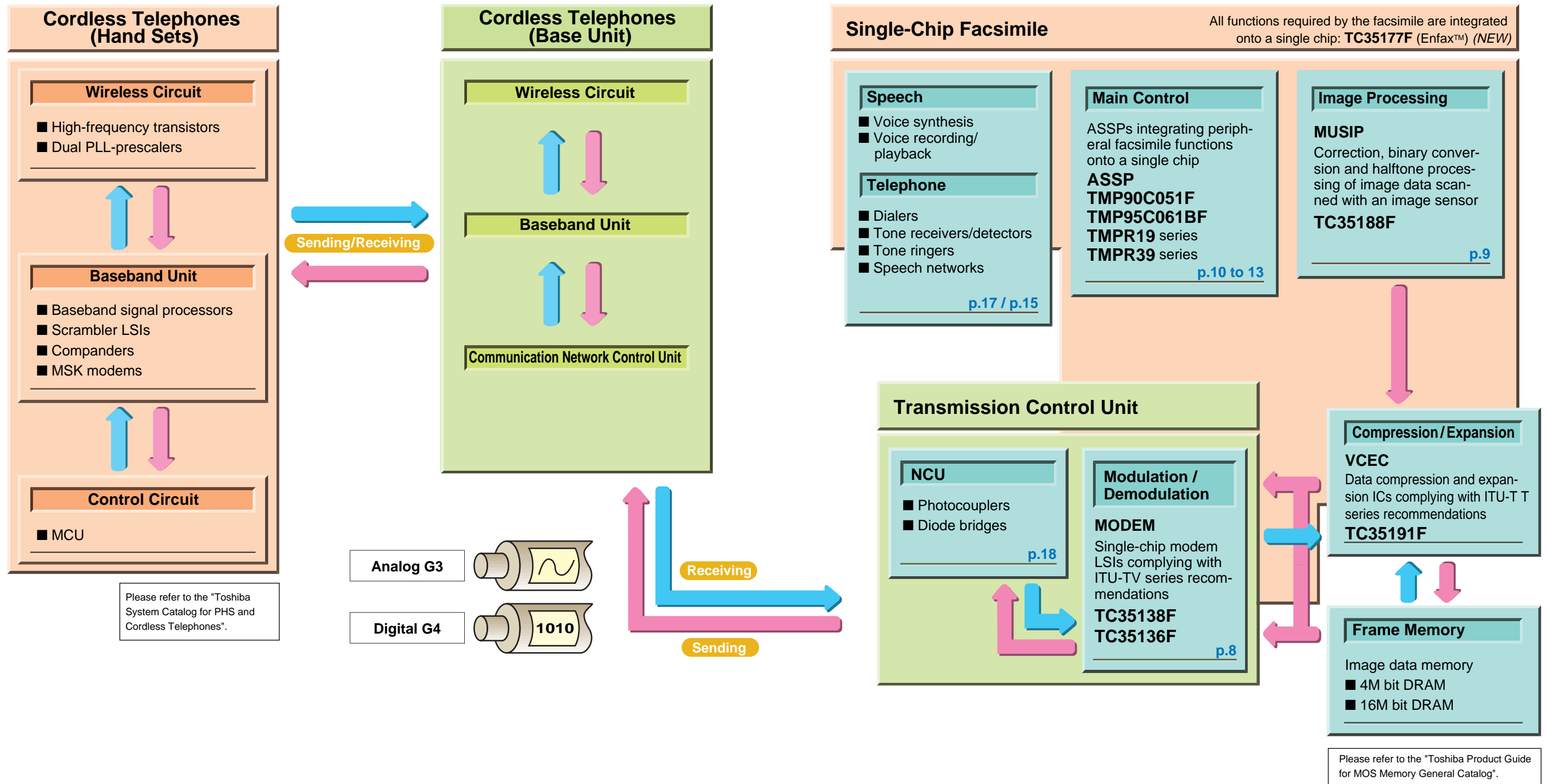
Photoelectric conversion processors

- TCD1252AP (A4)**
- TCD1208P (B4)**
- TCD1501D/1503D (A3)**

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Electric Signal Processing Block Diagram



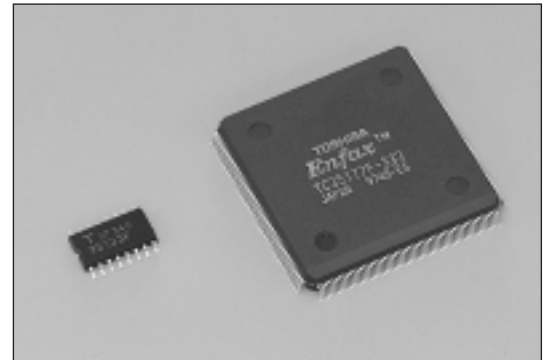
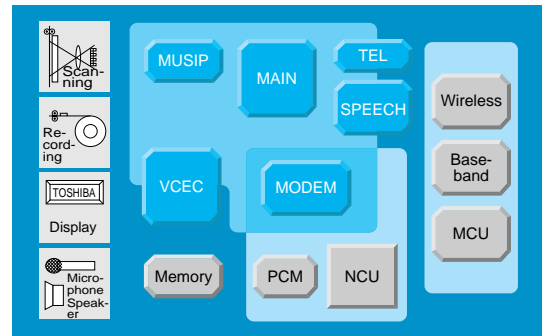
Single-Chip Facsimile Engine

System Advantages

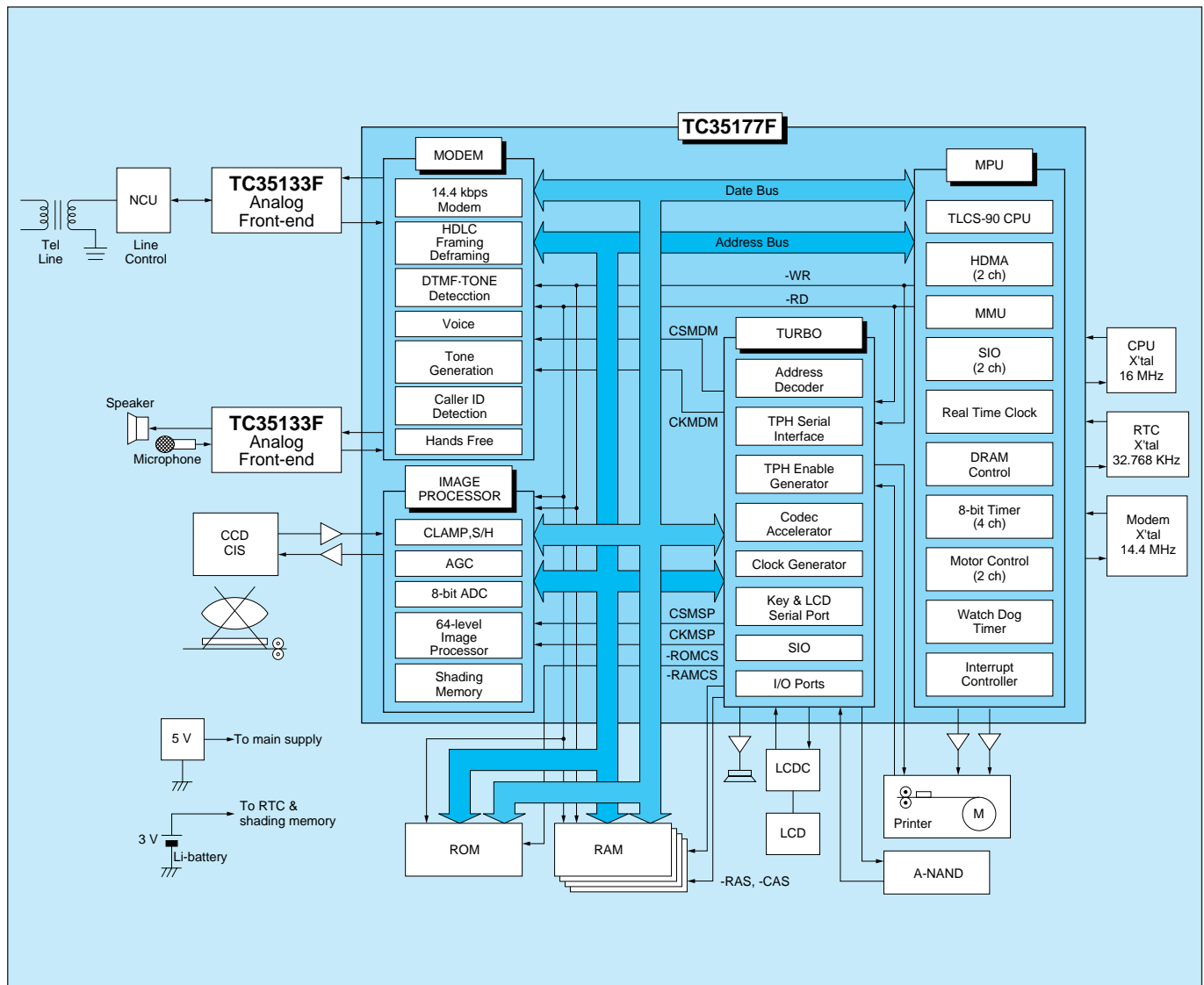
- Shortened system development time → Reduced total cost
- Reduced board area and number of parts → Reduced total cost
- 64 gray scale level image processing → Improved image quality

TC35177F (Enfax™)

The TC35177F (Enfax™) is a facsimile processor that integrates a 14400 bps modem, 64 gray scale level image processor, 8-bit MPU and data compression/expansion circuit that are required by facsimiles. The TC35177F inherits all of the functions of the Enfax™ series plus enhanced answering machine functions, including voice recording and hands-free operation. As a result of integrating all functions required for both inexpensive home machines and more advanced business machines onto a single chip, a system can be easily configured simply by connecting external ROM and RAM to a dedicated front-end IC (TC35133F). Use of this single-chip facsimile processor enables reduction both in the number of parts and in board area, greatly contributing to overall cost reduction.



TC35177F System Configuration





Functions and Overview of the TC35177F

■ 1. Modem

- Compatible with ITU-T G3 facsimile recommendations
- HDLC frame/deframing functions
- Programmable 4-part chord generation
- Programmable 4-frequency simultaneous tone detection
- Programmable DTMF detection and generation
- Programmable carrier detection and transmission levels
- V.21 flag detection when receiving image data
- Compatible with terminals displaying number of local oscillator
- Voice recording/playback functions
(compression rate: 4.3 kbps)
- Hands-free function (full duplex)
- Built-in quadler (clock quadrupling circuit)

■ 2. Image Processor (MUSIP)

- Document sizes: A3, B4, A4
- Full image shading correction (B4, A4 only)
- Error dispersion type, halftone processing function
(64 gray scale level)
- Programmable two-dimensional automatic contrast correction
- Programmable two-dimensional edge emphasis
(binary mode only)
- Programmable automatic background correction
- Built-in line memory
- Built-in 8-bit AD converter, clamp, sample hold and AGC circuit

■ 3. MPU (Equivalent to TMP90C051F)

- Built-in TLCS-90 high-performance 8-bit CPU
- Powerful memory control by MMU
(max 8M bytes)
- High-speed micro-DMA
(2 ch, max 1M byte/sec)
- Interrupt controller
- DRAM controller
- 8-bit timer (4 ch)
- Serial communication interface (2 ch)
- Stepping motor control port (2 ch)
- Built-in watchdog timer
- Built-in real-time clock

■ 4. Peripheral Control Circuit (TURBO)

- Soft CODEC accelerator
- TPH interface
TPH serial interface
TPH strobe signal generator
TPH overheating protective function
- Address decoder
- Clock control circuit
- I/O ports (32 pins, 16 pins can be added using the multiplex system)
- A-NAND interface

| | | |
|-------------|--|--------|
| ☆ TC351700F | Single-chip facsimile (MPU (16-bit) + MODEM (14.4 kbps) + 64 gray scale level image processor + peripheral control circuit + low bit rate voice recording and playback + hands-free) | QFP240 |
| ▲ TC35177F | Single-chip facsimile (MPU + MODEM (14.4 kbps) + 64 gray scale level image processor + peripheral control circuit + low bit rate voice recording and playback + hands-free) | QFP208 |
| ▲ TC35175F | Single-chip facsimile (MPU + MODEM (14.4 kbps) + 64 gray scale level image processor + peripheral control circuit) | QFP208 |
| ▲ TC35162F | Single-chip facsimile (MPU + MODEM (9.6 kbps) + 64 gray scale level image processor + peripheral control circuit + low bit rate voice recording and playback + hands-free) | QFP208 |
| TC35164F | Single-chip facsimile (MPU + MODEM (9.6 kbps) + 64 gray scale level image processor + peripheral control circuit + low bit rate voice recording and playback + hands-free) | QFP208 |
| TC35166F | Single-chip facsimile (MPU + MODEM (9.6 kbps) + 64 gray scale level image processor + peripheral control circuit) | QFP208 |
| TC35167F | Single-chip facsimile (MPU + MODEM (9.6 kbps) + 32 gray scale level image processor + peripheral control circuit) | QFP208 |
| TC35165F | Single-chip facsimile (MPU + MODEM (9.6 kbps) + 16 gray scale level image processor + peripheral control circuit) | QFP176 |
| TC35189F | TC35167F dedicated halftone image coprocessor using Toshiba's original error dispersion method (32 gray scale level) | QFP60 |
| TC35133F | Analog Front-end (AD, DA) for single-chip facsimile | SOP16 |
| TC35123F | | SOP16 |

▲: New product ☆: Under development

Single-Chip MODEM

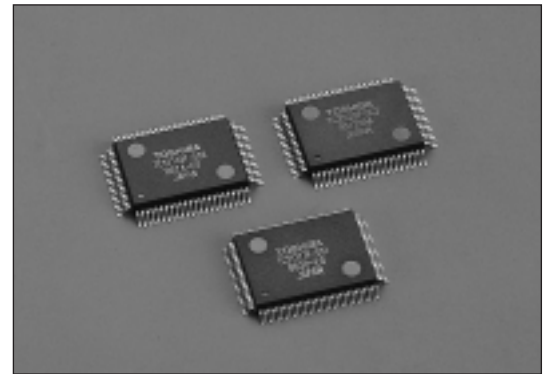
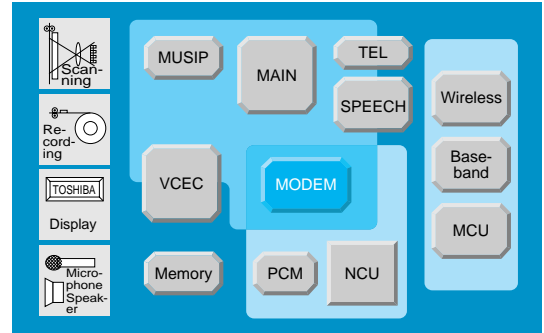


System Advantages

- Compatible with speeds up to 14.4 kbps
- Enhanced voice recording and playback functions are perfect for facsimiles equipped with answering machine functions
- A fully-digital, full-duplex hands-free system can be composed with a single chip

14400 bps Modem with Low-bit-rate Recording and Playback Functions TC35136F

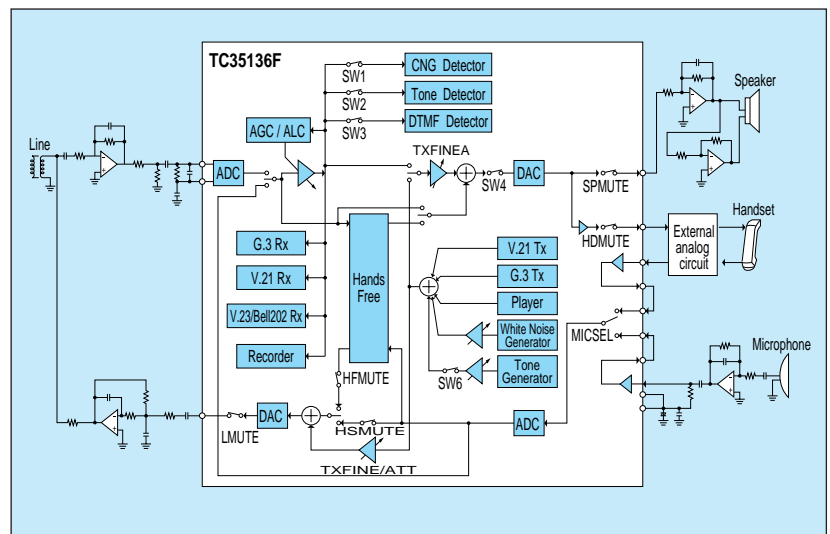
The TC35136F is a 14400 bps single-chip modem for G3 facsimiles featuring built-in recording and playback functions and a hands-free function. In addition to basic functions consisting of communication functions, recording and playback functions and hands-free function, it is also equipped with various additional functions useful for controlling the facsimile communications protocol and telephone answering machine. The bit rate of the recording and playback functions is 4.3 kbps, and allows approximately 16 minutes of recording by connecting 4M bits of external memory. In addition, two types of recording functions are provided consisting of line recording and microphone recording. Line recording can be used for recording of ICM, while microphone recording can be used for recording of OGM (response messages). Moreover, the TC35136F contains two channels of built-in AD-DA converters, enabling the configuration of a hands-free system without connecting an external codec.



Features

- Modem Functions
 - Complies with ITU-T V.17, V.33, V.29, V.27ter, V.21(ch2), T.30 and T.4
 - ITU-T V.23 and BELL202 receive functions (caller ID)
 - HDLC framing/deframing compatible with all transmission rates
 - Simultaneous V.21 preamble detection during high-speed G3 receiving
- Recording and Playback Functions
 - Variable bit rate (4.3 kbps)
 - Mute compression function/trigger recording function (during recording)
 - Mute skip function (during playback)
 - High-speed (1.25 times)/low-speed (0.5 times) playback
 - Simultaneous CNG detection function during playback
 - Simultaneous DTMF detection function in recording/playback mode
- Hands-free Function
 - Fully-digital, full-duplex hands-free operation
 - Level adjustment function
 - Speaker incoming call volume can be set from +9 dB to -12 dB

System Configuration Example



- Additional Functions
 - Quadruplex tone generation
 - Four-frequency simultaneous tone detection
 - DTMF transmission and reception
 - CNG detection function
 - General-purpose I/O ports (16 ch)
- Single +5 V power supply
- 100-pin plastic flat package

Single-Chip Modem Processor Lineup

| Device | V.17 | V.29 | HDLC | DTMF | | Tone | | Hands-free | Built-in analog circuits | Voice recording | | | Caller ID | DTE interface | | Master clock frequency | Process | Package |
|----------|------|------|------|------------|-----------|------------|------------------------|------------|---------------------------|----------------------------|------------------|---------------|-----------|---------------|------------|------------------------|---------|---------|
| | | | | Generation | Detection | Generation | Simultaneous detection | | | Mute compression/mute skip | Compression rate | CNG detection | | Parallel | Serial | | | |
| TC35136F | ○ | ○ | ○ | ○ | ○ | 4 ch | 4 ch | ○ | Line: 1 ch Audio: 1 ch | ○ | 4.3 k | ○ | ○ | ○ | 57.6 MHz | CMOS | QFP100 | |
| TC35127F | - | ○ | ○ | ○ | ○ | 4 ch | 4 ch | ○ | Line: 1 ch Audio: 1 ch | ○ | 4.3 k | ○ | ○ | ○ | 57.6 MHz | | QFP100 | |
| TC35138F | ○ | ○ | ○ | ○ | ○ | 4 ch | 4 ch | - | Line: 1 ch | ○ | 9.6 k/ 6.8 k | ○ | ○ | ○ | 41.472 MHz | | QFP80 | |
| TC35126F | - | ○ | ○ | ○ | ○ | 4 ch | 4 ch | - | Line: 1 ch | ○ | 9.6 k/ 6.8 k | ○ | - | ○ | 41.472 MHz | | QFP80 | |
| TC35129F | - | ○ | ○ | ○ | ○ | 4 ch | 4 ch | - | Line: 1 ch | ○ | 20.736 k | - | - | ○ | 20.736 MHz | | QFP80 | |

ITU-T: International Telecommunication Union-Telecommunication

HDLC: High-level Data Link Control procedures

ECM: Error Correction Mode

Image Processing Circuit



System Advantages

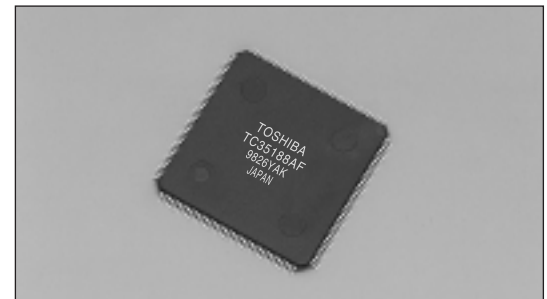
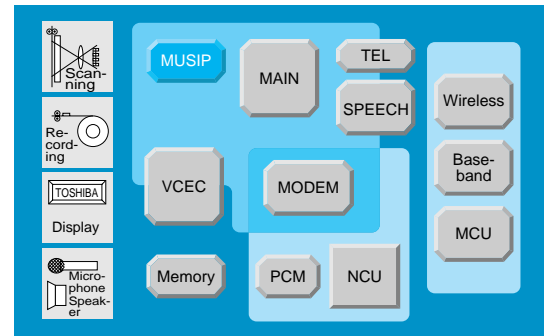
- Compatible with a wide range of sensors
- Built-in analog circuit and SRAM for fewer externally connected components
- High-speed scanning

MUSIP TC35188AF

The TC35188AF is an image scanner processor featuring a built-in 16-bit CPU, 64-gradation image processing circuit using an error diffusion system, and peripheral circuits including UART. In addition to the above circuits, this processor is equipped with a dedicated bus and dedicated controller for transfer of image data to external image memory for high-speed scanning.

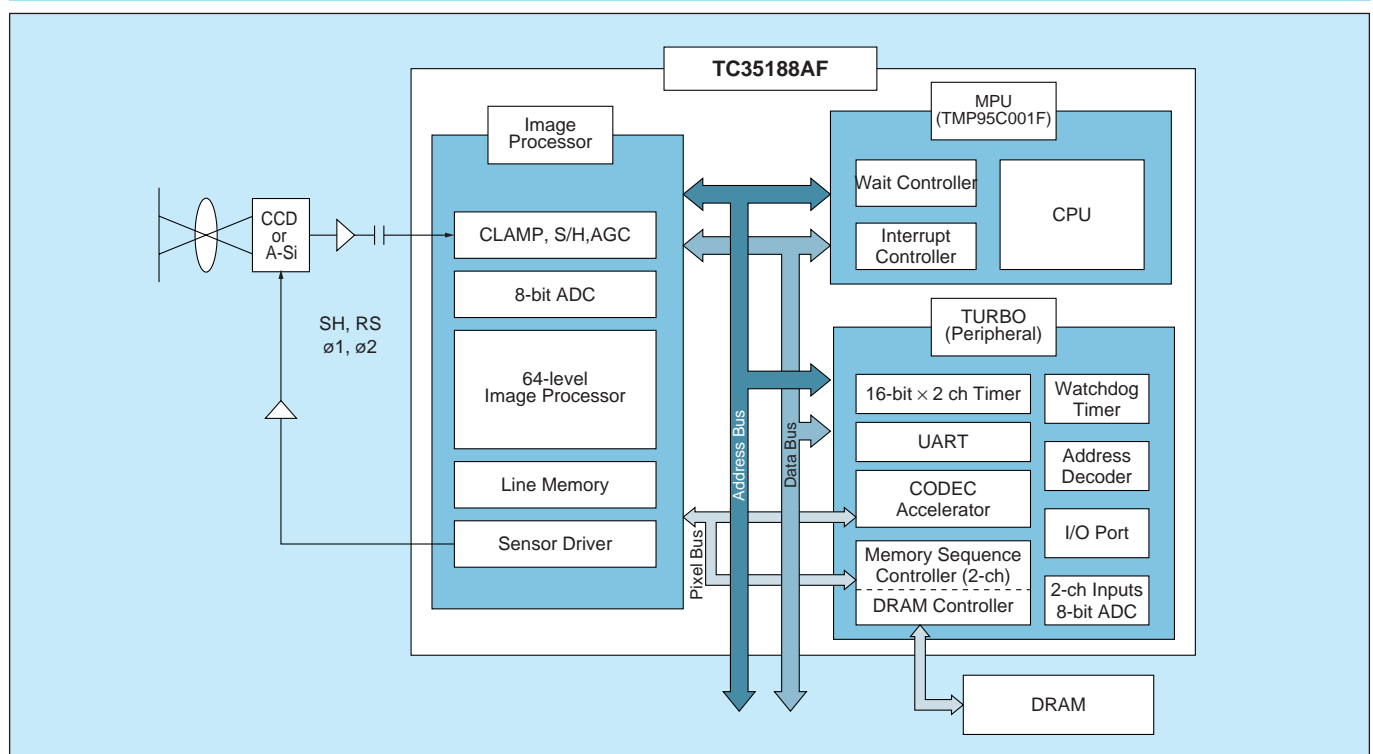
Features of the TC35188AF

- 16-bit CPU (equivalent to TMP95C001F)
 - 16M bytes of linear address space
 - External interrupt inputs: 7 inputs
 - Micro DMA controller: 4 channels
 - Wait controller: 4 blocks
- Image Processing Circuit
 - 64-gradation half-tone processing using a dither method or error diffusion system
 - Correction of shading and sensor output variation for each bit (built-in line memory for shading correction: can be backed up with a battery)
 - Built-in analog circuits (including clamping circuit, S/H circuit, AGC, 8-bit AD converter)
 - γ correction circuit
 - Size reduction function



- Peripheral Circuits
 - MR coding and decoding accelerator
 - DRAM controller and memory sequence controller: 2 channels
 - UART
 - Timer: Selectable between 16 bits x 2 ch and 8 bits x 4 ch
 - General-purpose I/O port
 - 2-input, 8-bit AD converter
 - Watchdog timer

System Configuration Example



| Device | Function | Package |
|-----------|---|---------|
| TC35188AF | MPU + 64 gray scale level image processing + UART + DRAM controller + CODEC accelerator + analog circuits | QFP144 |
| TC35183F | Scanner image processing LSI, analog circuits (6-bit ADC, S/H, clamp, AGC), shading memory | QFP60 |

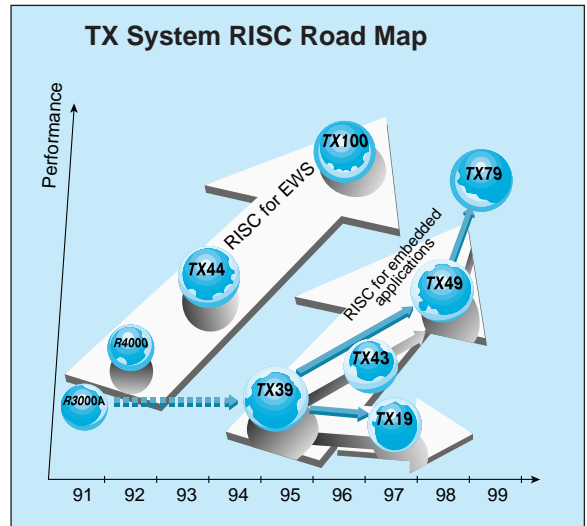
Microcontrollers for Main Control

System Advantages

- Product lineup ranging from low-priced models to intermediate and top-of-the-line models.
- Complete lineup of middleware for enhancing functions.

TX System RISC

Toshiba offers the TX39 family of 32-bit processors for embedded applications, the TX43 series of 64-bit processors for OA equipment, and TX44 and TX100 series of 64-bit processors for high-end workstations by introducing RISC processor technology from the MIPS Group of the US. Moreover, Toshiba also offers the TX19 family, in which a portion of the instruction set is compressed to 16 bits, and the TX49 family of 64-bit microprocessors for embedded applications in its product lineup. The TX19, TX39 and TX49 families provide customers with solutions for ASIC applications in combination with megacells of peripheral circuits in the form of CPU cores.



Family Products



TX19 Series of RISC Microcontrollers with Built-in ROM/RAM

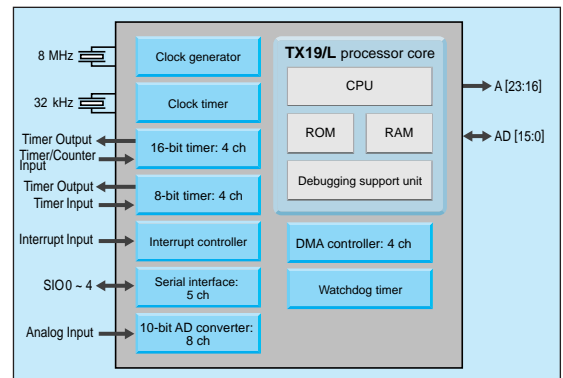
TMP1940CYAF[☆] / FDAF[☆]

☆: Under development

Single-chip 32-bit RISC Microcontrollers for Real-time Control

The TMP1940CYAF/FDAF are 32-bit RISC microcontrollers containing built-in peripheral circuits including DMA controller, timer, serial interface and AD converter based on the TX19/L processor core equipped with built-in high-speed ROM/RAM. As a result of featuring low voltage and low power consumption, these RISC microcontrollers are perfect for battery-powered application equipment including personal and portable information devices.

- Built-in ROM
TMP1940CYAF: Mask ROM 256 kbytes
TMP1940FDAF: Flash memory 512 kbytes
- Built-in RAM
TMP1940CYAF: 10 kbytes
TMP1940FDAF: 16 kbytes
- DMA controller: 4 channels
Memory-to-memory transfer, memory-to-I/O transfer
- Interrupt controller: 12 external factors
- 16-bit timer/counter: 4 channels
- 8-bit timer/counter: 4 channels
- Clock timer
- Serial interface
UART/SIC: 4 channels
I²C bus/SIO: 1 channel
- 10-bit AD converter: 8 channels
- Watchdog timer
- Max operating frequency: 32 MHz



- Power supply voltage: 2.7 to 3.6 V
- 100-pin mini-flat package (14 x 14 mm, 0.5 mm pitch, 1.4 mm thick)

General-purpose MCU

TMPR3901AF-70

32-bit General-purpose RISC Microcontroller Based on the TX39/H Core

The TMPR3901AF contains built-in peripheral circuits including a clock generator and write buffer and is based on the TX39/H high-speed core. In addition to applications as a general-purpose MPU, the TMPR3901AF-70 can also be used for performance evaluation during ASIC development using the TX39/H core and function trial production.

- Instruction cache: 4 kbytes built-in
- Data cache: 1 kbyte built-in
- Clock generator with built-in 8-times PLL
- 4-stage write buffer
- Half-speed bus mode
System bus frequency reduced to 1/2
- Low power consumption mode
Doze/halt mode reduces power consumption during idling
RF function reduces operating frequency
- Built-in debugging support unit
- Max operating frequency: 70 MHz
- Power supply voltage: 3.3 V
- Package: 160-pin QFP

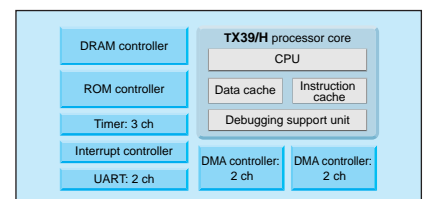
With Built-in Peripheral Functions

TMPR3904AF-66

32-bit General-purpose RISC Microcontroller with Built-in Peripheral Functions

The TMPR3904AF is a 32-bit RISC microcontroller with built-in peripheral circuits including a highly universal memory controller, DMA controller, UART and timer that is based on the TX39/H high-speed processor core.

- Instruction cache: 4 kbytes built-in
- Data cache: 1 kbyte built-in
- ROM controller: Enables 16-bit width setting, compatible with page mode reading
- DRAM controller: Enables 16-bit width setting, high-speed page mode, hyper-page mode
- DMA controller: 4 channels
Memory-to-memory transfer, memory-to-I/O transfer
- Interrupt controller: 8 external factors
- Timer: 3 channels
- UART: 2 channels



- PIO: 8 bits x 3 ports
- Max operating frequency: 66 MHz
- Power supply voltage: 3.3 V
- Package: 208-pin QFP



Family Products

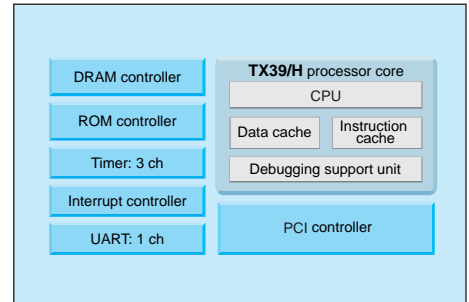


With Built-in PCI Controller TMPR3907F

■ 32-bit General-purpose RISC Microcontroller with Built-in PCI Controller

The TMPR3907F is a 32-bit RISC microcontroller with built-in peripheral circuits including PCI controller, memory controller, UART and timer that is based on the TX39/H processor core. The TMPR3907F uses the high-speed TX39/H core and the processor operates at 66 MHz while the PCI bus operates at 33 MHz.

- Instruction cache: 4 kbytes built-in
- Data cache: 1 kbyte built-in
- PCI controller: 3-slot support
- ROM controller: Enables interleaving operation
- DRAM controller
- Interrupt controller: 3 external factors
- Timer: 3 channels
- UART: 1 channel
- Max operating frequency: 66 MHz
- Power supply voltage: 3.3 V
- Package: 208-pin QFP

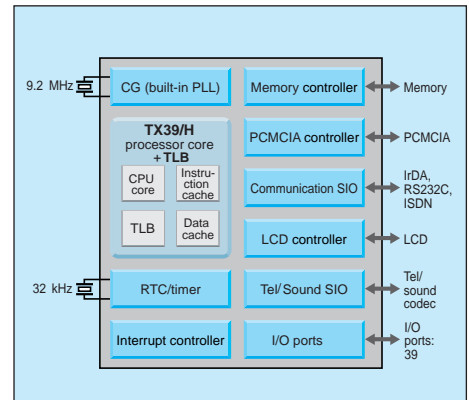


With Built-in Peripheral Functions TMPR3912AU / 3912XB-75 / 3912AU-92 / 3912XB-92

■ 32-bit RISC Microcontrollers with Built-in Peripheral Functions Required for Portable Information Consoles

In addition to integrating peripheral functions required for portable information consoles (PIC) onto a single chip, the TMPR3912AU/XB are ASSP based on the TX39/H processor core that are optimum for PIC having powerful management functions. Use of the TMPR3912AU/XB makes it possible to achieve reduced size, lower costs and higher performance of portable information terminal systems.

- Instruction cache: 4 kbytes built-in
 - Data cache: 1 kbyte built-in
 - Memory management unit (TLB): 32 entries, 4 kbytes page
 - Memory controller: For DRAM (EDO), SDRAM, SRAM, ROM and flash memory
 - Communication interface: For RS232C, IrDA (rev. 1.0) and ISDN
 - PCMCIA interface
 - LCD interface: For monochromatic and color LCDs, max 1024 x 1024 pixels
 - Timer: 2 channels (dedicated RTC) Watchdog timer
 - I/O ports: 39 bits
 - Low power consumption mode: Doze/sleep
 - Max operating frequency: 92 MHz/75 MHz
 - Power supply voltage: 3.3 V
 - Package: 208-pin LQFP (1.4 mm thick) 217-pin FBGA (1.4 mm thick)
- TMPR3912AU: LQFP, 75-MHz version
 TMPR3912XB-75: FBGA, 75-MHz version
 TMPR3912AU-92: LQFP, 92-MHz version
 TMPR3912XB-92: FBGA, 92-MHz version

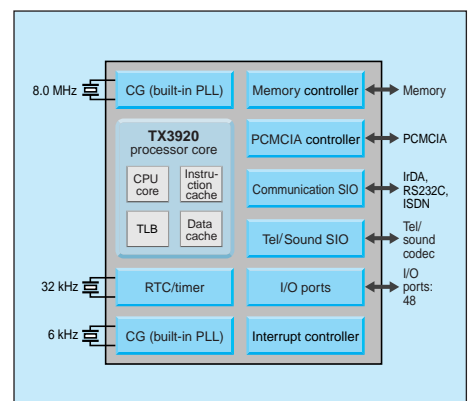


With Built-in Peripheral Functions TMPR3922CU / XB

■ High-performance 32-bit RISC Microcontrollers with Built-in Peripheral Functions

In addition to integrating peripheral functions required for highly functional portable information consoles (PIC) onto a single chip, the TMPR3922CU/XB are ASSP based on the TX3920 processor core that are optimum for highly functional PIC having powerful management functions. Use of the TMPR3922CU/XB makes it possible to achieve reduced size, lower costs and higher performance of highly functional portable information terminal systems and multimedia equipment.

- Instruction cache: 16 kbytes built-in (2-way set associative system)
 - Data cache: 8 kbyte built-in (2-way set associative system)
 - Memory management unit (TLB): 64 entries, 4KB/16KB/64KB/256KB/1 M/4M page
 - Memory controller: For DRAM (EDO), SDRAM, SRAM, ROM and flash memory
 - Communication interface: For RS232C, IrDA (rev. 1.1) and ISDN
 - PCMCIA interface
 - Timer: 2 channels, watchdog timer
 - RTC
 - I/O ports: 48 bits
 - Low power consumption mode: Sleep mode (operation of RTC only), Doze mode (low-frequency operation)
 - Max operating frequency: 129 MHz
 - Power supply voltage: I/O 3.3 V, internal 2.5 V
 - Package: 208-pin LQFP (1.4 mm thick) 217-pin FBGA (1.4 mm thick)
- TMPR3922CU: LQFP, 129-MHz version
 TMPR3922XB: FBGA, 129-MHz version



Microcontrollers for Main Control

Embedded Control Software

Middleware

Toshiba is proceeding with the development of a lineup of middleware products that realize functions conventionally realized with the peripheral LSI of the CPU with software through enhancing the performance and reducing the cost of the CPU. This software lineup is inherited by the TX series in the form of software IP.

Middleware for Communications and PC Interface

Software Modem

This middleware realizes modem functions with a program. The only externally connected circuits are the companion chip in the form of an analog front end (TC35143F) and a DAA circuit. Since the program supports Hayes-compatible AT commands, it makes using conventional resources easy. The functions provided by the software modem are indicated below. Three types are available according to the maximum communication speed (including those under development).

- Data modem function: Up to V.90 (rise 33.6 kbps, fall 56 kbps)
- Fax modem function: Up to V.17 (14.4 kbps)
- Data link layer function: Supports synchronous (HDLC), asynchronous protocol, MNP, LAP-M, V.42 bis
- Other functions: Pulse and tone dialing, ring detection, other

IEEE1394

- Basic shared section (bus management, transaction layer), SBP-2 and AV/C (digital camera) provided.
- Other host protocols will be sequentially made available.
- Able to realize optimum allocation of workload between hardware and software through a link with the hardware IP.
- Dedicated asynchronous link hardware and middleware also available.

USB

- Firmware for standard device requests and printer class requests is provided as a sample program.
- Firmware for other device classes is under development.
- Hardware USB Device which implements Standard Device Requests in hardware is available.

IrDA

- JetBeam™ by Counterpoint systems foundry is supported.
- JetBeam is based on IrDA1.1 (FIR).
- IrTran-P, IrOBEX IrLite, IrMC and JetSend™ are also supported.

Middleware for Processing Based on Image and Voice Multimedia Standards

JPEG (still-image compression / decompression)

Specifications

(conforms to ISO / IEC 10918, Sequential DCT and Baseline)

- Video input/output method: Y, Cb, Cr (4 : 4 : 4, 4 : 2 : 2, 4 : 1 : 1)
- Program size: 9-KB encoder, 7-KB decoder
- Data size: 3-KB encoder, 3-KB decoder
- Execution speed (example): TX39 @70 MHz, Y : Cb : Cr = 4 : 1 : 1, 640 x 480 pixels, compression = 1/10 — encoding time = 0.6 s

MH / MR / MMR ITU-T T.4 and T.6

- Integrated processing using three types of fax codec algorithm
- Encoding or decoding performed using software modules, enabling independent processing
- Multiple module calls possible
- Data input / output control in units of one line
- Execution speed within 0.19 seconds (standard chart 1, TX39@50 MHz)

JBIG ITU-T T.85

Toshiba has developed JBIG having specifications for facsimile applications. This demonstrates outstanding performance particularly for image transfer.

Product Lineup

| | Devices (for domestic use) for GHS compilers | For mass production | | Merits (Remarks) |
|-----------------------------------|--|--------------------------------------|---|--|
| | | TX39-based | TX39X2-based | |
| 1. Multimedia-related | | | | |
| JPEG | IPS3900J0-00FEG0 | Currently available | | Conforms to ISO/IEC10918 and Baseline |
| JBEG | IPS3900K0-00FEG0 | Preparations for release in progress | | ITU-T T.85 |
| MH / MR / MMR | IPS3900H0-00FEG0 | Currently available | | ITU-T T.4, T.6 |
| ADPCM (including PCM) | IPS3900A0-00FEG0 | Preparations for release in progress | | ITU-T G.726 |
| 2. Human I/F | | | | |
| Handwritten character recognition | IPS3901W1-0xFEG0 | Currently available | | 3,363 recognizable characters (Level 1 + a) |
| Voice synthesis (Japanese) | IPS3901S1-0xFEG0 | Currently available | | Pronunciation by deciphering text (140,000 registered words) |
| Voice recognition (Japanese) | IPS3901T1-0xFEG0 | Currently available | | High noise cancellation function + unspecified speaker compatibility + word registration function using text |
| 3. Communication and PC Interface | | | | |
| Software modem V.34 | IPS3902D2-0xFEG0 | — | Currently available | ITU-T V.34 (33.6 kbps), dedicated SIB-compatible CPU V.42LAP-M, MNP4, V.42 bps MNP5-compatible |
| Software modem V.90 | IPS3902D3-0xFEG0 | — | Preparations for release in progress | ITU-T V.90 (fall: 56 kbps), others are the same as above |
| Software modem V.32 | IPS3902D1-0xFEG0 | — | Currently available | ITU-T V.32ter (19.2 kbps), others are the same as above |
| IEEE1394 | IPS3903C1-1xFEG0 | Preparations for release in progress | Development currently under examination | Basic shared section and host protocol (SBP-2, AV/C) |
| IrDA | Please contact to sales office. | Currently available | Development currently under examination | Counterpoint protocol stack |
| USB | Please contact to sales office. | Currently available | Development currently under examination | Sales of host driver, providing of form samples |

Note: X: Variable according to copyright quantity The TX19 and TX49 are scheduled to be sequentially developed.



TLCS-900, 900 / H and 900 / H2 Series of Microcontrollers

The TLCS-900 series consists of 16-bit microcontrollers compatible with a wide range of applications including not only OA equipment and industrial equipment, but also products ranging from facsimiles to consumer devices. For the CPU core, Toshiba offers a complete lineup of products consisting of the TLCS-900/L for low-voltage and low-power-consumption applications, and the TLCS-900/H that emphasizes high performance. What is more, the TLCS-900/H2 is also available as a member of this lineup having twice the level of performance of the TLCS-900/H.

Microcontrollers for Main Control Units

TLCS-900 Series

| Device | ROM (bytes) | RAM (bytes) | Min instruction execution time (ns) | I/O | Operating voltage (V) | Functions |
|-------------|-------------|-------------|-------------------------------------|-----|-----------------------|---|
| TMP96C041BF | None | None | 200 | 47 | 4.5 to 5.5 | SIO/UART 10-bit AD converter Timer, PWM timer CS/WAIT controller |
| TMP96C031ZF | | | | 37 | | |
| TMP96C141BF | | | | 47 | | |
| TMP96CM40F | | | | 65 | | |
| | 32 k | 1 k | | | | |

TLCS-900 / H Series

| Device | ROM (bytes) | RAM (bytes) | Min instruction execution time (ns) | I/O | Operating voltage (V) | Functions |
|---------------------|-------------|-------------|-------------------------------------|-----|----------------------------|--|
| TMP95C001F | None | None | 160 (320) | 0 | 4.5 to 5.5 (2.7 to 3.3) | SIO/UART 10-bit AD converter 8-bit timer/counter 16-bit timer/counter CS/WAIT controller |
| TMP95C061BF | | | 160 | 56 | | |
| TMP95C063F | | | 160 (400) | 91 | | |
| TMP95C265F | | | 167 | 55 | | |
| TMP95CS54F (Note 1) | 64 k | 2 k | 160 (400) | 81 | | |
| TMP95CS64F | | | 160 (400) | | | |
| TMP95CW64F | 128 k | 4 k | 160 | | | |
| TMP95FY64F | 256 k | 8 k | | | | |

TLCS-900 / H2 Series

| Device | ROM (bytes) | RAM (bytes) | Min instruction execution time (ns) | I/O | Operating voltage (V) | Functions |
|----------------------|-------------|-------------|-------------------------------------|-----|-----------------------|--|
| TMP94C241CF | None | 2 k | 50 | 64 | 4.5 to 5.5 | SIO/UART, DRAM controller 10-bit AD converter, 8-bit DA converter |
| TMP94C251AF | | | | 72 | | |
| ☆ TMP94FU81F (Note2) | 96 k | 3 k | | | 2.7 to 3.3 | Timer, CS/WAIT controller |

☆ : Under development

Note 1: Operating voltage: 4.7 to 5.3 V

Note 2: Flash E²PROM products are subject to the patent owned by BULL CP8, US Patent No. 4,382,279

Telephone Function Unit Microcontrollers

TLCS-47 / 470 / 470A Series

| Device | ROM (bytes) | RAM (bytes) | Min instruction execution time (ns) | I/O | Operating voltage (V) | Functions |
|----------------|-------------|-------------|-------------------------------------|-----|-----------------------|----------------|
| TMP47C451BN | 4 k | 768 | 16.7 | 23 | 2.2 to 6.0 | DTMF generator |
| TMP47C452BN/BF | | | | 35 | | |
| TMP47C453AN/AF | | | | 8.3 | | |
| TMP47C853N/F | 8 k | 1 k | | | | |

TLCS-870 Series

| Device | ROM (bytes) | RAM (bytes) | Min instruction execution time (ns) | I/O | Operating voltage (V) | Functions |
|------------|-------------|-------------|-------------------------------------|-----|----------------------------|--------------------------------|
| TMP87CM53F | 32 k | 1 k | 0.50/122 (0.95/122) | 72 | 4.5 to 5.5 (2.2 to 5.5) | DTMF generator AD converter |

TLCS-900 / L Series

| Device | ROM (bytes) | RAM (bytes) | Min instruction execution time (ns) | I/O | Operating voltage (V) | Functions |
|------------|-------------|-------------|-------------------------------------|-----|----------------------------|--|
| TMP93CM40F | 32 k | 2 k | 200 (400) | 79 | 4.5 to 5.5 (2.7 to 3.3) | SIO/UART, 10-bit AD converter Timer, CS/WAIT controller |
| TMP93CS40F | 64 k | | | | | |

TLCS-900 / L1 Series

| Device | ROM (bytes) | RAM (bytes) | Min instruction execution time (ns) | I/O | Operating voltage (V) | Functions |
|-------------|-------------|-------------|-------------------------------------|-----|-----------------------|--|
| TMP91CW12AF | 128 k | 4 k | 150 | 81 | 2.7 V to 3.3 | SIO/UART, 10-bit AD converter Timer, CS/WAIT controller |



System Advantages

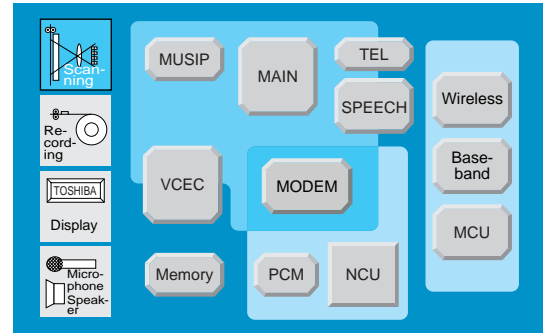
- Uses a non-floating junction type of charge detector
- Uses a new package material

Example: Uses the T-CAPP* (new package) — P Series

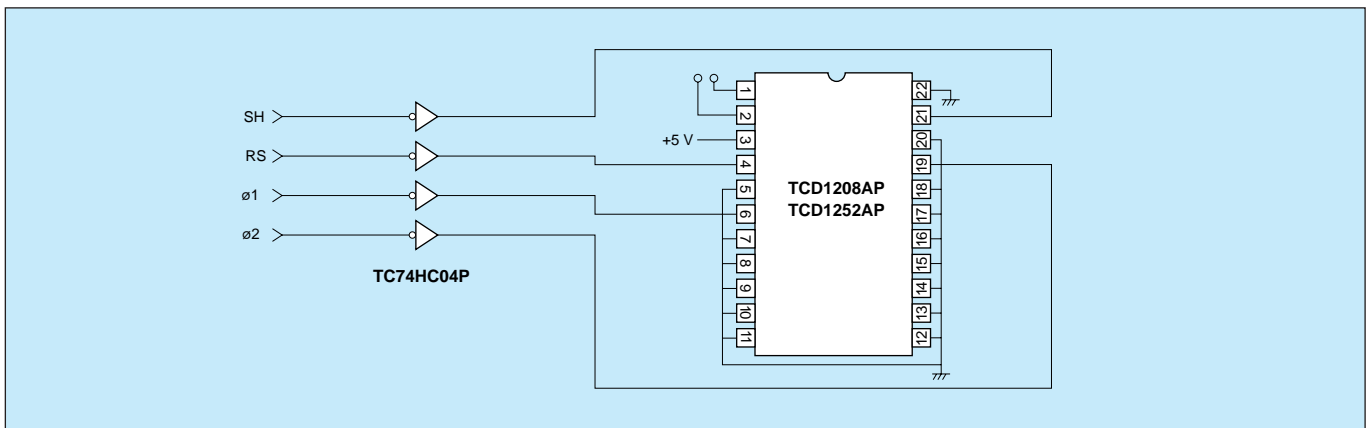
* T-CAPP : TOSHIBA CCD ADVANCED PLASTIC PACKAGE

Reduction-Type CCD Image Sensors

Lens reduction-type CCD image sensors are solid-state image-capturing devices that focus the image on the paper through a lens system onto a row of photodiodes shorter than the width of the paper, one-dimensionally convert the image data into electrical analog signals, and then output the data to a time series. These devices are optimum for application to facsimiles and various types of image scanners.



System Configuration Example



| | Device | Paper size | Resolution (DPI) | Pixels | Pixel size (μm ²) | Package | Remarks (Drive Pulse Voltage) |
|---------------------|---------------|------------|------------------|----------|-------------------------------|-----------------|--|
| Lens Reduction Type | TCD1208AP | B4 | 200 | 2160 | 14 × 14 | WDIP22 (T-CAPP) | High-sensitivity, non-FJ type (5 V only) |
| | TCD1252AP | A4 | 300 | 2700 | 11 × 11 | WDIP22 (T-CAPP) | High-sensitivity, non-FJ type (5 V only) |
| | TCD1501D | A3 | 400 | 5000 | 7 × 7 | WDIP22 | Built-in sample hold circuit |
| | TCD1503D | A3 | 400 | 5000 | 7 × 7 | WDIP22 | High-speed readout |
| | TCD1703C | A3 | 600 | 7500 | 7 × 7 | WDIP22 | High-speed readout |
| | TCD1705D | A3 | 600 | 7450 | 4.7 × 4.7 | WDIP22 | High-speed readout |
| | TCD2255D | A4 | 300 | 2700 × 3 | 8 × 8 | WDIP22 | For color MFP |
| Module | ☆CIPS308BF620 | A3 | 600 | 5340 × 3 | 7 × 7 | WDIP22 | For color MFP |
| | | | | | | — | Digital 8-bit output |

☆ : Under development

Photoelectric Conversion Circuit

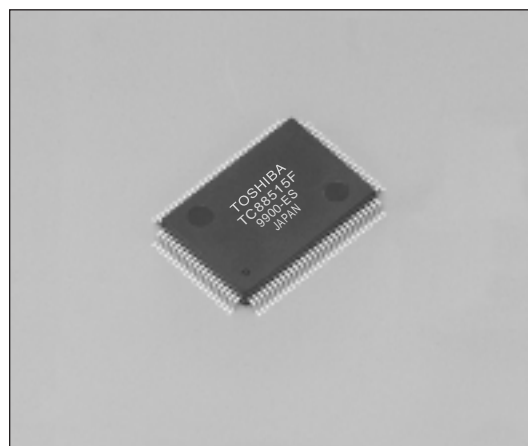
Operation of the Photoelectric Conversion Circuit

The photoelectric conversion circuit is equivalent to the eye of the facsimile, scanning the images on the paper that are to be sent. Light emitted from the light source (LED array) shines onto the paper and is reflected. The energy of this reflected light is converted to an electrical signal by a CCD image sensor. Since the dark portions of the paper have lower reflectance than the light portions, the voltage generated by the sensor is correspondingly lower. Characters and graphics are thus scanned by utilizing this difference in reflectance.



TC88515F — Voice Codec LSIs with Answering Machine Functions

The TC88515F is an LSI for fully digital telephone answering devices (DTAD). In addition to the DSP unit responsible for handling voice recording and playback, full-duplex hands-free functions, FSK demodulation functions and ruled synthesis functions, this single-chip voice codec IC features a Δ - Σ type AD-DA converter, 8-bit CPU for controlling the system, program ROM for the CPU and memory interface. Moreover, it also contains all of the built-in processing functions required for telephone answering devices, including DTMF / tone detection functions and various types of tone output functions. This LSI is also capable of realizing voice-recorded announcement of the caller by combining the FSK demodulation and ruled synthesis functions. In addition, a low-power-consumption system can be operated using standby function.



Features

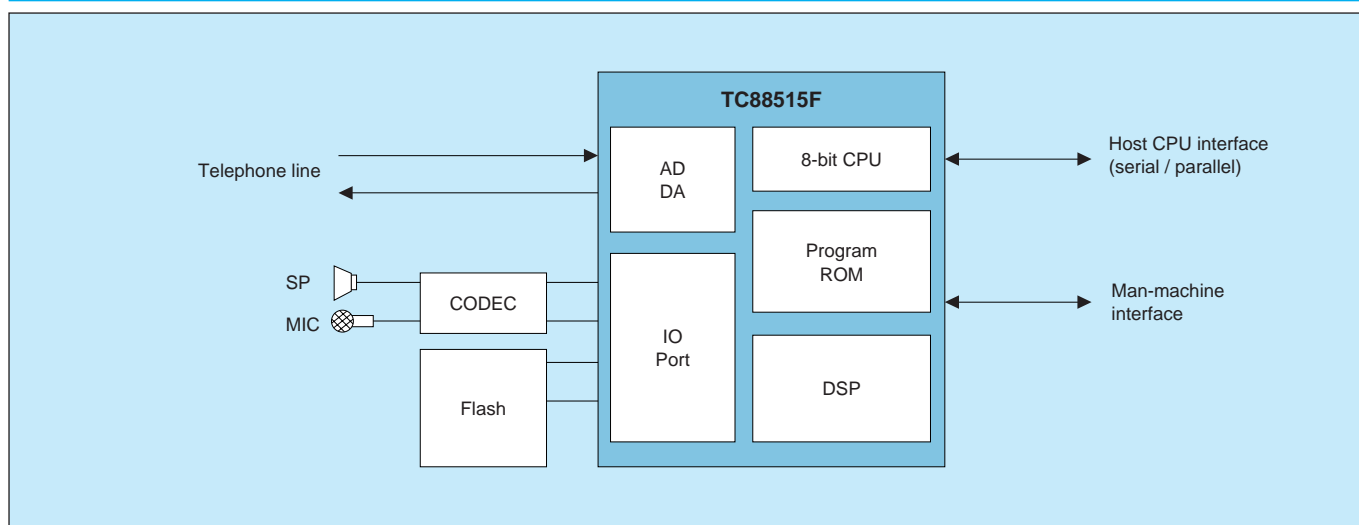
- 4.3 kbps Voice Compression and Restoration

The use of Toshiba Proprietary CELP-based voice compression algorithm allows 15 minutes of voice recording by connecting a single 4M-bit memory device.

- Ruled Synthesis

Natural synthetic voice sounds are output while adding accent automatically by using character data of names registered in the telephone directory. In addition, voice announcement functions can be achieved by combining with preset words.

System Configuration Example



Telephone Answering Device Function Voice Codec LSI Lineup

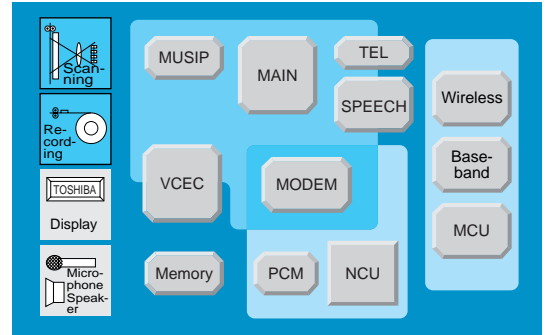
| Product name | TC88512AF | TC88513AF | TC88514AF | TC88515F |
|---------------------------------------|---------------|---------------|---------------|---------------|
| Built-in program ROM | ○ (18 KB) | ○ (18 KB) | ○ (18 KB) | ○ (24 KB) |
| Voice compression/restoration | 4.3 kbps | 4.3 kbps | 4.3 kbps | 4.3 kbps |
| DTMF receiver | ○ | ○ | ○ | ○ |
| Tone output/detection | ○ | ○ | ○ | ○ |
| Full-duplex hands-free function | ○ | — | ○ | ○ |
| FSK demodulation (caller ID) function | — | ○ | ○ | ○ |
| Ruled synthesis function | — | — | — | ○ |
| Operating range | 5 V ± 5% | 5 V ± 5% | 5 V ± 5% | 5 V ± 5% |
| Package (pitch: mm) | QFP100 (0.65) | QFP100 (0.65) | QFP100 (0.65) | QFP100 (0.65) |

Mechanical Control Circuit



Motor Control

A motor is used in facsimiles for the mechanisms of the document scanning and recording units. A stepping motor is frequently used in the document scanning unit for advancing documents to be sent through the device. Although heat-sensitive systems are the most common type of system used in the recording unit, there has recently been an increase in the use of laser systems, resulting from the reduced sizes and lower prices of laser systems. In the case of heat-sensitive systems, a stepping motor is frequently used for advancing the recording paper, while brush motors are often used for the paper cutter. In the case of laser systems, a brushless motor for the polygon mirror used for laser scanning, a brushless motor and brush motor for the drum, and a stepping motor for advancing the paper are used.



TB62201AF Microstep Drive Dual Stepping Motor Driver (New Product)

The TB62201AF is a chopper type, microstep pseudo sine wave drive dual stepping motor driver. This motor driver employs SIPO for the input system and is capable of microstep driving of two 2-phase bipolar type stepping motors with six control ports. The Power MOS FET outputs realizes low loss driving. In addition, a built-in mixed decay mode, which switches the attenuation ratio during chopping, enables improved current-following characteristics during microstep driving.

Features

- Monolithic IC employing a HV-BiCMOS (Power MOS) process
- Low on resistance: $R_{DS(on)} = 0.5 \Omega$ (@ $T_j = 25^\circ\text{C}$, 1.0 A: typ.)
- Two sets of built-in 4-bit D/A converters for microstep driving
- Built-in protective circuits consisting of TSD, V_{DD} and V_M power supply monitoring (reset) circuits, ISD (Over Current protect)
- Built-in charge pump circuit (externally connected condensers x 2)
- Package: 36-pin power flat package (HSOP36-P-450-0.65)
- Built-in mixed decay mode, it can be selecting from 4 stage of Decay Levels.
- Chopping frequency can be set by an externally connected resistor and capacitor for high-speed chopping at 100 kHz or higher

Maximum Ratings ($T_a = 25^\circ\text{C}$)

| Item | Symbol | Rating | Unit |
|--|-----------|----------------|------------------|
| Logic power supply voltage | V_{DD} | 7 | V |
| Output voltage | V_M | 40 | V |
| Output current | I_{out} | 1.5 (*1) | A/phase |
| Current detection pin voltage | V_{RS} | $V_M \pm 1.5V$ | V |
| Charge pump pin max voltage (CCP1 pin) | V_H | $V_M + 7.0$ | V |
| Logic input voltage | V_{IN} | $V_{DD} + 0.4$ | V |
| Power dissipation | P_d | 1.4 (*2) | W |
| | | 3.2 (*3) | W |
| Operating temperature | T_{opr} | -40 to 85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -50 to 150 | $^\circ\text{C}$ |

*1: Maximum peak current
*2: Driver alone

*3: When mounted on a board (90 x 230 x 1.6 mm) ($T_a = 25^\circ\text{C}$)

Motor Driver ICs for Facsimiles

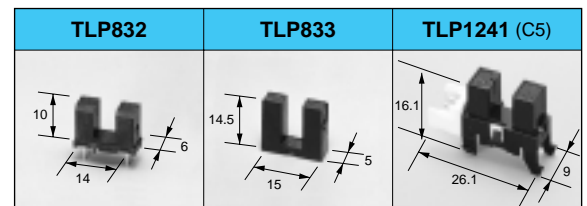
| Device | Functions | Features | Max rating | | Package |
|------------------------|---|--|--------------|-------------------------------------|---------------|
| | | | V_{CC} (V) | I_o (A) | |
| TA8411L | Facsimile system driver IC | Control of the PWM chopper of two bipolar stepping motors and one DC motor control unit with a serial signal | 30 | 0.8 x 2 (stepper) 0.6 (DC motor) | HDIP24 |
| TB6500AH | | | | | HZIP25 |
| TA8415P | Stepping motor driver IC | 3/4-phase, 1-, 2- and 1-2 phase excitation modes, unipolar drive | 7, 28 | 0.4 | DIP16 |
| TA7774P/F | | Bipolar drive | 7, 17 | 0.35 | DIP16/HSOP16 |
| TA7289P/F | | PWM chopper, bipolar drive | 30 | 0.7 | HDIP14/HSOP20 |
| TA8435H | | 2-phase, 1-2 phase, 1-2 phase excitation modes, forward/reverse mode switch, bipolar drive | 5.5, 40 | 2.5 | HZIP25 |
| TB6528P | | 5-phase universal controller | 16 | 0.02 | DIP24 |
| TA8428K(S)/ TA8429H | Bridge driver IC | Single | 30 | 1.5/3.0 | HSIP7/HZIP12 |
| TA7712P | Hall motor driver IC | 3-phase output with external transistor | 8 | 0.025 | DIP20 |
| TA7247AP | | 3-phase output with external transistor | 38 | 1.5 | HDIP20 |
| TA7259P/F | | 3-phase output current control type | 26 | 1.2 | HDIP14/HSOP20 |
| TD62064AP/BP-1/AF/BF | Stepping motor driver IC (unipolar constant voltage type) | 4-phase stepping motor driver Solenoid driver | 50/80/50/80 | 1.5 | DIP16/HSOP16 |
| TD62164AP/BP/AF/BF | | | 50/80/50/80 | 0.7 | DIP16/HSOP16 |
| TD62308AP/BP-1/AF/BF | | | 50/80/50/80 | 1.5 | DIP16/HSOP16 |
| TD62318AP/BP/AF/BF | | | 50/80/50/80 | 0.7 | DIP16/HSOP16 |
| ULN2803/2804AP/AFW | | | 50 | 0.5 | DIP18/SOL18 |
| TD62386 to 388AP/AF | | 50 | 0.5 | DIP20/SOP20 | |
| TD62C851P/852P | | Shift register latch driver | 50 | 0.2/0.5 | DIP20 |

Photointerrupters

Numerous mechanisms are employed within a facsimile, from those for the scanning of transmitted documents to the transport of received documents. Photointerrupters are used as position-detection sensors for these mechanisms. Toshiba offers a lineup of photointerrupters having a photo-transistor output that achieves high conversion efficiency. These photointerrupters are optimal for designs emphasizing low power consumption and long circuit life.

Features

- Numerous types of packages are available (custom packages are also available on request)
- High resolution: 0.5 mm slit width
- High current transfer ratio: $I_C/I_F = 5\%$ (min)
- Recommended models



| Device | Features | Max collector-emitter voltage (V) | Current transfer ratio (%) | | Operating temperature ($^\circ\text{C}$) |
|------------------------------|------------------------|-----------------------------------|----------------------------|-----|--|
| | | | Min | Max | |
| TLP832 | General-purpose type | 35 | 5 | 100 | -30 to 95 |
| TLP833 | Deep slot type (12 mm) | | | | |
| TLP1241 (C5) TLP1242 (C6) | With connector | | | | |

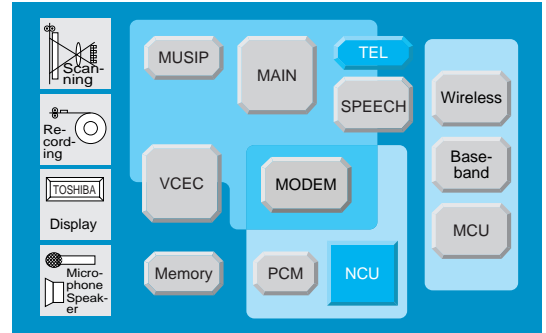
Telephones and NCU Circuits



Single-chip Audio Processing System IC (TB31307AF: Exclusively for facsimile use)

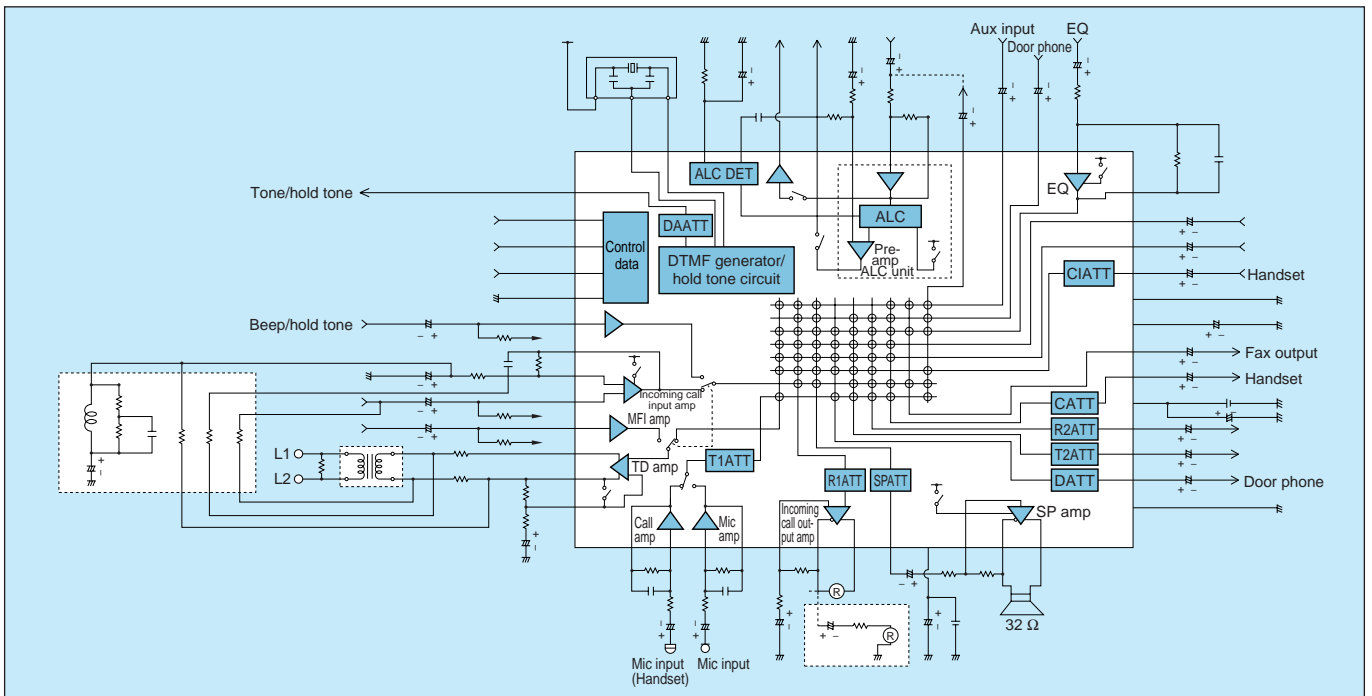
Since the TB31307AF incorporates all audio processing functions required for multi-functional facsimile and other systems in a single chip, inherent functions can be designed easily in a compact form.

| Device | Receiver | SP amp | ALC circuit | Digital ATT circuit | CP SW | DTMF generator circuit | Power supply voltage | Package |
|-----------|---------------------|----------|-------------|---------------------|--------------------------------|-----------------------------------|----------------------|--------------|
| TB31305F | Ceramic and low IMP | For 32 Ω | ○ | 3 paths | 8 inputs, 9 outputs, 45 points | — | 5 V | QFP52 (0.65) |
| TB31307AF | Ceramic and low IMP | For 32 Ω | ○ | 9 paths | 8 inputs, 9 outputs, 55 points | ○ + For 3 scales of hold tones | 5 V | QFP52 (0.65) |



Features

- Compatible with a diverse range of communication lines: Cross point switching (8 inputs x 9 outputs)
- Various built-in functions including DTMF generator/hold tone circuit (for chords: 3 scales), speaker amp (for 16 and 32 Ω), ALC circuit (allowing use of OP amp) and digital ATT circuit (for SP: 0 to -42 dB, other 8 circuits: 0 to -12 dB)
- Various types of control performed with serial data (8-bit)
- Power supply voltage: $V_{DD} = 5\text{ V}$, $V_{SP} = 5\text{ to }8.5\text{ V}$
- Package: 52-pin QFP (pitch: 0.65 mm)



Telephone and Peripheral Semiconductors

Speech Networks

| Device | Receiver | Pad control | Branch performance | MF/Beep input | SP amp | Circuit switching side tone | Package |
|-----------|---------------------------------|------------------------|--------------------|---------------|--------|-----------------------------|---------|
| TA31065N | Ceramic and low impedance types | Linear variable system | Excellent | ○ | — | — | SDIP20 |
| TA31065FA | | | | ○ | — | — | SSOP24 |
| TA31062N | | | — | MF only | ○ | ○ | SDIP36 |

Tone Ringers

| Device | Output form, other | Control method | Oscillation starting voltage | Package |
|--------------|---|--|------------------------------|--------------|
| TA31002P/F | Single output | Variable oscillating starting current type | 19 V | DIP8/SOP8 |
| TA31002AP/AF | | | 16 V | DIP8/SOP8 |
| TA31075AS/AF | Differential output, high sound pressure type | Variable oscillating starting current type | 11 V | SSIP9/SSOP10 |
| TA31076S/F | Single output, allowable operating voltage: 50 V, built-in ring detect function | | 12.4 V | SSIP9/SSOP10 |

Speaker Amps

| Device | Functions and Features | Operating voltage | Output power $R_L = 8\ \Omega$ | Package |
|------------|--|-------------------|--------------------------------|-------------|
| TA31056P/F | Low voltage operation | 1.5 V | 1 V | DIP8/SOP8 |
| TA7331P/F | Low current consumption speaker amp (using a bootstrap system) | 3 V | 0.12 W | SIP9/SSOP16 |
| TA7368P/F | Fewer externally connected components (min. 2), low current when no signals are received | 3 / 6 V | 0.08 W* / 0.45 W | SIP9/SSOP10 |
| TA7376P | Fewer externally connected components, built-in ripple filter | 3 V | 0.21 W (using BTL) | SIP9 |

*: $R_L = 4\ \Omega$, 0.12 W



Dialer Microcontrollers

| Device | Functions and Features | | | | | | | | | | Operating voltage | Operating temperature | Package |
|---------------|------------------------|-------|--------|---------------|--------|--------|------------|------------------|--------------|-------------------------------|-------------------|-----------------------|--------------------|
| | DTMF | Pulse | Redial | Mixed dialing | Memory | Muting | | Tone output time | Binary input | 2 of 8 keyboard compatibility | | | |
| | | | | | | DTMF | Pulse | | | | | | |
| TC35218P/F | ○ | — | — | — | — | — | — | — | ○ | ○ | 2.0 to 5.5 V | -40 to 85°C | DIP18/SOP20 |
| TC35219P/F/FS | ○ | — | — | — | — | — | All digits | — | Variable | ○ | | | DIP14/SOP14/SSOP16 |

Tone Receivers

| Device | DTMF decoding | | Dynamic range | Sensitivity time setting | Momentary interruption protection time setting | Operating voltage | Operating temperature | Package |
|------------|--------------------|--------|---------------|--------------------------|--|-------------------|-----------------------|---------|
| | Binary hexadecimal | 2 of 8 | | | | | | |
| TC35300BP | ○ | ○ | 34 dB or more | Externally connected CR | 4.75 to 5.25 V | -40 to 85°C | DIP18 | |
| TC35301BP | ○ | — | | Digital timer | | | | |
| TC35310F | ○ | ○ | | Externally connected CR | | | | |
| TC35311F | ○ | — | | Digital timer | | | | |
| TC35302P/F | ○ | — | 31 dB or more | Externally connected CR | 4.5 to 5.5 V | -40 to 85°C | DIP18/SOP20 | |
| TC35305P/F | ○ | — | 30 dB or more | Digital timer (fixed) | | | DIP14/SOP14 | |

Tone Detectors

| Device | Functions and Features | Power-down | Operating voltage | Operating temperature | Package |
|----------|---|--------------|-------------------|-----------------------|---------|
| TC35306P | Detection of tones at 305 to 640 Hz over a dynamic range of -40 to 0 dBm, and conversion to digital waveforms | Provided | 4.75 to 5.25 V | -10 to 70°C | DIP8 |
| TC35307P | | Not provided | | | |

NCU Circuits

In NCU circuits, transistor couplers are used for detection of incoming calls from the telephone line, high voltage-resistant Darlington transistor couplers or photorelays are used for generation of dial signals, photorelays are used for line switching, and rectifiers are used for polarity switching and in the protective and backup circuits of LSIs.

Photocouplers (NCU-compatible) Features

| Application | Package | Device | | Features |
|--------------------------------|-------------------|----------------|----------|--|
| | | DC input | AC input | |
| Incoming call detection | 4-pin DIP | TLP521-1 | TLP620 | Transistor output |
| | 8-pin, 2 circuits | TLP521-2 | TLP620-2 | |
| | Mini-flat | TLP281, TLP181 | TLP280 | |
| Dial switching, hook switching | 4-pin DIP | TLP627 | — | High collector voltage-resistant Darlington transistor output |
| | Mini-flat | TLP127 | — | High collector voltage-resistant transistor output |
| | 4-pin DIP | TLP628 | — | |
| | 4-pin DIP | TLP227G | — | MOSFET output photorelay |
| | 4-pin SOP | TLP176G | — | |
| Local line monitoring | 4-pin DIP | TLP629 | TLP320 | LED input current rating $I_f = 150$ mA allowing serial connection to the line |

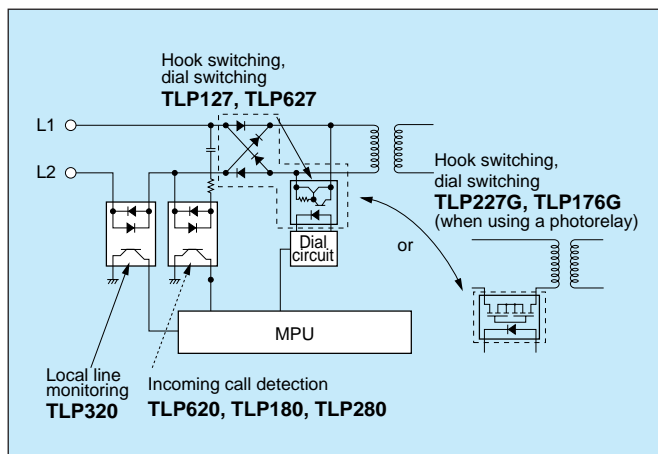
Zener Diodes (for Surge Absorption)

| Device | Power dissipation | Surge power | Zener Voltage (V) | Package |
|-------------|-------------------|-------------|-------------------|--------------|
| 1Z series | 1 W | 400 W | 6.2 to 390 | DO-15 |
| 1ZB series | 1 W | 400 W | 6.5 to 390 | DO-41SS |
| U1ZB series | 1 W | 400 W | 12 to 390 | I-FALT (SMD) |

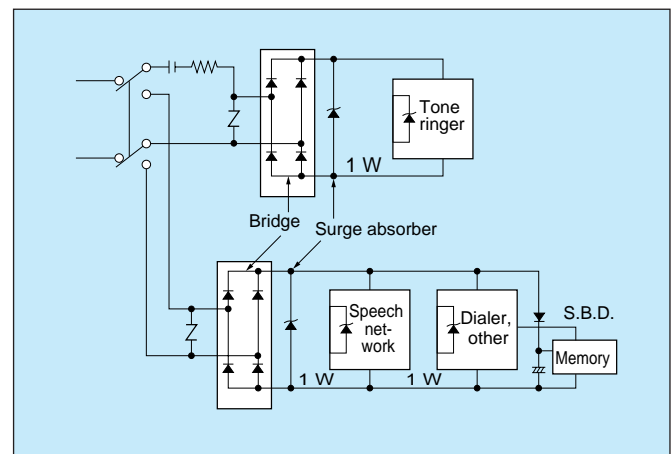
Zener Diodes (for Constant Voltage Circuits)

| Device | Power dissipation | Zener Voltage (V) |
|-------------|-------------------|-------------------|
| 02CZ series | 200 mW | 2 to 39 |
| 02DZ series | 200 mW | 2 to 24 |
| 1ZC series | 1000 mW | 12 to 120 |

Photocoupler System Configuration Example



Rectifier System Configuration Example



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