

TOSHIBA CMOS GATE ARRAY

FEATURES

The Toshiba CMOS Gate Array families are developed by the master slice method on the foundation of Toshiba's famous and proprietary HC²MOS and VLSI technologies.

The product lines are impressive. There are 6 types of base array, with gate complexity of 880 to 6K, in the TC15G series. The TC17G series comprises 9 types of base array, with gate complexity between 540 and 10K. The TC19G series, 5 base arrays of 3200 to 10K.

The great variety of I/O pads provided assures an extensive range of possible applications. For instance, for the smallest base array (540 gates), there are 52; and

for the largest base array (10K gates), there are 232.

These internal gates and I/O pads are wired in accordance with the logic design decided by the individual. These are what give these gate arrays their power and performance.

The LSI design is fully supported by famous LDS-II™, LDS-III™ and Toshiba CAD system. It is capable of executing design verification, logic simulation and auto place and route, having sub-systems for generating mask tapes and test tapes and for performing path analysis. Thus, a customer can develop an ASIC in a short time at a relatively low cost.

LDS-II, LDS-III are trademarks of LSI Logic Corp.

Basic Characteristics

Product line-up	*TC15G series	*TC17G series	TC19G series
Process-technology	3μm	2μm	1.5μm
	HC ² MOS Si-gate double layer metal		
Maximum toggle frequency	50MHz	100MHz	120MHz
Gate speed (inner gate, typ.)	2.5ns	1.5ns	1.0ns
Supply voltage	5V		
Application	LSTTL/ALSTTL	STTL	ASTTL

* TC15G/17G series are alternately-sourced by LSI Logic Corp.

Product Lines

	Part Number	Gate Complexity	Maximum Pads ¹⁾		Maximum I/O Pads ¹⁾	
			Standard pitch	Fine pitch	Standard pitch	Fine pitch
TC15G series ²⁾	TC15G008	880	74	/	70	/
	TC15G014	1,400	92		88	
	TC15G022	2,200	114		110	
	TC15G032	3,200	138		134	
	TC15G042	4,200	156		152	
	TC15G060	6,000	180		176	
TC17G series ²⁾	TC17G005	540	47 ³⁾	55 ³⁾	44	52
	TC17G008	880	52	71 ³⁾	46	68
	TC17G014	1,400	68	89 ³⁾	62	86
	TC17G022	2,200	82	109 ³⁾	76	106
	TC17G032	3,200	98	128	92	122
	TC17G042	4,200	118	150	112	144
	TC17G060	6,000	146	186	140	180
	TC17G080	8,000	174	222	168	216
	TC17G100	10,000	180	232	174	226
TC19G series	TC19G032	3,200	98	128	92	122
	TC19G042	4,200	118	150	112	144
	TC19G060	6,000	146	186	140	180
	TC19G080	8,000	174	222	168	216
	TC19G100	10,000	180	232	174	226

Notes: 1. Additional I/O pads may be configured as V_{DD}/V_{SS}, subject to number and drive of output buffers.

2. Alternately-sourced by LSI Logic Corp.

3. Includes 3 evaluation pads which cannot be configured as power pads.

CAD System Features

Integrated Design System using Macrocell library for:

- Functional design
- Logic design
- Auto place & route
- Test pattern generation

Hierarchical design using:

- Macrofunctions (which consist of Macrocells)

Maximum circuit size: ● 10K gates

Timing verification of critical paths and safe margin check by Toshiba Delay Path analysis System (TDPS)

Automatic test pattern generation

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DESIGN & DEVELOPMENT

Development Flow & Customer Interface

	Functional & logic design	Network entry	Verify design	Functional & timing simulation	Verify node coverage	Auto place & route	Re-simulation	PG & MASK tooling
Interface level	Level 1	→						
	Level 2	→	→	→	→			
	Level 3	→	→	→	→	→		
	Level 4	→	→	→	→	→	→	

Notes: (1) At level-2, design procedure takes place by customer at Toshiba LSI Design Center and at customer site for level-3.
 (2) The EWS interface such as LOGICIAN^{TM3}, IDEA Series^{TM4}, SCALSystem^{TM5}, HP EDS⁸, DASH^{TM6} and Workview^{TM7} is available.

In the note (2)
 3) to 7) are Trademarks of.
 3) Daisy Systems Corporation.
 4) Mentor Graphics Corporation
 8) is the system of HewlettPackard Corporation.

5) Valid Logic Systems Incorporated
 6) FutureNet Corporation.
 7) Viewlogic Systems Incorporated

Electrical Specifications

Parameter	Symbol	Rating	Unit
DC supply voltage	V _{DD}	-0.3 to +7.0	V
DC input voltage	V _{IN}	-0.3 to V _{DD} + 0.3	V
Input current	I _{IN}	±20	mA
Storage temperature	Tstg	-40 to +125	°C

Recommended Operating Conditions (V_{SS} = 0V)

Parameter	Symbol	Rating	Unit
DC supply voltage	V _{DD}	4.75 to 5.25	V
Ambient temperature	T _a	0 to +70	°C

DC Electrical Specifications Under Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Max.	Unit			
V _{IH}	High Level Input Voltage				V			
	TTL Level		2.2					
	CMOS Level		3.5					
	SCHMITT Trigger		4.0					
V _{IL}	Low Level Input Voltage				V			
	TTL Level			0.8				
	CMOS Level			1.5				
	SCHMITT Trigger			1.0				
I _{IH}	High Level Input Current		-10	10	μA			
	Input Buffer with Pull-down	V _{IN} = V _{DD}	15G	1.0		30		
			17G	10		200		
			19G	10		200		
I _{IL}	Low Level Input Current		-10	10	μA			
	Input Buffer with Pull-up	V _{IN} = V _{SS}	15G	-30		-1.0		
			17G	-200		-10		
			19G	-200		-10		
V _{OH}	High Level Output Voltage		2.4		V			
	Buffer Type	15G				17G	19G	I _{OH} = -2mA
		B18				B18	B14	I _{OH} = -4mA
		B1				B1	B18	I _{OH} = -8mA
		B2 ¹⁾				B2 ¹⁾	B1	I _{OH} = -16mA
	—	—	B2 ²⁾					
V _{OL}	Low Level Output Voltage			0.4	V			
	Buffer Type	15G				17G	19G	I _{OL} = 2mA
		B18				B18	B14	I _{OL} = 4mA
		B1				B1	B18	I _{OL} = 8mA
		B2 ¹⁾				B2 ¹⁾	B1	I _{OL} = 16mA
	—	—	B2 ¹⁾					
I _{oz}	High Impedance Leakage Current		-10	10	μA			
	Output Buffer with Pull-up	V _{OUT} = V _{DD} or V _{SS}	Same as I _{IL} with Pull-up					
	Output Buffer with Pull-down		Same as I _{IL} with Pull-down					
I _{DD}	Quiescent Supply Current	V _{IN} = V _{DD} or V _{SS}		100 ²⁾	μA			

Note: 1) Requires two I/O pads, others unspecified require one.
 2) Customer-Design dependent

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DESIGN DATA (As of Mar., 1988)

Macrocell List (TC15G/17G/19G Series)

Function	Types		
	TC15G	TC17G	TC19G
LOGIC GATE	21	26	26
INVERTER/INTERNAL BUFFER	9	9	9
TRI-STATE INTERNAL BUFFER	5	5	5
LATCH	4	11	11
FLIP-FLOP	7	13	13
DECODER	2	4	4
MULTIPLEXER	3	5	5
INPUT BUFFER	5	17	17
OUTPUT BUFFER	9	14	14
BIDIRECTIONAL INPUT BUFFER	5	6	6
BIDIRECTIONAL OUTPUT BUFFER	7	28	28
OTHERS	0	3	3
Total	77	141	141

Macrofunction List (TC17G/19G Series)

Function	Types	
	LSI Compatible	74HC Series Compatible
ADDERS	6	1
COMPARATORS	6	2
COUNTERS	19	11
DECODERS	10	4
FLIP-FLOPS	—	6
GATES	—	16
MULTIPLEXERS	11	10
REGISTERS	19	16
OTHERS	8	8
Total	79	74

PACKAGE ADAPTABILITY LIST

Package	Part No.	TC15G						TC17G						TC19G									
		008	014	022	032	042	060	005	008	014	022	032	042	060	080	100	032	042	060	080	100		
DIP	16							A															
	18							A															
	24	A	A					A	A	A	A												
	28	A	A					A	A	A	A	A					A						
	40	A	A	A				A	A	A	A	A	A				A	A					
	42	A	A	A				A	A	A	A	A	A				A						
	48	A	A	A				A	A	A	A	A	A				A	A					
	42	A	A	A				A	A	A	A	A	A				A	A					
	64	A	A	A				A	A	A	A	A	A				A						
PGA	64	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
	68	A	A	A	A	A	A		A	A	A	A	A	A	A	A	A	A	A	A	A		
	84		A	A	A	A	A			A	A	A	A	A	A	A	A	A	A	A	A		
	100		A	A	A	A	A				A	A	A	A	A	A	A	A	A	A	A		
	120			A	A	A	A				A	A	A	A	A	A	A	A	A	A	A		
	135				A	A	A					A	A	A	A	A	A	A	A	A	A		
	144				A	A	A					A	A	A	A	A	A	A	A	A	A		
	180					A	A							A	A	A			A	A	A		
	224														A	A				A	A		
PPGA ²⁾	120										A	A	A				A	A	A				
	144												A					A					
MPGA ²⁾	120									P	P	P	P				P	P	P				
	144										D	D	D				D	D	D	D	D		
CD ²⁾ PGA	95																P	P			P	P	
	155																P	P			P	P	
	223																D	D			D	D	
	299																				D	D	
PLCC	44							D	D	D	D	D	D				D	D					
	68	A	A	A	A			A	A	A	A	A	A	P	P		A	A	A	P	P		
	84		A	A	A					A	A	A	A	P	P		A	A	A	P	P		
PFP	SQUARE	μ44						A	A	A	A												
		44	A	A	A			A	A	A	A	A					A	A					
		60							A	A	A	A	A					A	A				
		100A ¹⁾	A	A							A												
		100 ¹⁾		A	A	A						A	A	A	A	D	D		A	A	A	D	D
	144											A	A						A	A	D	D	
	184																	P	P		P	P	
	REC-TANGULAR	64	A	A	A					A	A	A	A	A					A	A			
80		A	A	A					A	A	A	A	A					A	A				
100			A	A						A	A	A						A	A				
CFP	100 ¹⁾			A	A	A	A						A	A	A			A	A	A	A	A	
	144					A	A							A	A	A			A	A	A	A	
	184														P	P				P	P	P	

A: Adaptable
D: Check with Toshiba for availability (Under development)
P: Check with Toshiba for availability (Under planning)

Notes: 1) Flat Package 100 pin is classified into 2 types determined by number of inner leads available: 100A—84 inner leads, 100—100 inner leads.
2) PPGA—Plastic PGA, MPGA—Metal PGA, CD PGA—Cavity Down PGA.
3) Please refer to "Package Selector Guide" (Document I.D. SEMI-E-S1001) for further information in detail.

OVERSEAS OFFICES

São Paulo:

Toshiba Brasileira Representacoes Ltda.
Av. Paulista, 807, 21 Andar Cjto 2106,
Cerqueira Cesar.
Cep: 01311-São Paulo-S.P.-Brasil
Tel.: 283-4511, 4714, 4964 Fax: (11) 251-4104

Athens:

Toshiba Corporation Athens Office
Athens Tower Bldg. A, 2-4 Mesogion Ave.,
Athens 115-27, Greece
Tel.: 7799828-9, 7791824 Telex: 21-6502 TSBA GR
Cable: TOSHIBA ATHENS

Tehran:

Toshiba Corporation Iran Office
No. 79 Bucharest Ave., 3rd Floor, Argentine
Square, Tehran, Iran
P.O. Box 15745-343, Tehran, Iran
Tel.: 624729 Telex: 212531 TSBAIR
Cable: TOSHIBACO TEHERAN

Beijing:

Toshiba Corporation Beijing Office
Room 1622/1624 Beijing Hotel, Dong Chang An Jie,
Beijing, The People's Republic of China
Tel.: 500-7766 (EX. 1622, 1624, 3857) 55-4179, 4768
(Direct)
Telex: 22807 TOSPK CN Cable: TOSHIBA PEKING

Guangzhou:

Toshiba Corporation Guangzhou Office
Room 609, Office Tower, China Hotel, Liu Hua, Lu,
Guangzhou, The People's Republic of China
Tel.: 663388 (EX. 2609) 677427 (Direct)
Fax: (20) 67-7427 Telex: 44585 TSBGZ CN
Cable: TOSHIBA GUANGZHOU

Shanghai:

Toshiba Corporation Shanghai Office
Room 2705 - 8, Shanghai Union Building Yanan Rd
East/Sichuan Rd., Shanghai, The People's Republic of
China
Tel.: 200156, 200157, 200076 Fax: (21) 200075

Wellington:

**Toshiba Corporation Representative
in New Zealand**
12th Floor, Paxus House, 79 Boulcott Street
P.O. Box 3549, Wellington, New Zealand
Tel.: 721865, 726001 Fax: (4) 731-394
Telex: 3433 TOSHIBA NZ
Cable: TOSHIBA WELLINGTON

Toshiba America, Inc.:

**Electronic Components Business Sector
Irvine Head Office**
(MOS IC Div., Sem conductor Div.)
9775 Toledo Way, Irvine, CA 92718, U.S.A.
Tel.: (714) 455-2000 Fax: (714) 859-3963

Eastern Area Office

(MOS IC Div., Sem conductor Div.)
25 Mall Road, 5th Floor,
Burlington, MA 01303, U.S.A.
Tel.: (617) 272-4351 Fax: (617) 272-3089

South Eastern Regional Office

(MOS IC Div.)
4025 Pleasantdale Rd., Suite 320 Atlanta, GA 30340,
U.S.A.
Tel.: (404) 493-4240 Fax: (404) 493-4401

San Jose Office (Electron Tubes & Devices Div.)

Western Area Office (MOS IC Div.)
2021 The Alameda Suite 220
San Jose, CA 95126, U.S.A.
Tel.: 408-244-4070 Fax: 408-248-5370

Southwestern Regional Office

(MOS IC Div.)
1400 Quail St., Suite 100 Newport Beach, CA 92660,
U.S.A.
Tel.: (714) 752-0373

Chicago Office (Electron Tubes & Devices Div.,
Semiconductor Div.)

Central Area Office (MOS IC Div.)
1101A Lake Cook Rd., Deerfield, IL 60015, U.S.A.
Tel.: (312) 945-1500 Fax: (312) 945-1044

South Central Regional Office

(MOS IC Div.)
1750 North Collins Blvd., Suite # 116
Richardson, Texas 75080, U.S.A.
Tel.: (214) 480-0470 Fax: (214) 235-4114

Poughkeepsie Sales Office

(MOS IC Div.)
RR 1 Box 6E
Windsor Park Fishkill, New York 12524, U.S.A.
Tel.: (914) 896-6500 Fax: (914) 297-2605

Boca Raton Sales Office

(MOS IC Div.)
1200 N. Federal Highway Suite 407
Boca Raton, FL 33432, U.S.A.
Tel.: (305) 394-3004 Fax: (305) 394-3006

Detroit Office

(Automotiv Div.)
26533 Evergreen Road,
Suite 420 Southfield, MI 48076, U.S.A.
Tel.: (313) 827-7700 Fax: (313) 827-4444

Toshiba (UK) Limited

Electronic Components Group
Riverside Way, Camberley,
Surrey GU15 3YA, U.K.
Tel.: 0276-694600 Fax: 0276-691583

Toshiba Electronics Scandinavia AB

Box 438 (VASAGATAN 3) 101 25 Stockholm Sweden
Tel.: 08-145600 Fax: 08-119574
Telex: 14169 (TSB STK S)

Toshiba Electronics Europe GmbH

Düsseldorf Head Office
Hansaallee 181, 4000 Dusseldorf 11,
F.R. Germany
Tel.: (0211) 5296-0 Fax: (0211) 5296-400
Telex: 8582685

Liaison Offices

Stuttgart: Vertriebsbüro Baden-Württemberg
Eltlinger Str. 61
D-7250 Leonberg F.R. Germany
Tel.: (07152) 21061-66 Fax: (07152) 27658
Telex: 7245706

München: Büro München Arabellastr. 33/v
8000 München 81, F.R. Germany
Tel.: (089) 928091-0 Fax: 089-9280942
Telex: 5-212363

Paris: Tour de Bureaux de Rosny,
2, 93118 Rosny, Sous Bois, France
Tel.: 4855-5656 Fax: 4855-5248
Telex: 613351 F TOSPAR

Toshiba Electronics Italiana S.R.L.

Centro Direzionale Colleoni Palazzo Orione-
Ingresso 3 (3° Piano) 20041 Agrate
Brianza (Milano), Italy
Tel.: 039-638891 Fax: 039-638892
Telex: 326423 SIAVBC

Toshiba Electronics Taiwan Corp.

Taipei Head Office
8F, Min Sheng Chen Kou Bldg., 348-350 Min Sheng
East Road Taipei, Taiwan
Tel.: 02-502-9641 Fax: 02-503-7964
Telex: 26874 TETTP

Kaohsiung Office

16F-A Chung-Cheng Building
No. 2 Chung-Cheng 3rd, 80027 Kaohsiung
Tel.: (07) 241-0826 Fax: (07) 282-7446

Toshiba Electronics Asia, Ltd.

Hong Kong Head Office
Suite 501, Hong Kong Hotel, Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel.: 3-671-141 ~ 4, 3-721-6111 Fax: 3-739-8969
Telex: 38501 TSBEH HX

Seoul Branch Office

Room 1061, Chamber Building, 45, 4-KA
Namdaemun-Ro, Chung-Ku, Seoul, Korea
Tel.: (2) 757-2472 ~ 3 Fax: (2) 757-2475

Singapore Branch Office

460 Alexandra Road #26-01, PSA Bldg.,
Singapore 0511
Tel.: 2785252 Fax: 2735368
Telex: RS 23892 TOSHIBA

Toshiba (Australia) Pty, Ltd.

84-92 Talavera Road, North Ryde, N.S.W. 2113
Australia
Tel.: (2) 887-3322 Fax: 2-887-3201 Telex: AA27235

MANUFACTURING SUBSIDIARIES AND JOINT VENTURES

Toshiba America, Inc.

Microelectronics Center
1220, Midas Way, Sunnyvale, CA 94086, U.S.A.
Tel.: 408-739-0560 Fax: 408-746-0577
Telex: 346378

Toshiba Westinghouse Electronics Corporation

Westinghouse Circle, Horseheads, New York
14845, U.S.A.
Tel.: (607) 796-3500

Industria Mexicana Toshiba, S.A.

Calzada de Guadalupe, No. 303, Cuatitlan,
Edo de Mexico, Mexico
Tel.: 5-65-00-88 Telex: 017-72-560
Cable: Toshiba Mexico

Semp Toshiba Amazonas S.A.

Rua Ica No. 500, Distrito Industrial de Sufrema, Manaus,
CEP 69000, Amazonas, Brazil
Tel.: (092) 237-2366
Telex: 38922197 SEMP BR Cable: SEMP AMAZON

Toshiba Semiconductor G.m.b.H.

Grottrian-Steinweg Str. 10, 3300
Braunschweig, F.R. Germany
Tel.: (0531) 31-0060 Fax: (0531) 31006139
Telex: 952368 TSCD

Toshiba Electronics Malaysia Sdn. Bhd.

42057 Telok Panglima, Grang, 15KM Klang-Banting
road, Kuala Langat Selangor, Malaysia
Tel.: 03-352-6001-7 Fax: 03-352-6139
Telex: TOEL MA 39506

Penang Branch Office

Lot 2.08 2nd Floor, Wisma Chocolate Products,
41 Adoo Sittle Lane Penang 10400 Malaysia
Tel.: 04-368523, 04-368529 Fax: 04-368515

Toshiba Singapore Pte Ltd.

20 Pasir Panjang Road, 09-18/26 PSA Multi-Storey
Complex, Singapore 0511
Tel.: 2718066 Telex: RS 36592 TSPMFG

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TOSHIBA

TOSHIBA CORPORATION
INTERNATIONAL OPERATIONS—ELECTRONIC COMPONENTS

1-1 SHIBAURA 1-CHOME, MINATO-KU, TOKYO, 105, JAPAN
Tel.: 457-3495 Fax: 451-0576 Telex: J22587 TOSHIBA
CABLE: TOSHIBA TOKYO