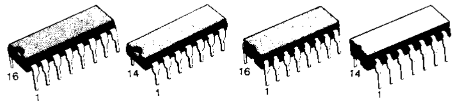
DUAL DECADE COUNTER
DUAL 4-STAGE BINARY COUNTER

DESCRIPTION

The T54LS/T74LS390 and T54LS/T74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two section can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50% duty cycle) at the final output.
Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.



B1
Plastic Package

D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

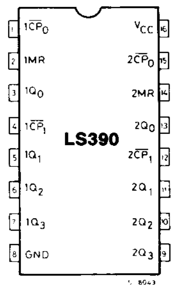
ORDERING NUMBERS:

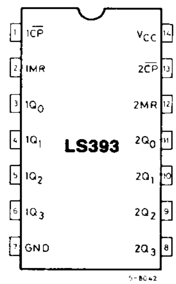
T54LSXXX D2
T74LSXXX D1
T74LSXXX B1
T74LSXXX C1
T74LSXXX M1

- DUAL VERSION OF LS290 AND 293
- LS390 HAS SEPARATE CLOCKS ALLOWING ÷2, ÷2.5, ÷5
- INDIVIDUAL ASYNCHRONOUS CLEAR FOR EACH COUNTER
- TYPICAL MAX COUNT FREQUENCY OF 50 MHz
- INPUT CLAMP DIODES MINIMIZE HIGH SPEED TERMINATION EFFECTS

PIN CONNECTION
(top view)

DUAL IN LINE





PIN NAMES

$\overline{CP}$	Clock Active LOW going edge Input to – 16 (LS393)
$\overline{CP}_0$	Clock Active LOW going edge Input to – 2 (LS390)
$\overline{CP}_1$	Clock Active LOW going edge Input to – 5 (LS390)
MR	Master Reset (Active HIGH) Input
Q_0-Q_3	Flip-Flops Outputs

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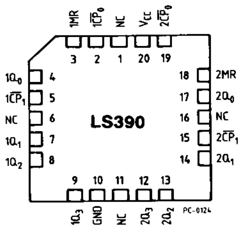
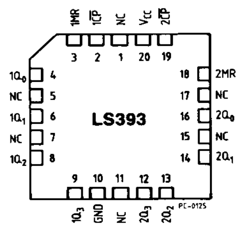
CHIP CARRIER





NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 5.5	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS390/393D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS390/393XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

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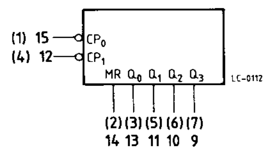
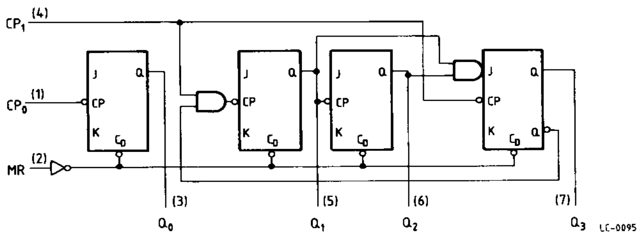
FUNCTIONAL DESCRIPTION

Each half of the LS393 Operates in the Modulo 16 binary sequences, as indicated in the ÷ 16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs for not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.
Each half of the LS390 contains a ÷ 5 section that is independent except for the common MR function. The ÷ 5 section operates in 4.2.1 binary sequence, as shown in the ÷ 5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a ÷ 10 function having a 50% duty cycle output, connect the input signal to CP_1 and connect Q_3 output to the CP_0 input; the Q_0 output provides the 50% duty cycle output. If the input frequency is connected to CP_0 and the Q_0 output is connected to CP_1, a decade divider operating in the 8.4.2.1 BCD code is obtained, as show in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signal derived from combinations of LS390 outputs are also subject to decading spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

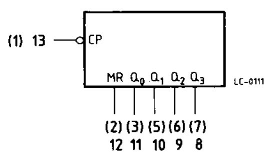
LOGIC SYMBOLS AND LOGIC DIAGRAMS

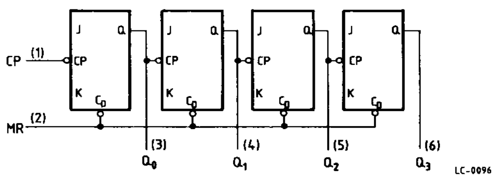
LS390 (one half shown)





LS393 (one half shown)





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TRUTH TABLES

LS390 BCD
(Input on $\overline{CP}_0$; Q_0 $\overline{CP}_1$)

COUNT	OUTPUTS Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS390 ÷ 5
(Input on $\overline{CP}_1$)

COUNT	OUTPUTS Q_3	Q_2	Q_1
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

LS393

COUNT	OUTPUTS Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Typ.	Max.	Test Conditions (Note 1)		Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Theresold		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Theresold		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IL} or V_{IH} per Truth Table		V
		74	2.7	3.4				
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per truth table	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current	$\overline{CP}$.$\overline{CP}_0$ $\overline{CP}_1$ MR			40 80 20	V_{CC} = MAX, V_{IN} = 2.7V		μA
		$\overline{CP}$.$\overline{CP}_0$ $\overline{CP}_1$ MR			400 800 100	V_{CC} = MAX, V_{IN} = 2.7V		μA
I_{IL}	Input LOW Current	$\overline{CP}$.$\overline{CP}_0$ $\overline{CP}_1$ MR			−2.4 −3.2 −0.4	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−120	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current	LS390 LS393		20 20	30 30	V_{CC} = MAX		mA

Notes: 1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the device type.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

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AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0V$

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions	Units
f_{MAX}	Maximum Clock Frequency $\overline{CP}_0$ to Q_0	25	35		$C_L = 15pF$	MHz
f_{MAX}	Maximum Clock Frequency $\overline{CP}_1$ to Q_1	12.5	20			MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_0 LS393		12 13	20 20		ns
t_{PLH} t_{PHL}	$\overline{CP}_0$ to Q_0 LS390		12 13	20 20		ns
t_{PLH} t_{PHL}	$\overline{CP}$ to Q_3 LS393		40 40	60 60		ns
t_{PLH} t_{PHL}	$\overline{CP}_0$ to Q_2 LS390		37 39	60 60		ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ to Q_1 LS390		13 14	21 21		ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ to Q_2 LS390		24 26	39 39		ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ to Q_3 LS390		13 14	21 21		ns
t_{PHL}	MR to Any Input LS390/393		24	39		ns

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions	Units
t_W	Clock Pulse Width LS390	20			$V_{CC} = 5.0V$	ns
t_W	$\overline{CP}_0$ Pulse Width LS390	20				ns
t_W	CP_1 Pulse Width LS390	40				ns
t_W	MR Pulse Width LS390/393	20				ns
t_{rec}	Recovery Time LS390/393	25				ns

RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognized and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

Fig. 1

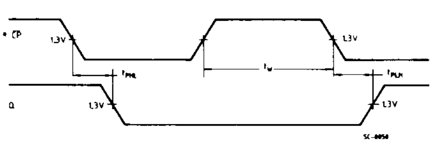
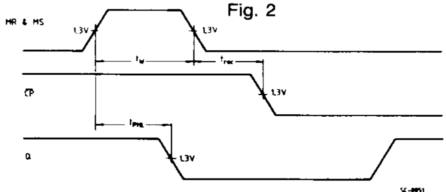


Fig. 2



* The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Table

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