

# SRM2264L<sub>10/12</sub>

## HIGH SPEED CMOS 64K-BIT STATIC RAM

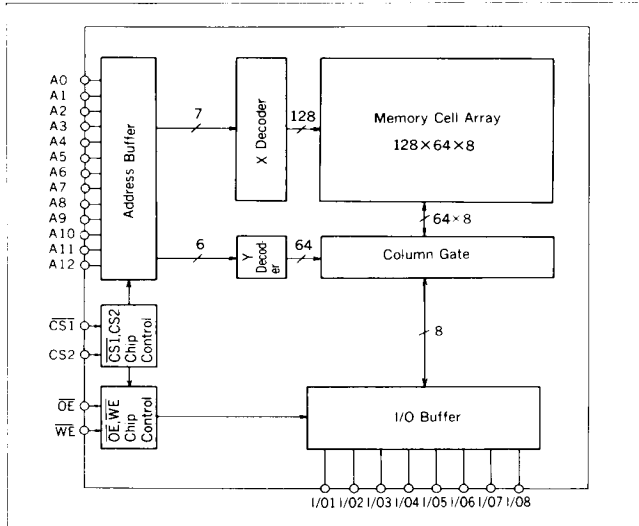
### DESCRIPTION

The SRM2264L<sub>10/12</sub> is an 8,192 words x 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible; and the three-state output allows easy expansion of memory capacity.

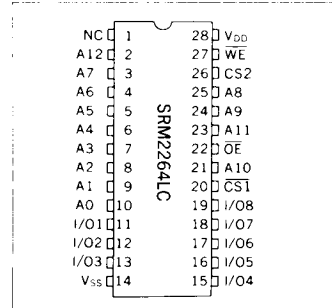
### FEATURES

- Fast access time ..... SRM2264L<sub>10</sub> 100ns (Max)  
SRM2264L<sub>12</sub> 120ns (Max)
- Low supply current ..... Standby : 0.5μA (Typ)  
Operation: 47mA (Typ) ..... 100ns  
45mA (Typ) ..... 120ns
- Completely static ..... No clock required
- Single power supply ..... 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package ..... SRM2264LC<sub>10/12</sub> 28-pin DIP (plastic)  
SRM2264LM<sub>10/12</sub> 28-pin SOP (plastic)

### BLOCK DIAGRAM



### PIN CONFIGURATION



### PIN DESCRIPTION

A0 to A12	Address Input
WE	Write Enable
OE	Output Enable
CS1, CS2	Chip Select
I/O1 to 8	Data I/O
V <sub>DD</sub>	Power Supply(+5V)
V <sub>SS</sub>	Power Supply(0V)
NC	No connection

**ABSOLUTE MAXIMUM RATINGS**(V<sub>SS</sub>=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	-0.5 to 7.0	V
Input voltage *	V <sub>I</sub>	-0.5 to 7.0	V
Input/Output voltage*	V <sub>I/O</sub>	-0.5 to V <sub>DD</sub> +0.3	V
Power dissipation	P <sub>D</sub>	1.0	W
Operating temperature	T <sub>opr</sub>	0 to 70	°C
Storage temperature	T <sub>stg</sub>	-65 to 150	°C
Soldering temperature and time	T <sub>sol</sub>	260°C, 10s (at lead)	—

\* V<sub>I</sub>, V<sub>I/O</sub> (Min) = -1.0V when pulse width is 50 ns(V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>DD</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input Voltage	V <sub>IH</sub>	2.2	3.5	V <sub>DD</sub> + 0.3	V
	V <sub>IL</sub>	-0.3 *	—	0.8	V

**ELECTRICAL CHARACTERISTICS**

\* If pulse width is less than 50 ns, it is -1.0V

**DC Electrical Characteristics**(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	SRM2264L10			SRM2264L12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> = 0 to V <sub>DD</sub>	-1	—	1	-1	—	1	μA
Standby supply current	I <sub>DDs</sub>	CS1=V <sub>IH</sub> or CS2=V <sub>IL</sub>	—	0.5	1.0	—	0.5	1.0	mA
	I <sub>DDs1</sub>	CS1=CS2=V <sub>DD</sub> -0.2V or CS2≤0.2V	—	0.5	20	—	0.5	20	μA
Average operating current	I <sub>DDA</sub>	V <sub>I</sub> =V <sub>IL</sub> , V <sub>IH</sub> I <sub>I/O</sub> =0mA t <sub>avg</sub> =Min	—	47	82	—	45	80	mA
Operating supply current	I <sub>DDO</sub>	V <sub>I</sub> =V <sub>IL</sub> , V <sub>IH</sub> I <sub>I/O</sub> =0mA	—	35	60	—	35	60	mA
Output leakage	I <sub>LO</sub>	CS1=V <sub>IH</sub> or CS2=V <sub>IL</sub> or $\overline{WE}$ =V <sub>IL</sub> or $\overline{OE}$ =V <sub>IH</sub> , V <sub>I/O</sub> =0 to V <sub>DD</sub>	-1	—	1	-1	—	1	μA
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	V <sub>DD</sub> -0.1	—	2.4	V <sub>DD</sub> -0.1	—	V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> =4.0mA	—	0.2	0.4	—	0.2	0.4	V

**Terminal Capacitance**(f = 1MHz, T<sub>a</sub> = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C <sub>ADD</sub>	V <sub>ADD</sub> = 0V	—	3	5	pF
Input Capacitance	C <sub>I</sub>	V <sub>I</sub> = 0V	—	5	6	pF
I/O Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	6	7	pF

**AC Electrical Characteristics O Read Cycle**(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	SRM2264L10		SRM2264L12		Unit
			Min	Max	Min	Max	
Read cycle time	t <sub>RC</sub>	*1	100	—	120	—	ns
Address access time	t <sub>ACC</sub>		—	100	—	120	ns
CS1 access time	t <sub>ACS1</sub>		—	100	—	120	ns
CS2 access time	t <sub>ACS2</sub>		—	100	—	120	ns
OE access time	t <sub>OE</sub>		—	50	—	60	ns
CS1 output set time	t <sub>CLZ1</sub>	*2	10	—	10	—	ns
CS1 output floating time	t <sub>CHZ1</sub>		—	35	—	40	ns
CS2 output set time	t <sub>CLZ2</sub>		10	—	10	—	ns
CS2 output floating time	t <sub>CHZ2</sub>		—	35	—	40	ns
OE output set time	t <sub>OLZ</sub>		5	—	5	—	ns
OE output floating time	t <sub>OHZ</sub>		—	35	—	40	ns
Output hold time	t <sub>OH</sub>		*1	10	—	10	—

**O Write Cycle**

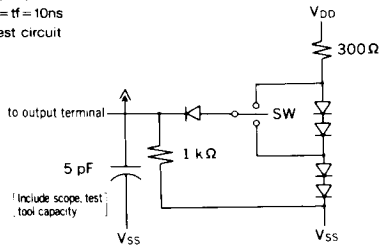
Parameter	Symbol	Conditions	SRM2264L10		SRM2264L12		Unit
			Min	Max	Min	Max	
Write cycle time	t <sub>WC</sub>	*1	100	—	120	—	ns
Chip select time 1	t <sub>CW1</sub>		80	—	85	—	ns
Chip select time 2	t <sub>CW2</sub>		80	—	85	—	ns
Address enable time	t <sub>AW</sub>		80	—	85	—	ns
Address setup time	t <sub>AS</sub>		0	—	0	—	ns
Write pulse width	t <sub>WP</sub>		60	—	70	—	ns
Address hold time	t <sub>WR</sub>		0	—	0	—	ns
Input data setup time	t <sub>DW</sub>		50	—	50	—	ns
Input data hold time	t <sub>DH</sub>		0	—	0	—	ns
WE output floating	t <sub>WHZ</sub>		*3	—	35	—	40
WE output setup time	t <sub>OW</sub>	5		—	5	—	ns

**\* 1 Test Conditions**

1. Input pulse level : 0.8V to 2.4V
2. tr = tf = 10ns
3. Input and output timing reference levels : 1.5V
4. Output load I<sub>HL</sub> + C<sub>L</sub> = 100pF

**\* 3 Test Conditions**

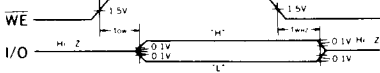
1. Input pulse level : 0.8V to 2.4V
2. tr = tf = 10ns
3. Test circuit



Test : t<sub>ow</sub>, t<sub>whz</sub> Hi-Z → "H" and "H" → Hi-Z SW is V<sub>DD</sub> side

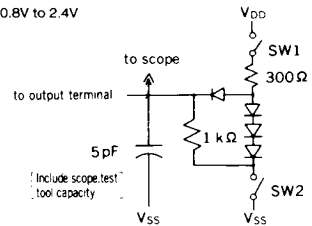
Test : t<sub>ow</sub>, t<sub>whz</sub> Hi-Z → "L" and "L" → Hi-Z SW is V<sub>SS</sub> side

Output turnon turnoff time



**\* 2 Test Conditions**

1. Input pulse level : 0.8V to 2.4V
2. tr = tf = 10ns
3. Test circuit

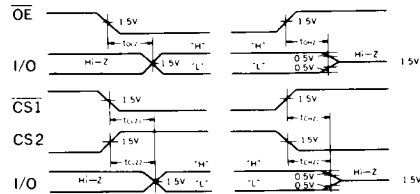


Test : t<sub>chz1</sub>, t<sub>chz2</sub>, t<sub>ohz</sub> Both SW1 and SW2 are close

Test : t<sub>clz1</sub>, t<sub>clz2</sub>, t<sub>olz</sub> Hi-Z → "H" SW1 is open, SW2 is close.

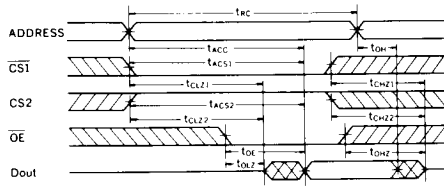
Test : t<sub>clz1</sub>, t<sub>clz2</sub>, t<sub>olz</sub> Hi-Z → "L" SW1 is close, SW2 is open.

Output turnon turnoff time

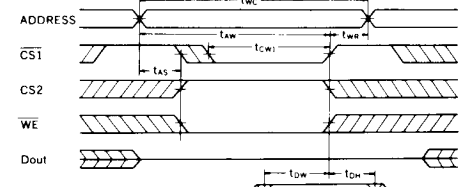


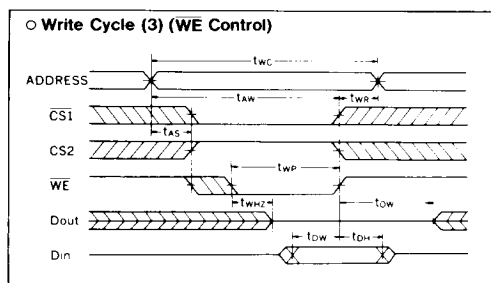
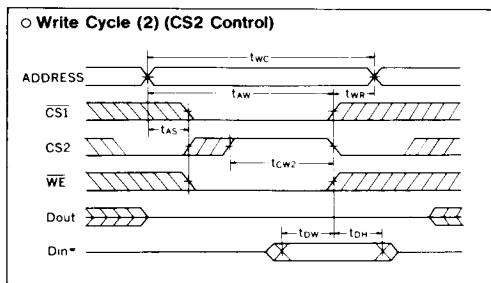
**● Timing Chart**

**○ Read Cycle**



**○ Write Cycle (1) (CS1 Control)**





- Note :
1. During read cycle time,  $\overline{WE}$  is to be "H" level.
  2. During write cycle time that is controlled by CS1 or CS2, Output Buffer is in high impedance state whether  $\overline{OE}$  level is "H" or "L".
  3. During write cycle time that is controlled by  $\overline{WE}$ , Output Buffer is high impedance state if  $\overline{OE}$  is "H" level.

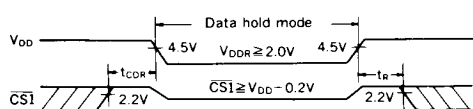
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

( $T_a = 0$  to  $70^\circ\text{C}$ )

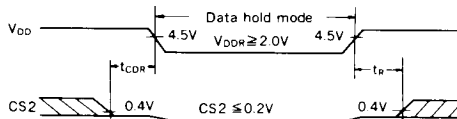
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	$V_{DDR}$		2.0	—	5.5	V
Data retention current	$I_{DDR}$	$V_{DD} = 3\text{V}$ $CS1 = CS2 = V_{DD} - 0.2\text{V}$ or $CS2 = 0.2\text{V}$	—	—	10	$\mu\text{A}$
Chip select data hold time	$t_{CDR}$		0	—	—	ns
Operation recovery time	$t_R$		$t_{RC}^*$	—	—	ns

\*  $t_{RC}$  = Read cycle time

Data retention timing ( $\overline{CS1}$  Control)



Data retention timing ( $\overline{CS2}$  Control)



■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A0 to A12	DATA I/O	Mode	$I_{DD}$
H	X	—	—	—	Hi-Z	Unselected	$I_{DD0}, I_{DDS1}$
—	L	—	—	—	Hi-Z	Unselected	$I_{DD0}, I_{DDS1}$
L	H	X	L	Stable	Input data	Write	$I_{DD0}$
L	H	L	H	Stable	Output data	Read	$I_{DD0}$
L	H	H	H	Stable	Hi-Z	Output disable	$I_{DD0}$

X: "H" or "L", —: "H", "L" or "Hi-Z"

● Reading data

Data is able to be read when the address is setted while holding  $\overline{CS1} = "L"$ ,  $CS2 = "H"$ ,  $\overline{OE} = "L"$  and  $\overline{WE} = "H"$ . Since Data I/O terminals are in high impedance state when  $\overline{OE} = "H"$ , the data bus line can be used for any other objective, then access time apparently is able to be cut down.

### ● Writing data

There are the following four ways of writing data into the memory.

- (1) Hold  $\overline{CS2}$  = "H",  $\overline{WE}$  = "L" set addresses and give "L" pulse to  $\overline{CS1}$ .
- (2) Hold  $\overline{CS1}$  = "L".  $\overline{WE}$  = "L", set addresses and give "H" pulse to  $\overline{CS2}$ .
- (3) Hold  $\overline{CS1}$  = "L",  $\overline{CS2}$  = "H", set addresses and give "L" pulse to  $\overline{WE}$ .
- (4) After setting addresses, give "L" pulse to  $\overline{CS1}$ ,  $\overline{WE}$  and give "H" pulse to  $\overline{CS2}$ .

Anyway, data on the Data I/O terminals are latched up into the SRM2264L<sub>90/10/12</sub> at the end of the period that  $\overline{CS1}$ ,  $\overline{WE}$  are "L" level, and  $\overline{CS2}$  is "H" level. As Data I/O terminals are in high impedance state when any of  $\overline{CS1}$ ,  $\overline{OE}$  = "H", or  $\overline{CS2}$  = "L", the contention on the data bus can be avoided.

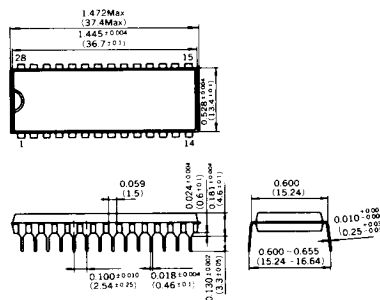
### ● Standby mode

When  $\overline{CS1}$  is "H" or  $\overline{CS2}$  is "L" level, the SRM2264L<sub>90/10/12</sub> is in the standby mode which has retaining date operation. In this case Data I/O terminals are Hi-Z, and all inputs of addresses,  $\overline{WE}$  and data can be any "H" or "L". When  $\overline{CS1}$  and  $\overline{CS2}$  level are in the range over  $V_{DD}-0.2V$ , or  $\overline{CS2}$  level is in the range under 0.2V, in the SRM2264L<sub>10/12</sub> there is almost no current flow except through the high resistance parts of the memory.

### ■ PACKAGE DIMENSIONS

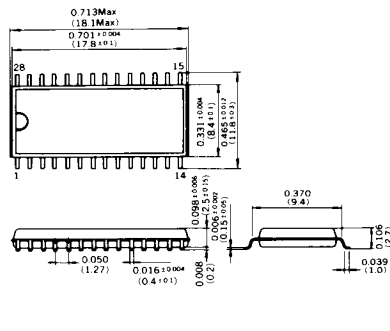
C28

28-pin DIP



M28-2 \*1

28-pin SOP



\*1 SRM2264LM<sub>90/10/12</sub> has the same characteristics as SRM2264LC<sub>90/10/12</sub>.

CHARACTERISTICS CURVES

