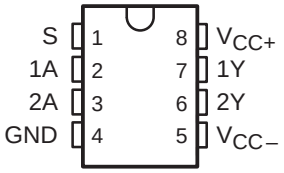
- **Meets or Exceeds the Requirement of TIA/EIA-232-F and ITU Recommendation V.28**
- **Withstands Sustained Output Short Circuit to Any Low-Impedance Voltage Between –25 V and 25 V**
- **2-μs Maximum Transition Time Through the 3-V to –3-V Transition Region Under Full 2500-pF Load**
- **Inputs Compatible With Most TTL Families**
- **Common Strobe Input**
- **Inverting Output**
- **Slew Rate Can Be Controlled With an External Capacitor at the Output**
- **Standard Supply Voltages . . . ±12 V**

D OR P PACKAGE
(TOP VIEW)

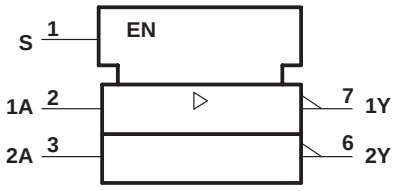


description

The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data-terminal equipment and data-communication equipment as defined by TIA/EIA-232-F. A rate of 20 kbits/s can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL families. Operation is from 12-V and –12-V power supplies.

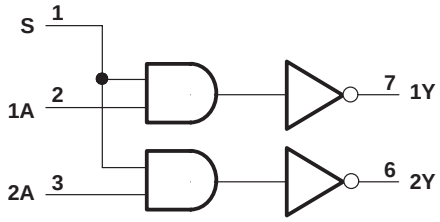
The SN75150 is characterized for operation from 0°C to 70°C.

logic symbol†



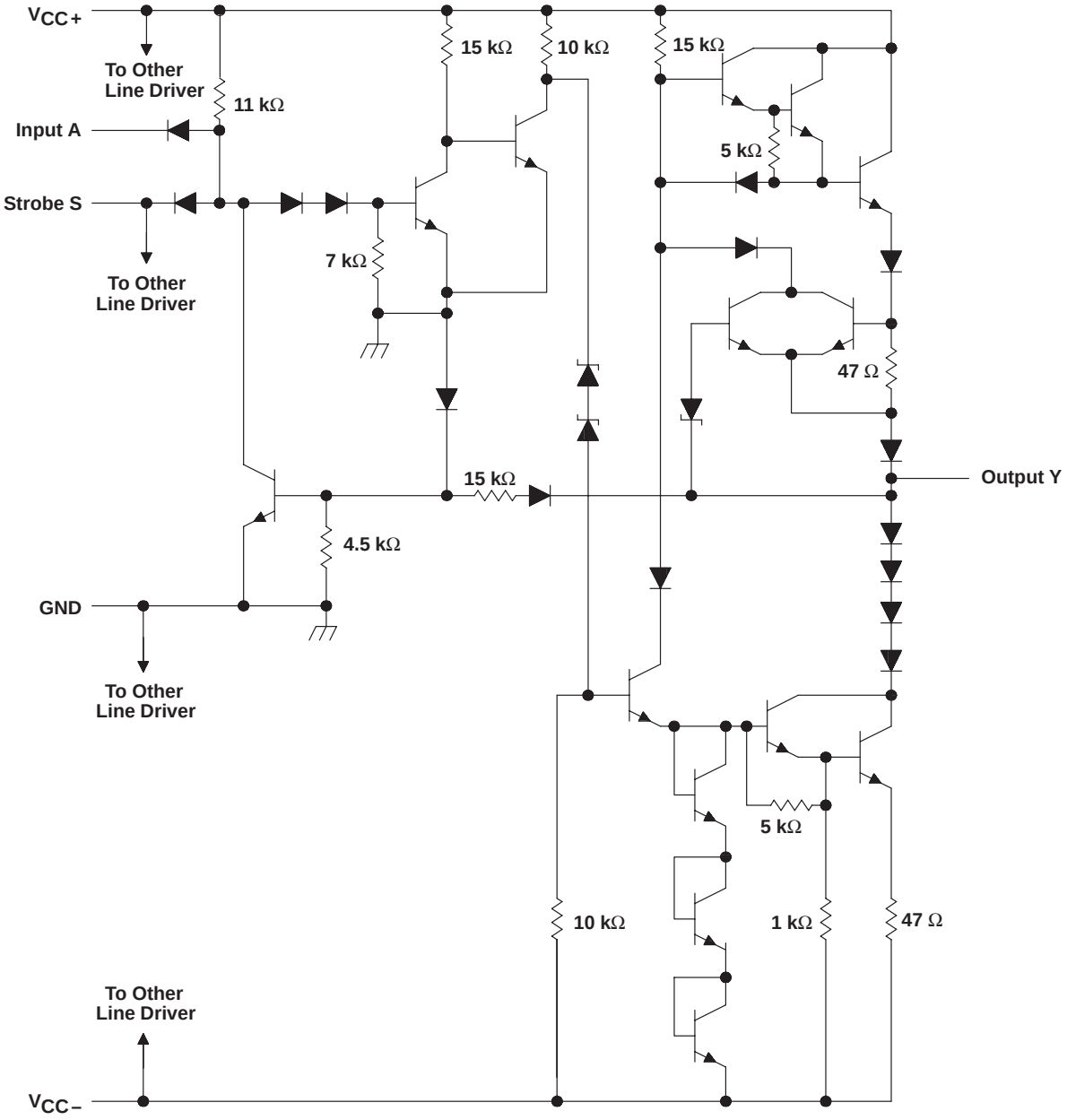
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

schematic (each line driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC-} . . . . . –15 V
Input voltage, V_I . . . . . 15 V
Applied output voltage . . . . . ±25 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . . 197°C/W
P package . . . . . 104°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{CC+}	10.8	12	13.2	V
	V_{CC-}	–10.8	–12	–13.2	
High-level input voltage, V_{IH}		2		5.5	V
Low-level input voltage, V_{IL}		0		0.8	V
Driver output voltage, V_O				±15	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±13.2 V (unless otherwise noted)

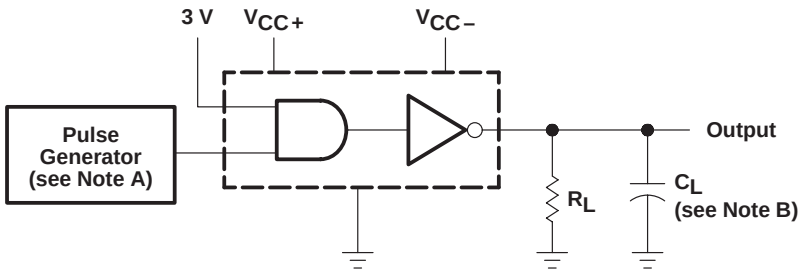
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC+} = 10.8 V, V_{IL} = 0.8 V,	V_{CC-} = –10.8 V, R_L = 3 kΩ to 7 kΩ	5	8		V
V_{OL}	Low-level output voltage (see Note 4)		V_{CC+} = 10.8 V, V_{IH} = 2 V,	V_{CC-} = –10.8 V, R_L = 3 kΩ to 7 kΩ		–8	–5	V
I_{IH}	High-level input current	Data input	V_I = 2.4 V			1	10	μA
		Strobe input				2	20	
I_{IL}	Low-level input current	Data input	V_I = 0.4 V			–1	–1.6	mA
		Strobe input				–2	–3.2	
I_{OS}	Short-circuit output current‡		V_O = 25 V			2	8	mA
			V_O = –25 V			–3	–8	
			V_O = 0,	V_I = 3 V	10	15	30	
			V_O = 0,	V_I = 0	–10	–15	–30	
I_{CCH+}	Supply current from V_{CC+}, high-level output		V_I = 0, R_L = 3 kΩ, T_A = 25°C			10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output					–1	–10	mA
I_{CCL+}	Supply current from V_{CC+}, low-level output		V_I = 3 V, T_A = 25°C	R_L = 3 kΩ,		8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output					–9	–20	mA

† All typical values are at V_{CC+} = 12 V, V_{CC-} = –12 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.
NOTE 4: The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic levels only, e.g., when –5 V is the maximum, the typical value is a more negative voltage.

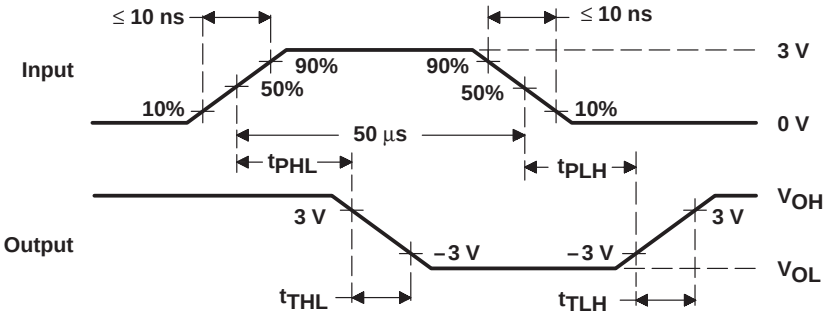
switching characteristics, V_{CC+} = 12 V, V_{CC-} = –12 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	C_L = 2500 pF,	R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	μs
t_{THL}	Transition time, high-to-low-level output			0.2	1.5	2	μs
t_{TLH}	Transition time, low-to-high-level output	C_L = 15 pF,	R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output				20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output				45		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

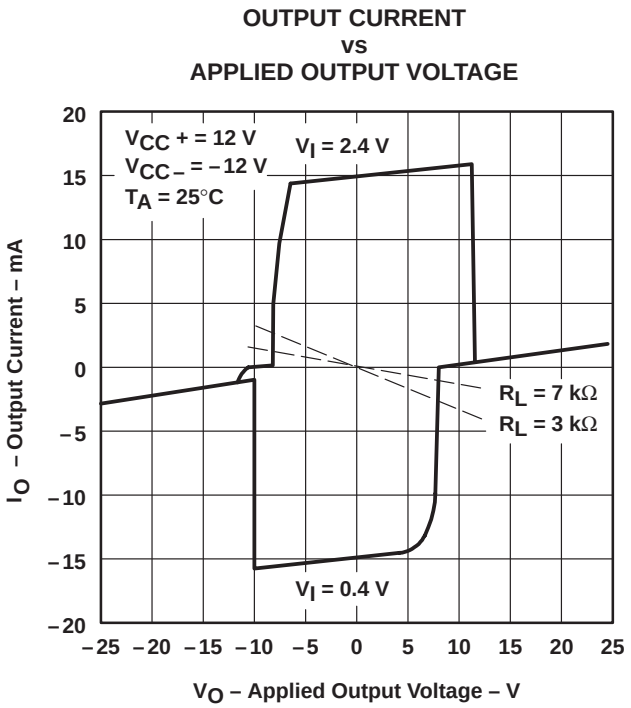


Figure 2

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