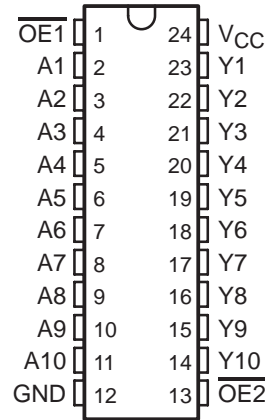


# SN54BCT2828A, SN74BCT2828B 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

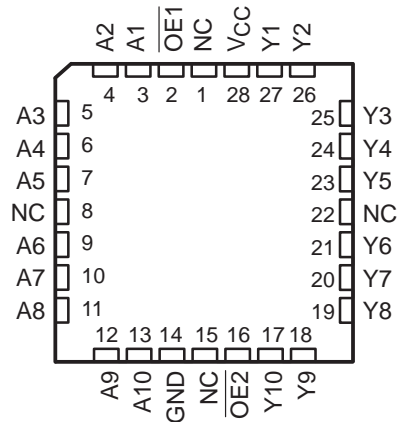
SCBS058A – APRIL 1987 – REVISED NOVEMBER 1993

- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Output Ports Have Equivalent 33- $\Omega$  Series Resistors, So No External Resistors Are Required
- 3-State Inverting Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks, and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

SN54BCT2828A . . . JT OR W PACKAGE  
SN74BCT2828B . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54BCT2828A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

These 10-bit bus/MOS memory drivers provide a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all ten outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

The outputs, which are designed to source or sink up to 12 mA, include 33- $\Omega$  series resistors to reduce overshoot and undershoot.

The SN54BCT2828A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74BCT2828B is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
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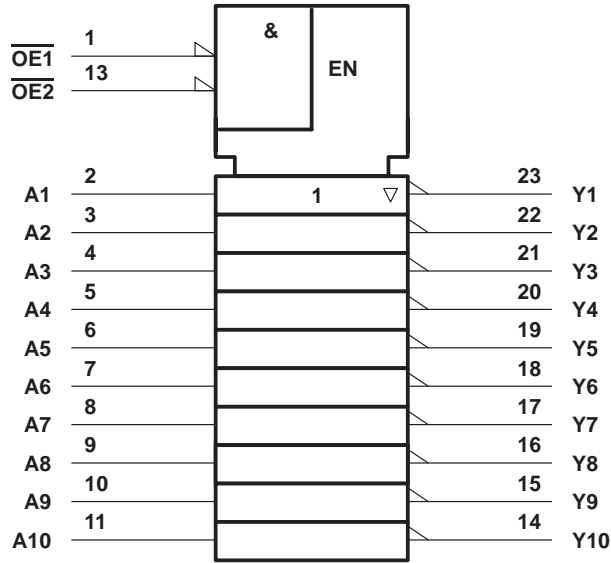
# SN54BCT2828A, SN74BCT2828B

## 10-BIT BUS/MOS MEMORY DRIVERS

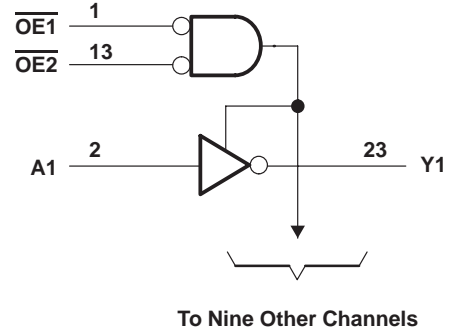
### WITH 3-STATE OUTPUTS

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#### logic symbol†



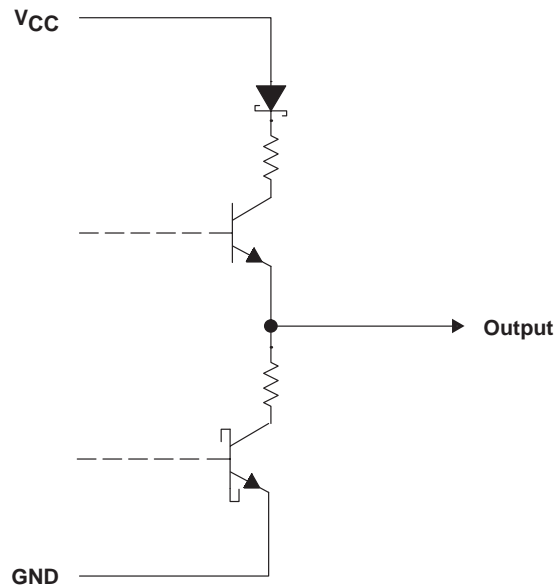
#### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, NT, and W packages.

#### schematic of each output



# SN54BCT2828A, SN74BCT2828B 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ .....	–0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–30 mA
Current into any output in the low state, $I_O$ .....	24 mA
Operating free-air temperature range: SN54BCT2828A .....	–55°C to 125°C
SN74BCT2828B .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

## recommended operating conditions (see Note 2)

		SN54BCT2828A			SN74BCT2828B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current			–1			–1	mA
$I_{OL}$	Low-level output current			12			12	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

NOTE 2: Unused or floating inputs must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54BCT2828A			SN74BCT2828B			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2			–1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -1$ mA	$V_{CC}-2$			$V_{CC}-2$			V
$V_{OL}$	$V_{CC} = 4.5$ V, $I_{OL} = 1$ mA		0.35	0.5		0.35	0.5	V
						0.42	0.8	
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			20	μA
$I_{IL}$	$V_{CC} = 5.5$ V, $V_I = 0.5$ V			–0.2			–0.2	mA
$I_{OZH}$	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			20			20	μA
$I_{OZL}$	$V_{CC} = 5.5$ V, $V_O = 0.5$ V			–20			–20	μA
$I_{OL}$	$V_{CC} = 4.5$ V, $V_O = 2$ V	50			50			mA
$I_{O}^{\S}$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	–30		–112	mA
$I_{CCL}$	$V_{CC} = 5.5$ V, Outputs open		28			28	40	mA
$I_{CCZ}$	$V_{CC} = 5.5$ V, Outputs open		3.5			3.5	6	mA
$C_i$	$V_{CC} = 5$ V, $V_I = 2.5$ V or 0.5 V		5			5		pF
$C_o$	$V_{CC} = 5$ V, $V_O = 2.5$ V or 0.5 V		8			8		pF

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25$ °C.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



**SN54BCT2828A, SN74BCT2828B**  
**10-BIT BUS/MOS MEMORY DRIVERS**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54BCT2828A		SN74BCT2828B		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1.8	2.7	5.9	1.5	10	1.3	6.6	ns
$t_{PHL}$			1.2	3.1	4.8	1.5	9	0.9	5	
$t_{PZH}$	$\overline{OE}$	Y	3.6	5.8	7.8	2	15	2.9	9	ns
$t_{PZL}$			5.5	7.9	10.2	2	21	4.8	11.5	
$t_{PHZ}$	$\overline{OE}$	Y	4.7	7.2	9.3	2	18	3.8	10.8	ns
$t_{PLZ}$			3.3	5.4	7.2	2	15	2.7	8.7	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74BCT2828BDW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74BCT2828BNT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SNJ54BCT2828AFK	OBSOLETE	LCCC	FK	28		TBD	Call TI	Call TI
SNJ54BCT2828AJT	OBSOLETE	CDIP	JT	24		TBD	Call TI	Call TI
SNJ54BCT2828AW	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

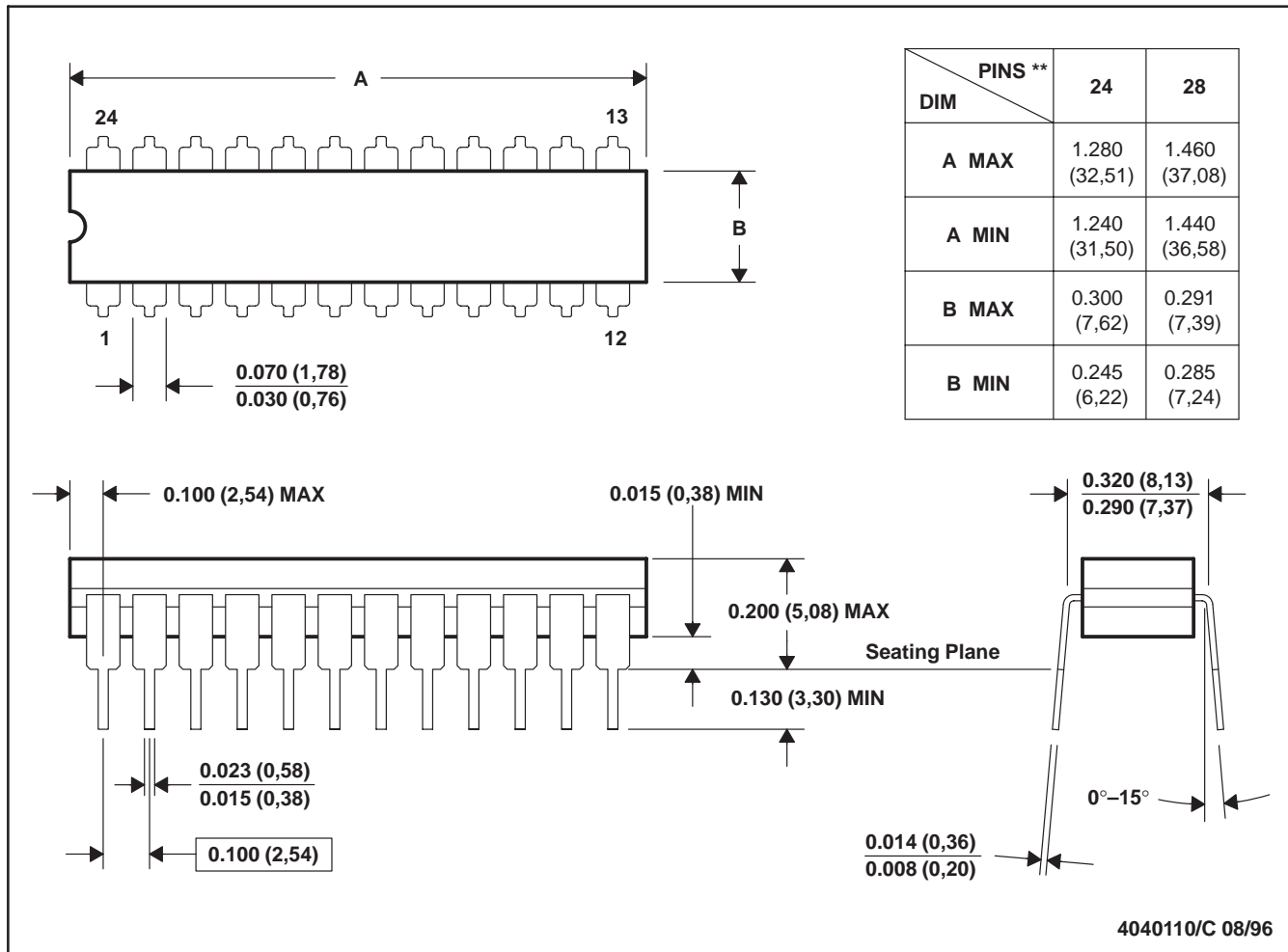
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JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



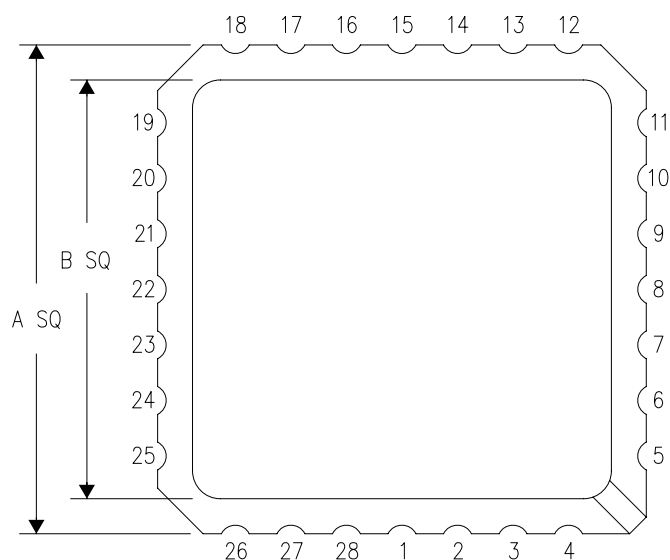
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB



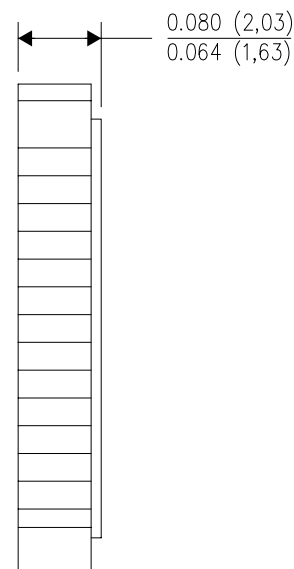
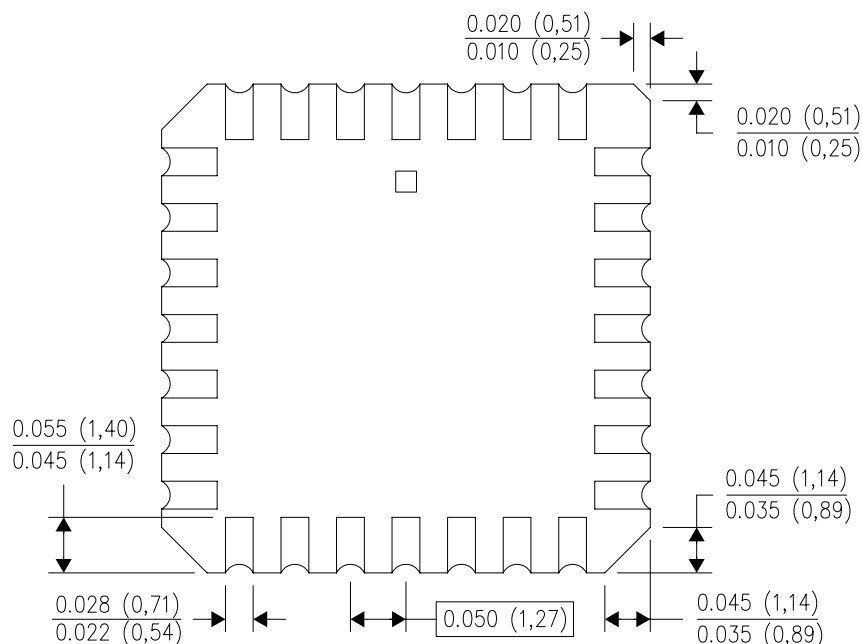
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



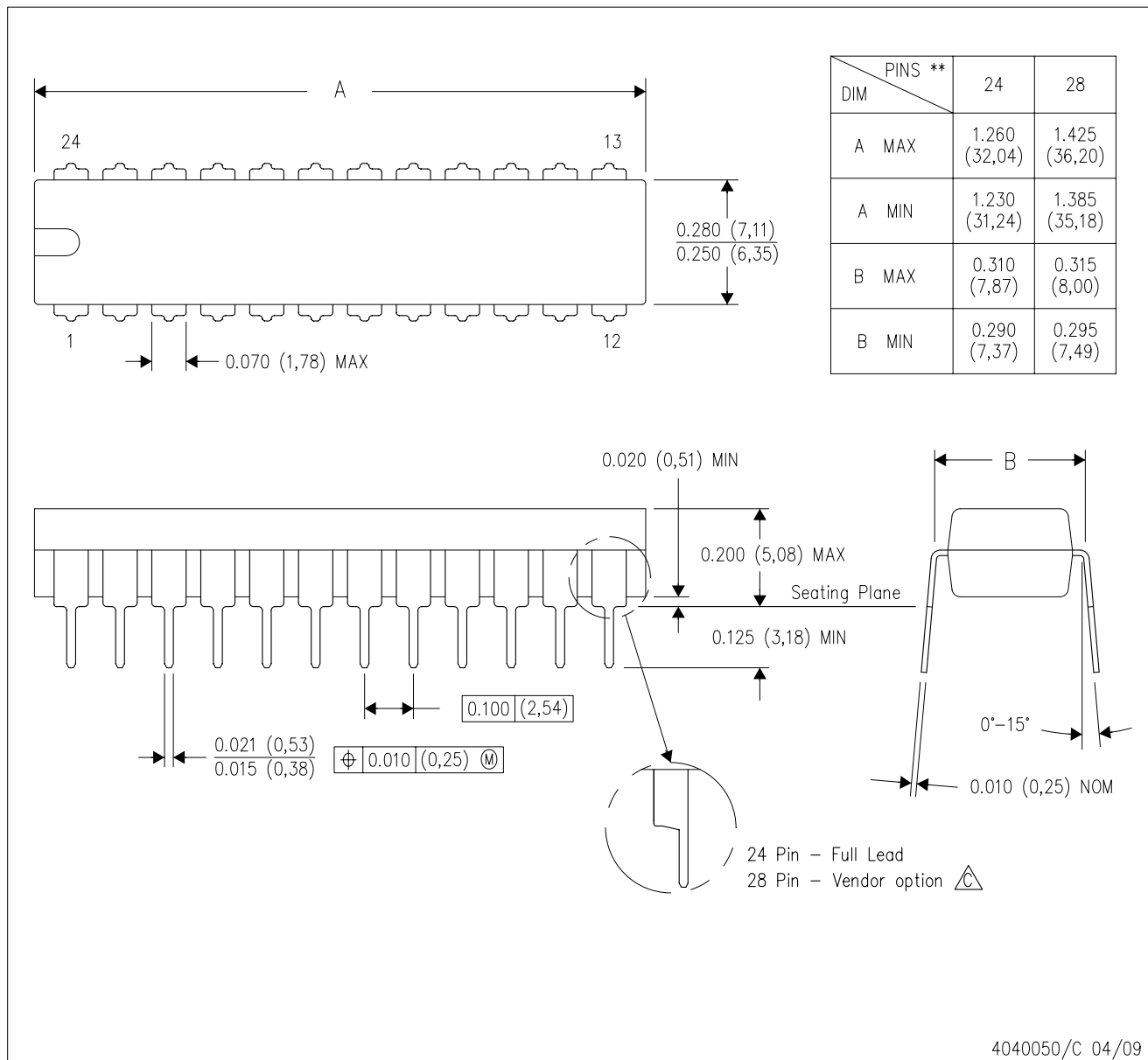
4040140/D 01/11


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NT (R-PDIP-T\*\*) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.



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