

- Free-Running Read and Write Clocks Can Be Asynchronous or Coincident
- Read and Write Operations Synchronized to Independent System Clocks
- Input-Ready Flag Synchronized to Write Clock
- Output-Ready Flag Synchronized to Read Clock
- 2048 Words by 9 Bits
- Low-Power Advanced CMOS Technology
- Programmable Almost-Full/Almost-Empty Flag
- Input-Ready, Output-Ready, and Half-Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 12 ns With a 50-pF Load
- Data Rates up to 67 MHz
- 3-State Outputs
- Package Options Include 44-Pin Plastic Leaded Chip Carrier (FN) and 64-Pin Thin Quad Flat (PAG, PM) Packages

## description

The SN74ACT7807 is a 2048-word by 9-bit FIFO with high speed and fast access times. It processes data at rates up to 67 MHz and access times of 12 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The write-clock (WRTCLK) and read-clock (RDCLK) inputs should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when the write-enable (WRTEN1/DP9, WRTEN2) inputs are high and the input-ready (IR) flag output is high. Data is read from memory on the rising edge of RDCLK when the read-enable (RDEN1, RDEN2) and output-enable (OE) inputs are high and the output-ready (OR) flag output is high. The first word written to memory is clocked through to the output buffer regardless of the levels on RDEN1, RDEN2, and OE. The OR flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronous to WRTCLK and RDCLK.  $\overline{\text{RESET}}$  must be asserted while at least four WRTCLK and four RDCLK cycles occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and half-full (HF) flags low and the almost-full/almost-empty (AF/AE) flag high. The FIFO must be reset upon power up.

The SN74ACT7807 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

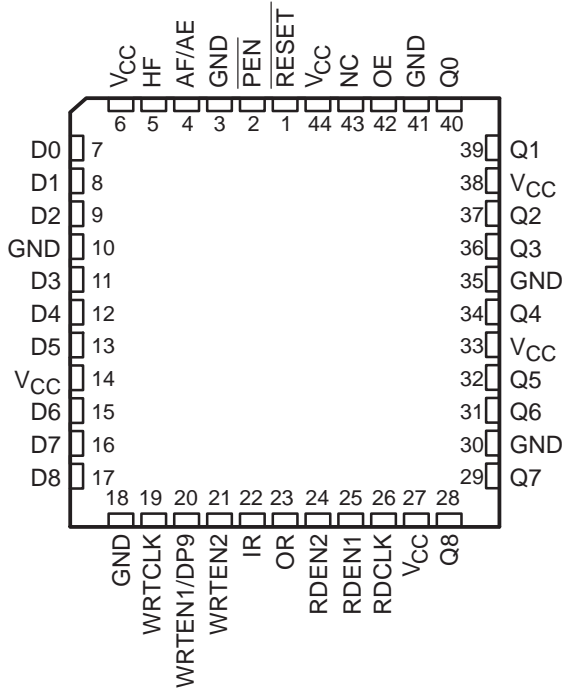
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

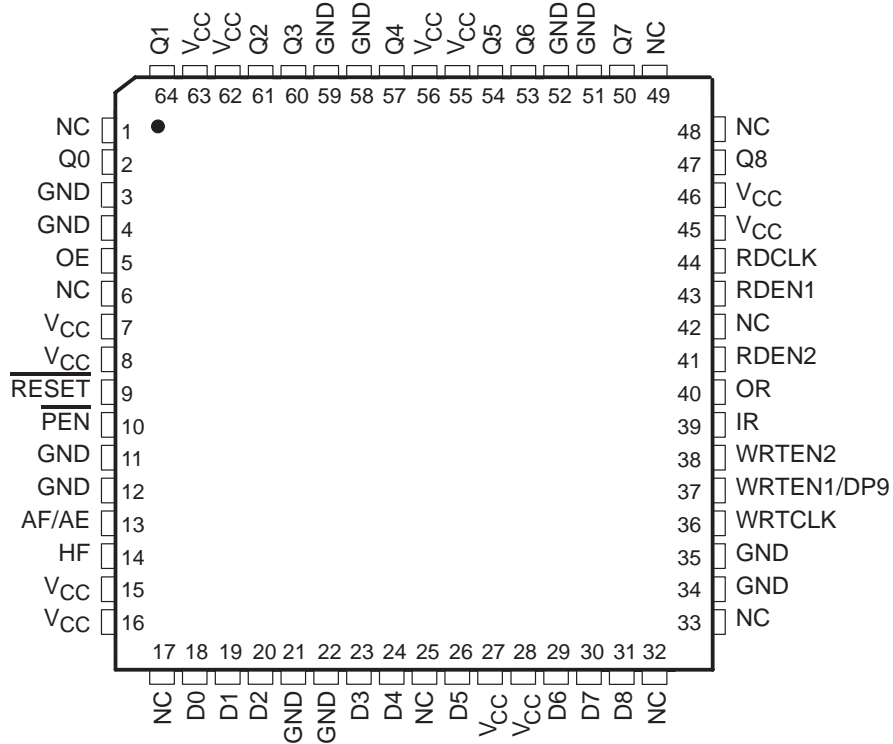
CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS200D – JANUARY 1991 – REVISED APRIL 1998

FN PACKAGE  
(TOP VIEW)

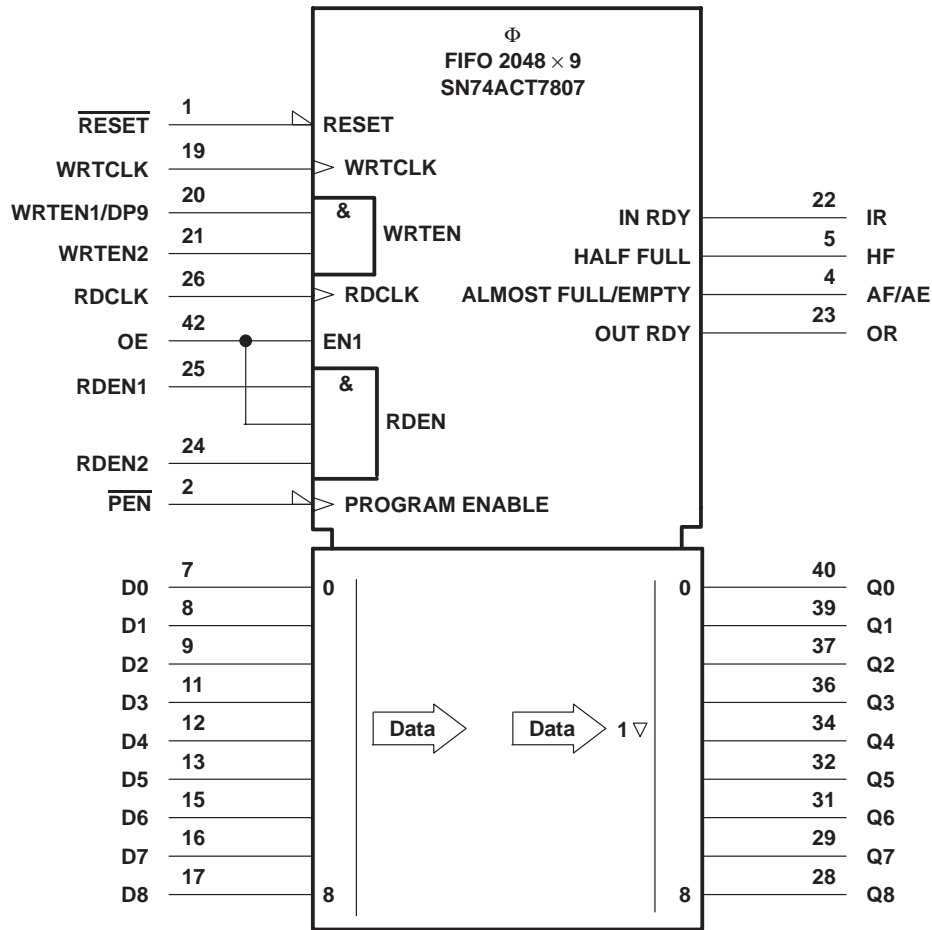


PAG OR PM PACKAGE  
(TOP VIEW)



NC – No internal connection

logic symbol†

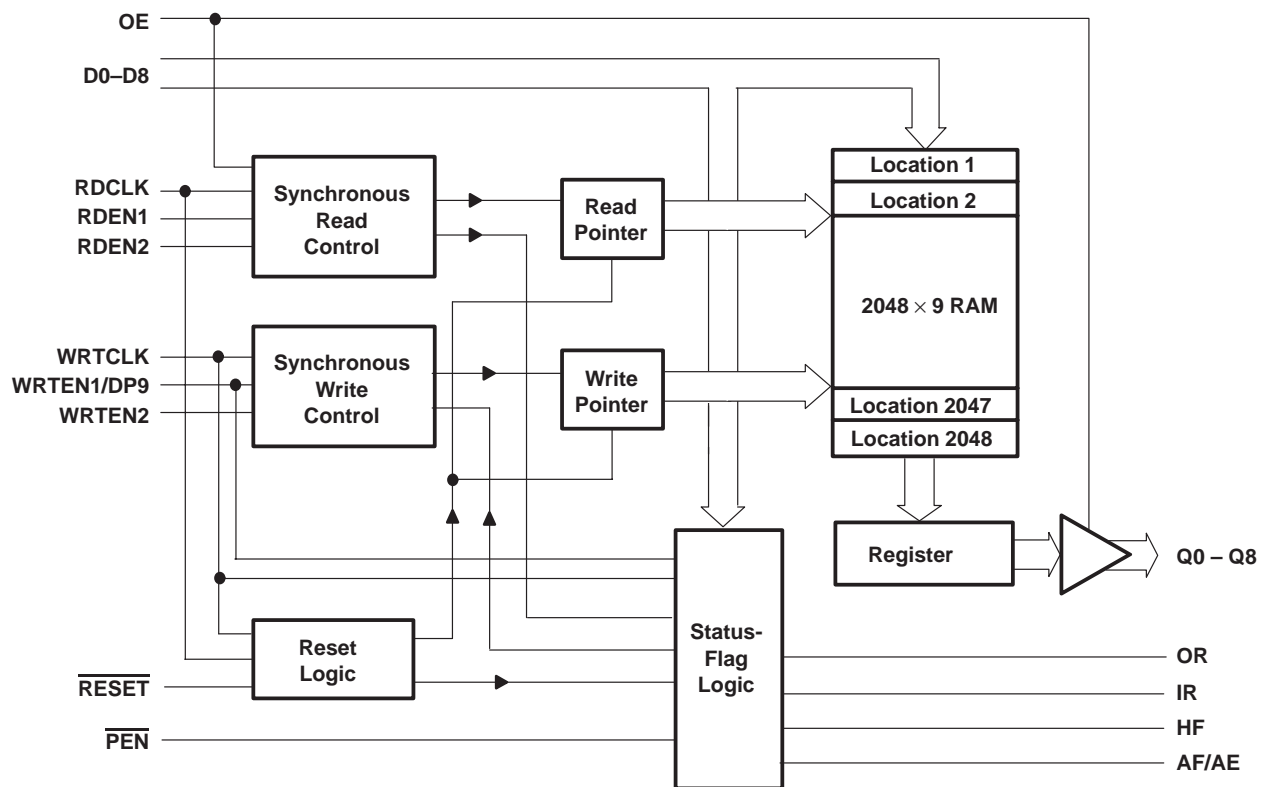


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the FN package.

**SN74ACT7807**  
**2048 × 9**  
**CLOCKED FIRST-IN, FIRST-OUT MEMORY**

SCAS200D – JANUARY 1991 – REVISED APRIL 1998

**functional block diagram**



## Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
AF/AE	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE or the default value of 256 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or fewer words or (2048 – Y) or more words. AF/AE is high after reset.
D0–D8	I	Nine-bit data input port
HF	O	Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset.
IR	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
OE	I	Output enable. When OE, RDEN1, RDEN2 and OR are high, data is read from the FIFO on a low-to-high transition of RDCLK. When OE is low, reads are disabled and the data outputs are in the high-impedance state.
OR	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{\text{PEN}}$	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q8	O	Nine-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q8 on the third rising edge of RDCLK. OR also is asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q8.
RDCLK	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when RDEN1, RDEN2, OE, and OR are high. OR is synchronous to the low-to-high transition of RDCLK.
RDEN1 RDEN2	I	Read enables. When RDEN1, RDEN2, OE, and OR are high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{\text{RESET}}$	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when WRTEN1/DP9, WRTEN2, and IR are high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1/DP9	I	Write enable/data pin 9. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK. When programming an AF/AE offset value, WRTEN1/DP9 is used as the most-significant data bit.
WRTEN2	I	Write enable. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

**offset values for AF/AE**

The AF/AE flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 256 are used. The AF/AE flag is high when the FIFO contains X or fewer words or (2048 – Y) or more words.

Program enable ( $\overline{PEN}$ ) should be held high throughout the reset cycle.  $\overline{PEN}$  can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D8 and WRTEN1/DP9 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding  $\overline{PEN}$  low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D8 and WRTEN1/DP9 at the time of the second WRTCLK low-to-high transition. While the offsets are programmed, data is not written to the FIFO memory, regardless of the state of the write enables (WRTEN1/DP9, WRTEN2). A maximum value of 1023 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 256,  $\overline{PEN}$  must be held high.

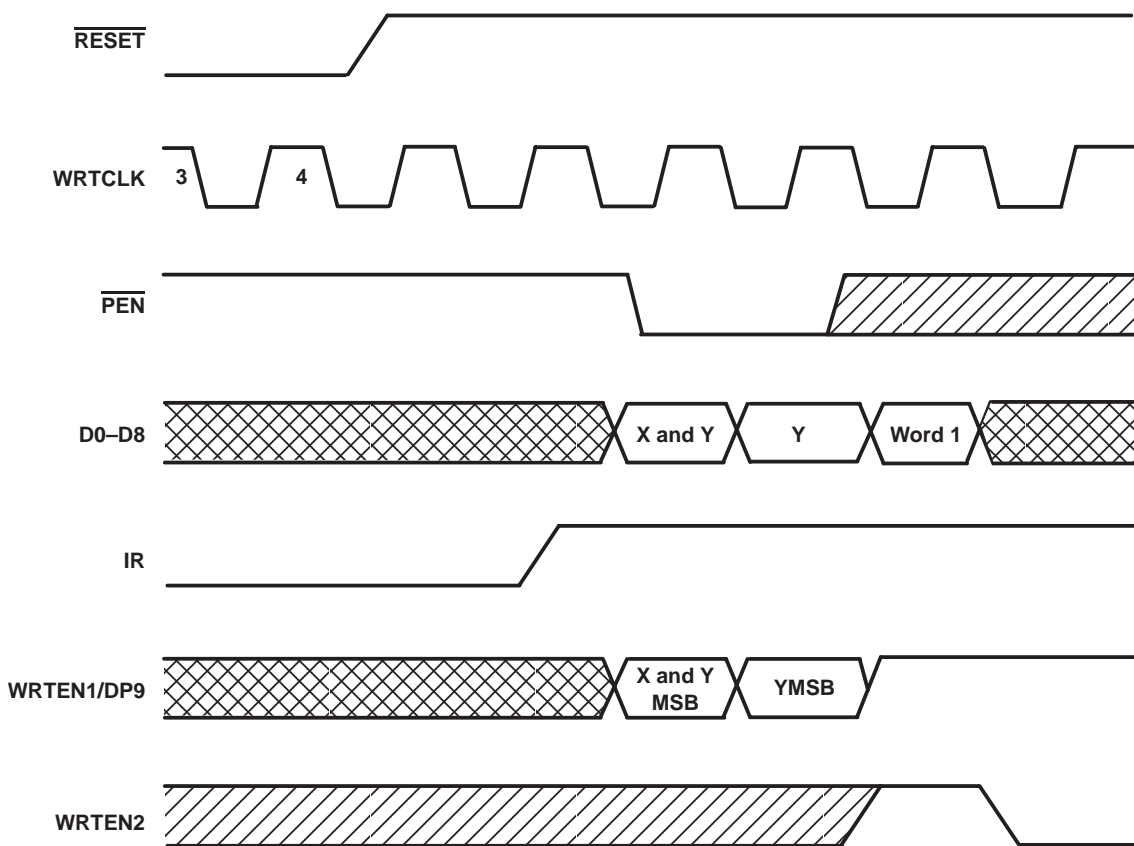
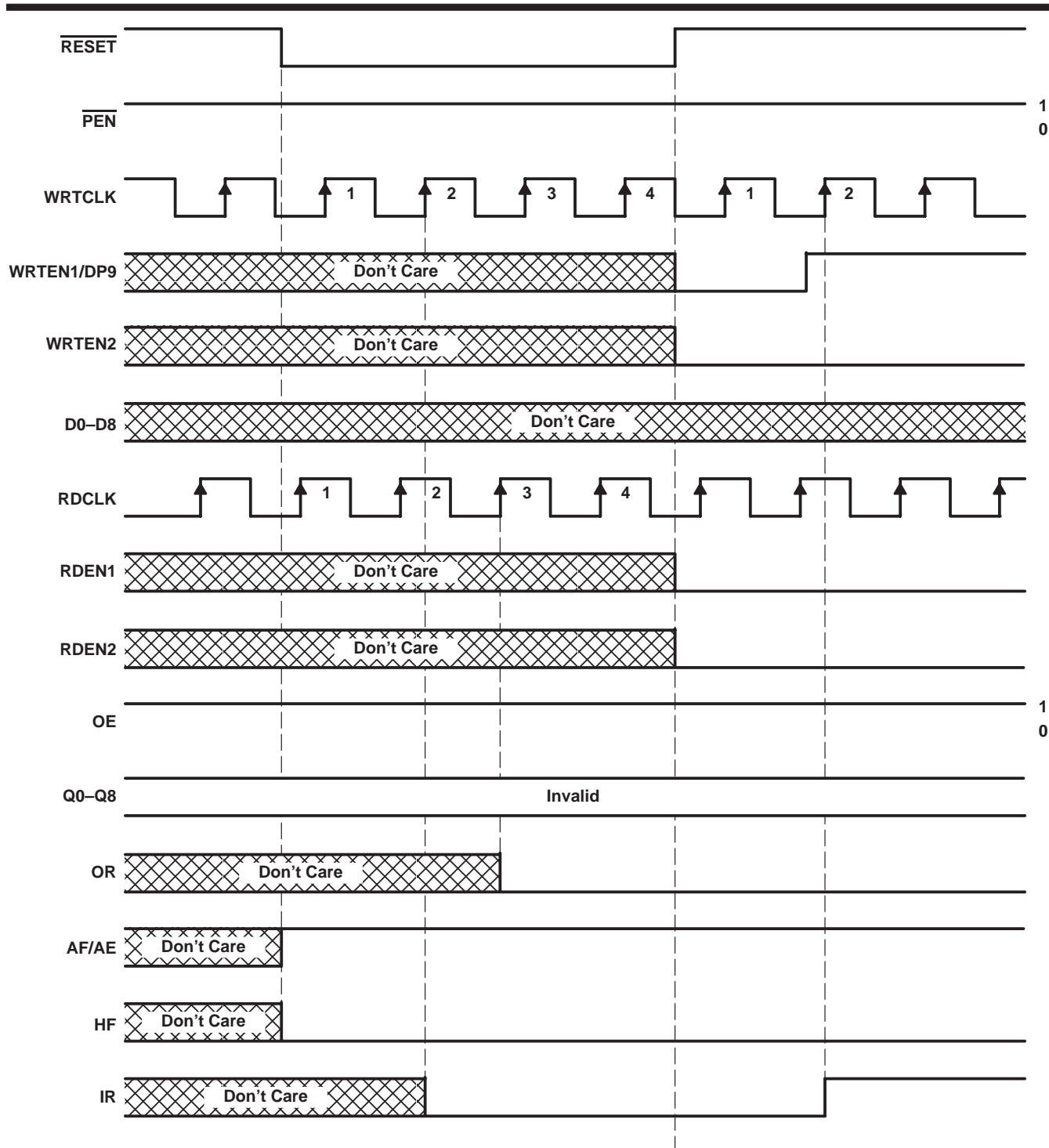


Figure 1. Programming X and Y Separately



Define the AF/AE Flag Using the Default Value of X = Y = 256

Figure 2. Reset Cycle

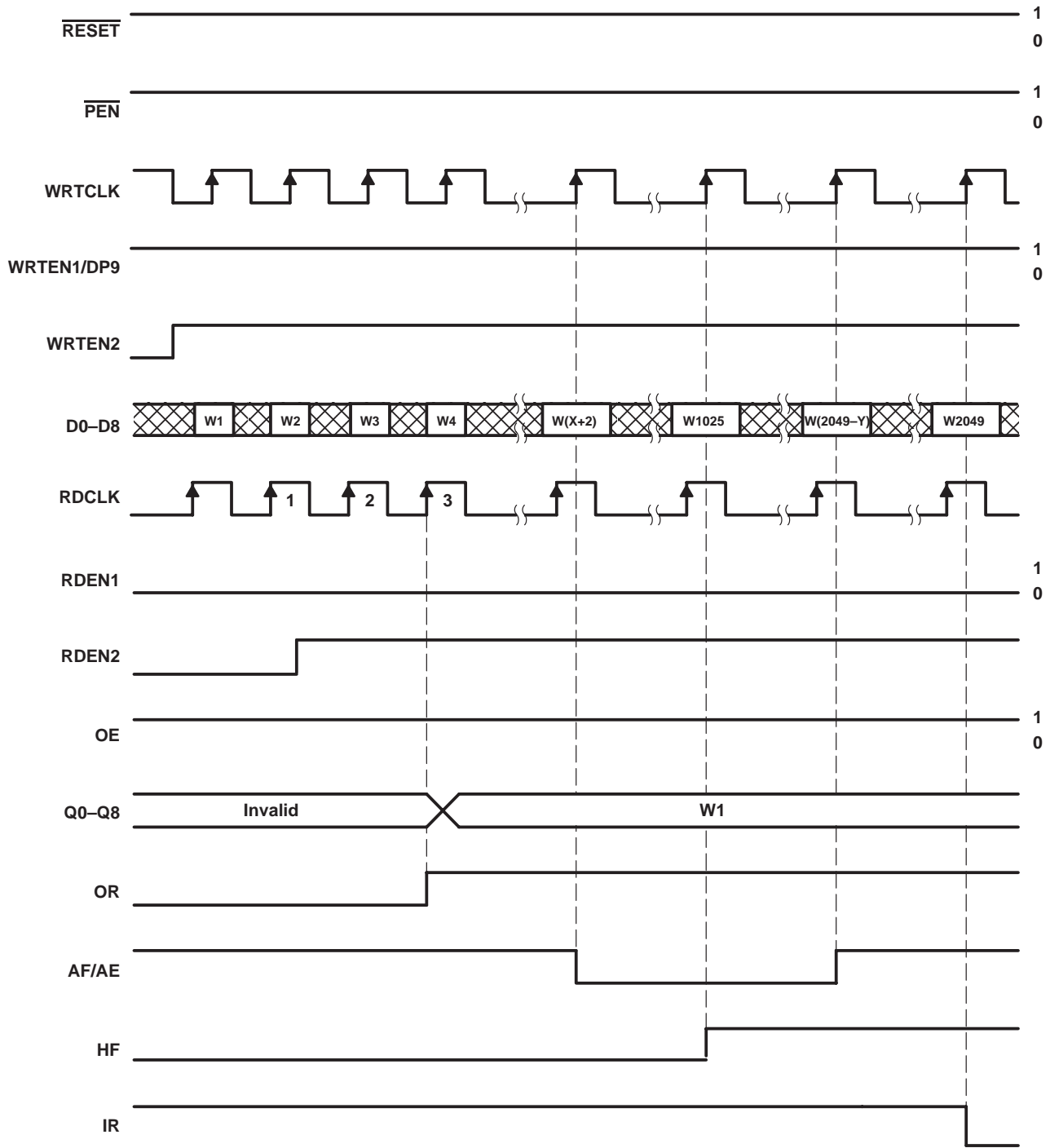


Figure 3. Write Cycle



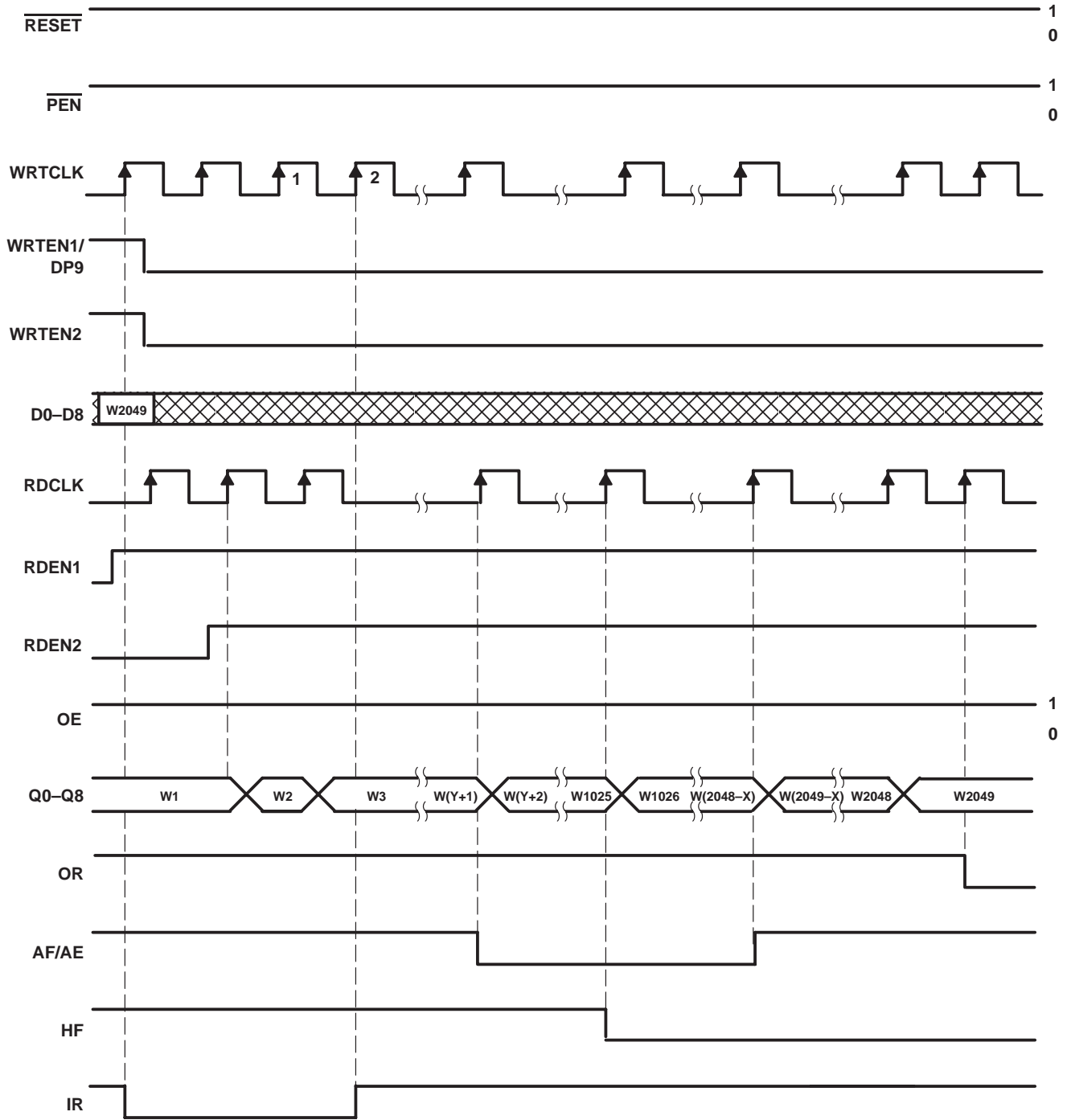


Figure 4. Read Cycle

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ .....	-0.5 V to 7 V
Voltage range applied to a disabled 3-state output .....	-0.5 V to 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): FN package .....	46°C/W
PAG package .....	58°C/W
PM package .....	67°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions**

		'ACT7807-15		'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8		0.8		0.8	V
$I_{OH}$	High-level output current	Q outputs, flags		-8		-8		-8		mA
$I_{OL}$	Low-level output current	Q outputs		16		16		16		mA
		Flags		8		8		8		
$T_A$	Operating free-air temperature	0	70	0	70	0	70	0	70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -8\text{ mA}$	2.4			V
$V_{OL}$	Flags			0.5	V
	Q outputs			0.5	
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$ or 0			±5	µA
$I_{OZ}$	$V_{CC} = 5.5\text{ V}$ , $V_O = V_{CC}$ or 0			±5	µA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC} - 0.2\text{ V}$ or 0			400	µA
$\Delta I_{CC}$ §	WRTEN1/DP9	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND		2	mA
	Other inputs			1	
$C_i$	$V_I = 0$ , $f = 1\text{ MHz}$			4	pF
$C_o$	$V_O = 0$ , $f = 1\text{ MHz}$			8	pF

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or  $V_{CC}$ .

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 5)

		'ACT7807-15		'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	67		50		40		25		MHz
$t_w$	Pulse duration	WRTCLK high or low		6	8	9	13			ns
		RDCLK high or low		6	8	9	13			
		$\overline{\text{PEN}}$ low		6	9	9	13			
$t_{\text{su}}$	Setup time	D0–D8 before WRTCLK $\uparrow$		4	5	5	5			ns
		WRTE1, WRTE2 before WRTCLK $\uparrow$		4	5	5	5			
		OE, RDEN1, RDEN2 before RDCLK $\uparrow$		5	6	6	6.5			
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK $\uparrow$ and RDCLK $\uparrow$		7	8	8	8			
		$\overline{\text{PEN}}$ before WRTCLK $\uparrow$		4	5	5	5			
$t_h$	Hold time	D0–D8 after WRTCLK $\uparrow$		0	0	0	0			ns
		WRTE1, WRTE2 after WRTCLK $\uparrow$		0	0	0	0			
		OE, RDEN1, RDEN2 after RDCLK $\uparrow$		0	0	0	0			
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK $\uparrow$ and RDCLK $\uparrow$		5	5	5	5			
		$\overline{\text{PEN}}$ high after WRTCLK $\downarrow$		0	0	0	0			
		$\overline{\text{PEN}}$ low after WRTCLK $\uparrow$		3	3	3	3			

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7807-15			'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
			MIN	TYP $\ddagger$	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$	WRTCLK or RDCLK		67			50		40		25		MHz
$t_{\text{pd}}$	RDCLK $\uparrow$	Any Q	3	9	12	3	13	3	18	3	25	ns
$t_{\text{pd}}^{\S}$	RDCLK $\uparrow$	Any Q	8									ns
$t_{\text{pd}}$	WRTCLK $\uparrow$	IR	1		9	1	12	1	14	1	16	ns
	RDCLK $\uparrow$	OR	1		9	2	12	2	14	2	16	
	WRTCLK $\uparrow$	AF/AE	2		16	2	20	2	25	2	30	
	RDCLK $\uparrow$		2		17	2	20	2	25	2	30	
$t_{\text{PLH}}$	WRTCLK $\uparrow$	HF	2		19	2	21	2	23	2	25	ns
$t_{\text{PHL}}$	RDCLK $\uparrow$	HF	2		16	2	18	2	20	2	22	ns
$t_{\text{PLH}}$	$\overline{\text{RESET}}$ low	AF/AE	1		12	1	18	1	22	1	24	ns
$t_{\text{PHL}}$	$\overline{\text{RESET}}$ low	HF	2		12	2	18	2	22	2	24	ns
$t_{\text{en}}$	OE	Any Q	2		10	2	13	2	15	2	18	ns
$t_{\text{dis}}$	OE	Any Q	1		11	1	13	1	15	1	18	ns

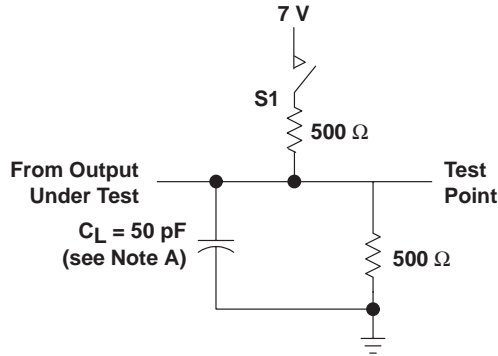
$\ddagger$  All typical values are at  $V_{\text{CC}} = 5$  V,  $T_A = 25^\circ\text{C}$ .

$\S$  This parameter is measured with  $C_L = 30$  pF (see Figure 6).

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

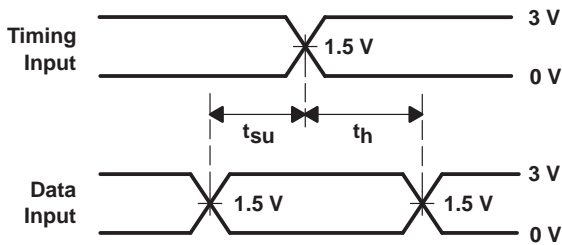
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per FIFO channel	Outputs enabled	91	pF

PARAMETER MEASUREMENT INFORMATION

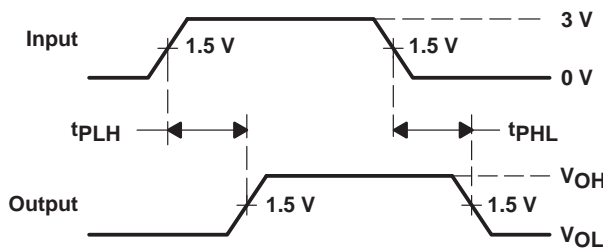


LOAD CIRCUIT

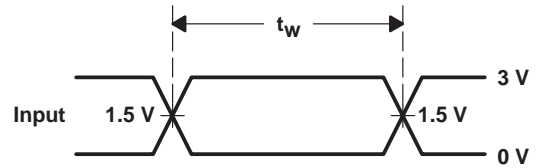
PARAMETER	S1	
$t_{en}$	$t_{pZH}$	Open
	$t_{pZL}$	Closed
$t_{dis}$	$t_{pHZ}$	Open
	$t_{pLZ}$	Closed
$t_{pd}$	$t_{pLH}$	Open
	$t_{pHL}$	Open



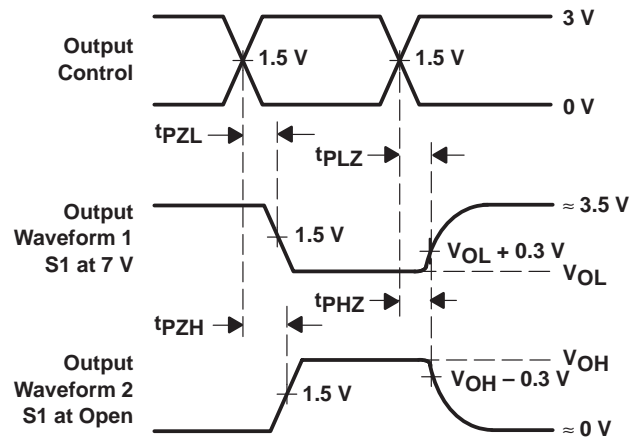
VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES

NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 5. Load Circuit and Voltage Waveforms

**TYPICAL CHARACTERISTICS**

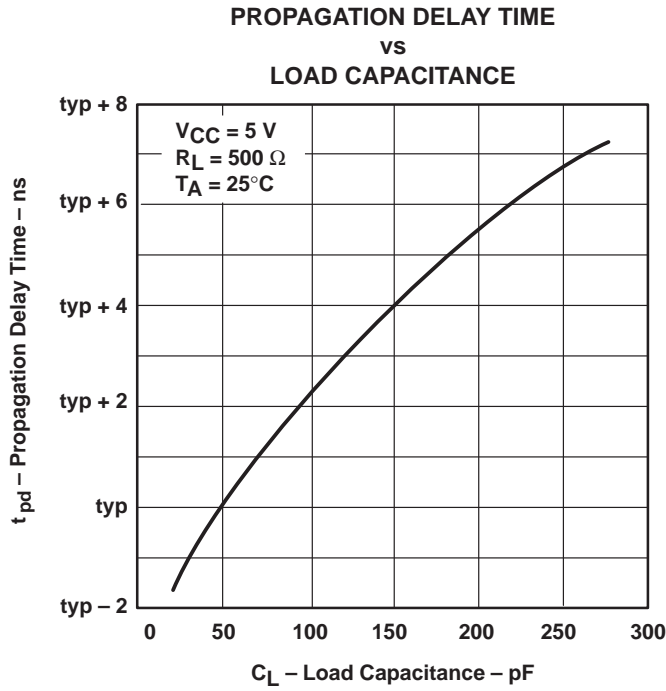


Figure 6

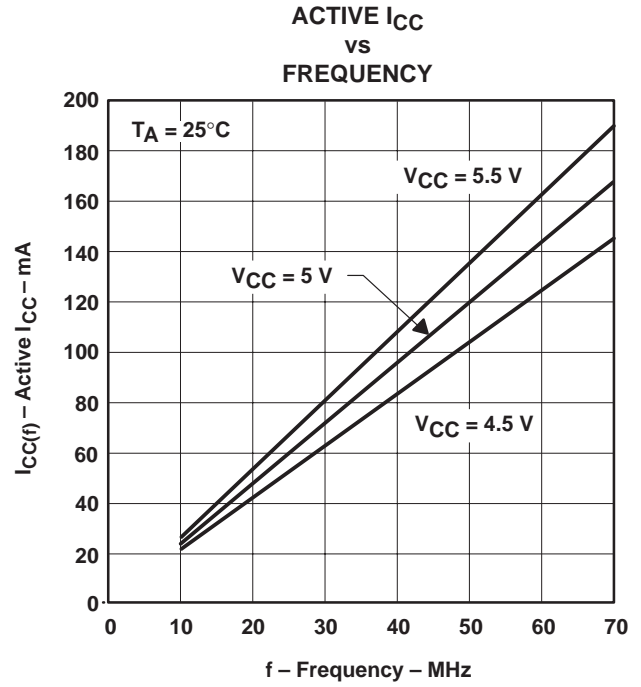


Figure 7

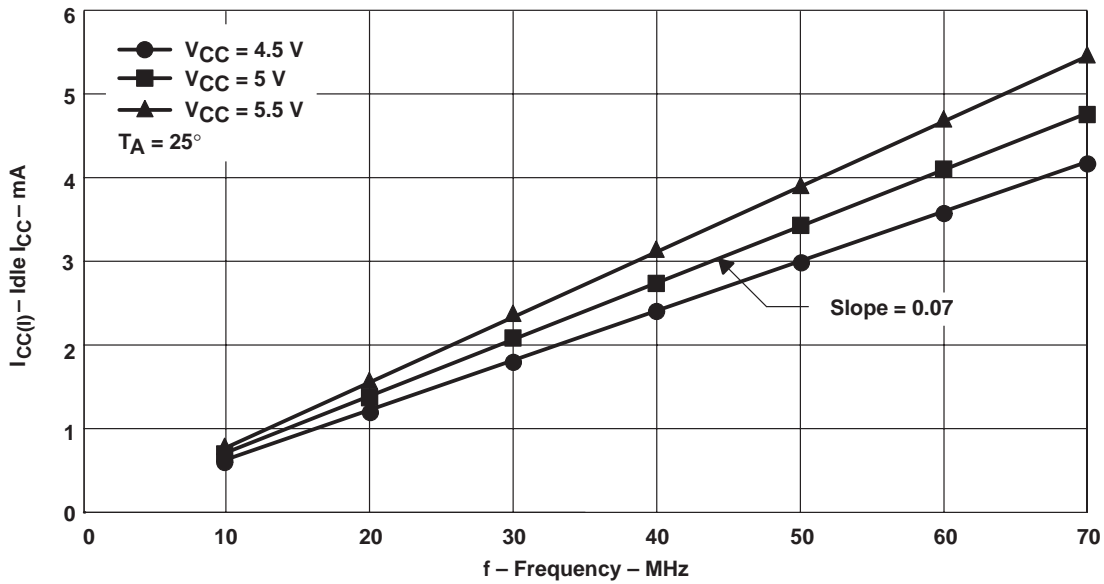
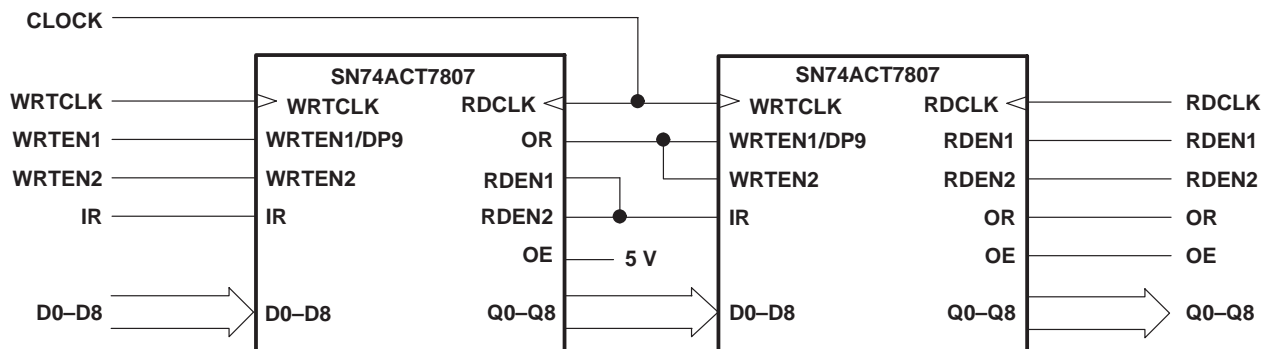
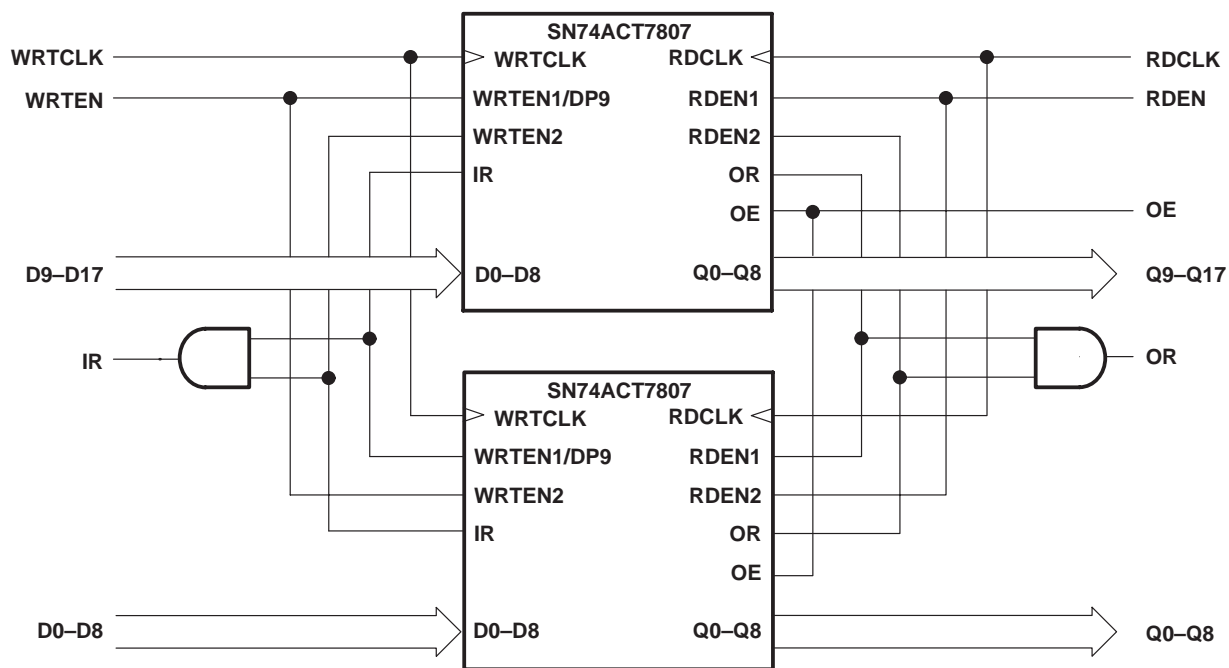


Figure 8. SN74ACT7807 Idle  $I_{CC}$  With WRTCLK Switching,  
Other Inputs at 0 or  $V_{CC} - 0.2\text{ V}$  and Outputs Disconnected

**APPLICATION INFORMATION**



**Figure 9. Word-Depth Expansion: 4096 × 9 Bits**



**Figure 10. Word-Width Expansion: 2048 × 18 Bits**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
1M7807-15PAGG4	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Purchase Samples</a>
SN74ACT7807-15FN	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Purchase Samples</a>
SN74ACT7807-15PAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Purchase Samples</a>
SN74ACT7807-15PM	OBSOLETE	LQFP	PM	64		TBD	Call TI	Call TI	Samples Not Available
SN74ACT7807-20FN	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Purchase Samples</a>
SN74ACT7807-20PAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Purchase Samples</a>
SN74ACT7807-20PM	OBSOLETE	LQFP	PM	64		TBD	Call TI	Call TI	Samples Not Available
SN74ACT7807-25FN	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Purchase Samples</a>
SN74ACT7807-25PM	OBSOLETE	LQFP	PM	64		TBD	Call TI	Call TI	Samples Not Available
SN74ACT7807-40PM	OBSOLETE	LQFP	PM	64		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

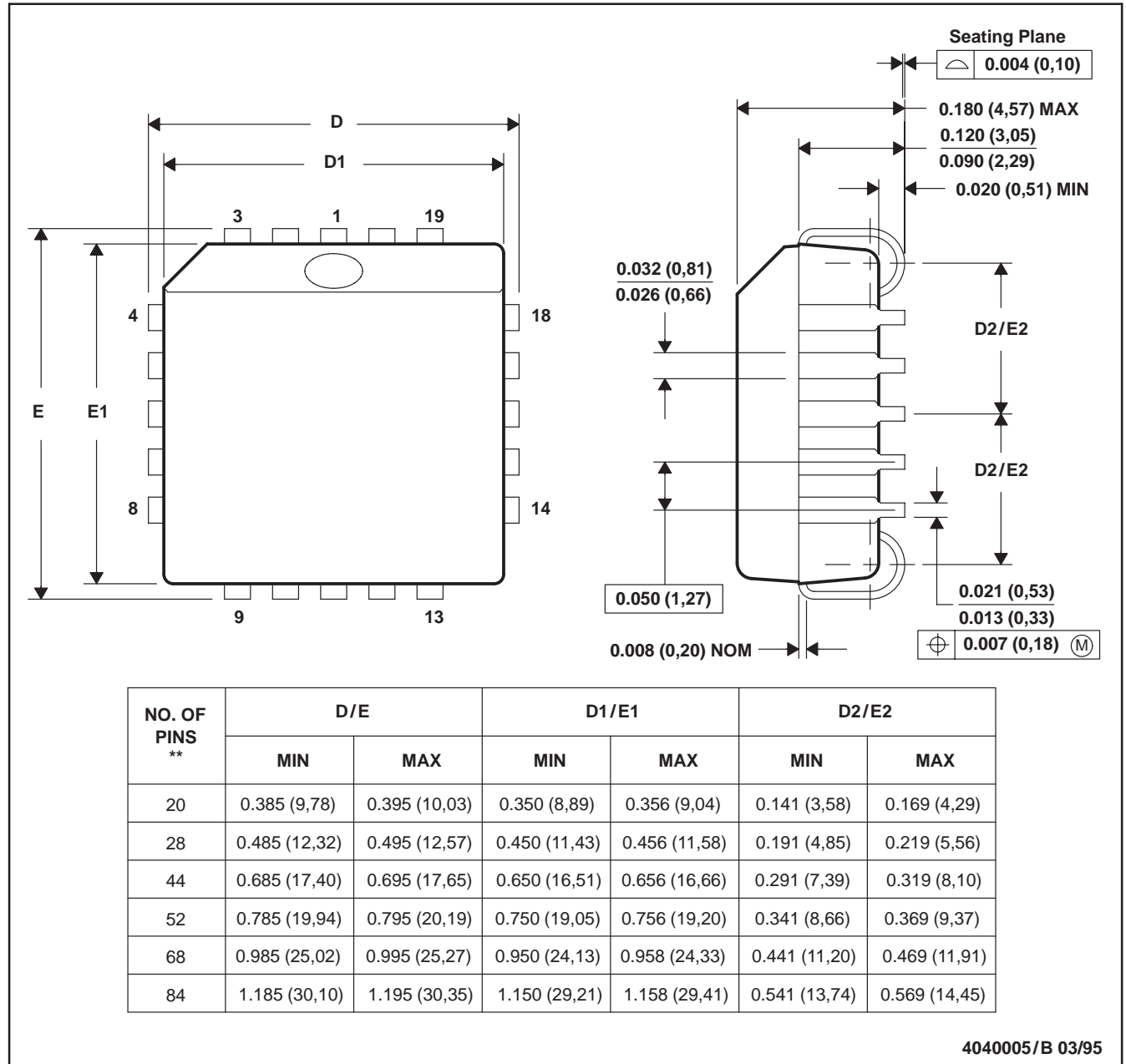
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

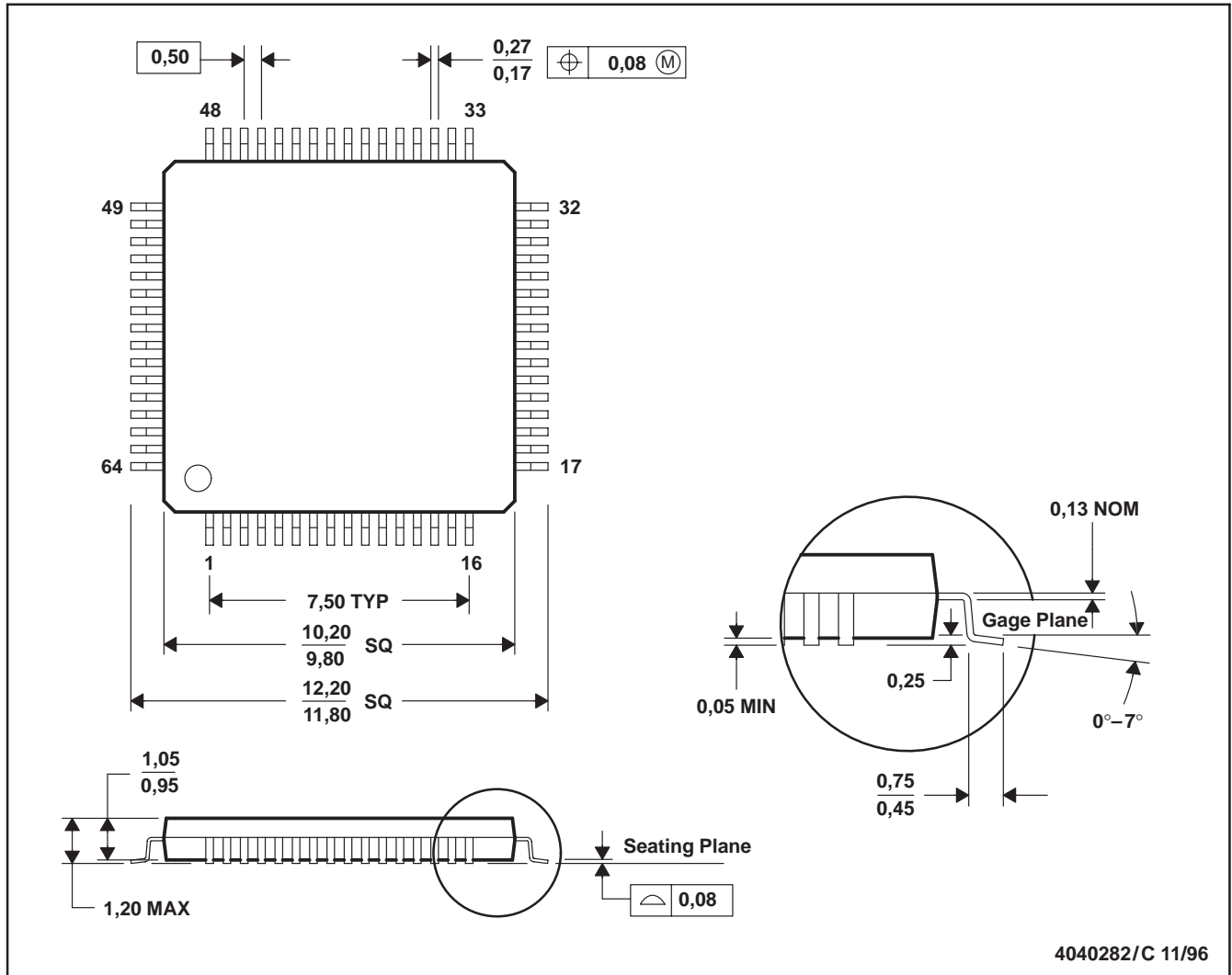
20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

PAG (S-PQFP-G64)

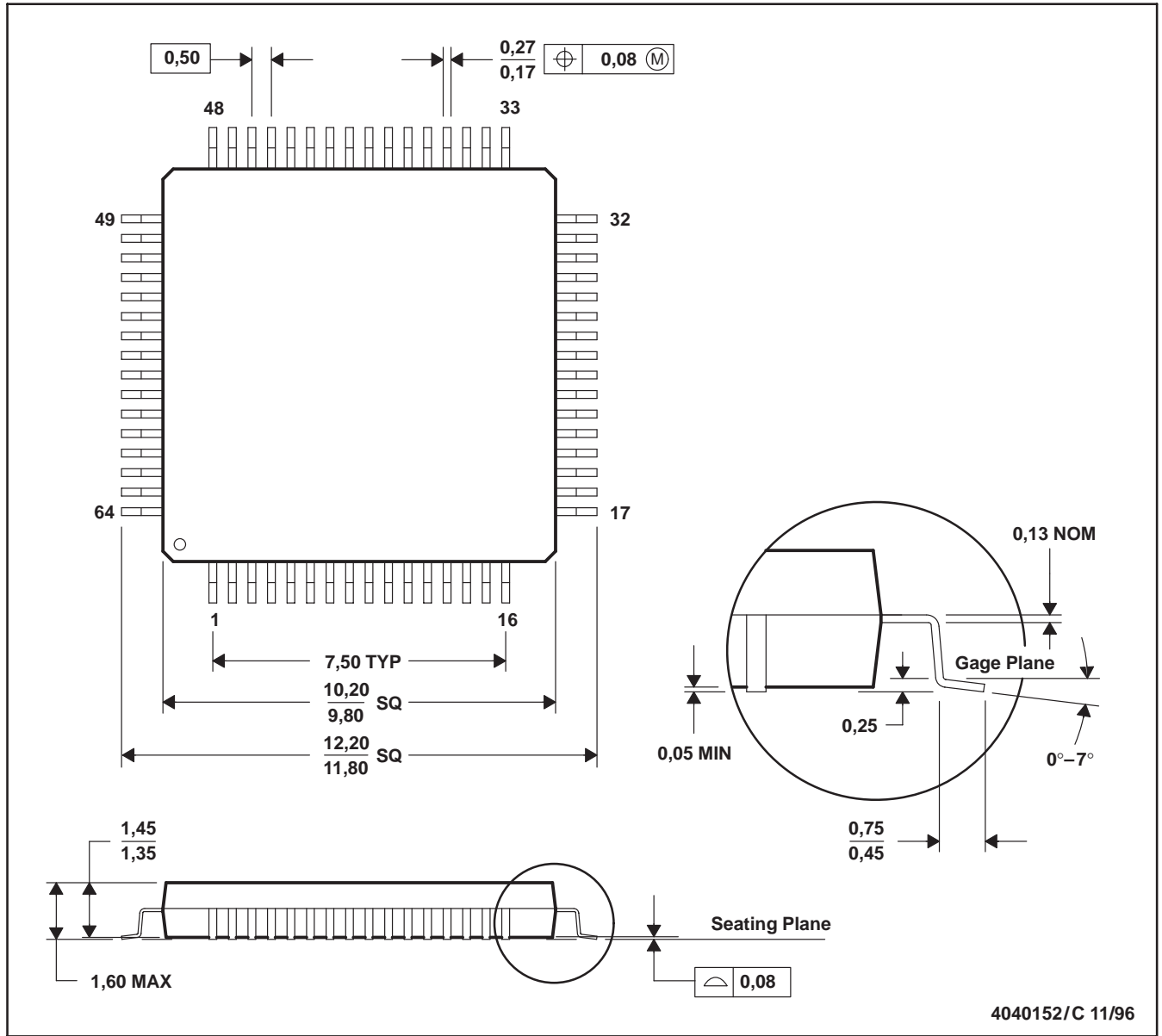
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026  
 D. May also be thermally enhanced plastic with leads connected to the die pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2010, Texas Instruments Incorporated