SIEMENS

ASIC Product Description
SH100E
ECL/CML Gate Array Family

FEATURES

- **Gate complexities from 1,500 to 16,000 gates**
- **120 ps gate delay, 90 ps differential**
- **1.5 GHz D flip-flop, 1.7 GHz differential**
- **Both ECL and CML macro families**
- **TTL I/O available**
- **ECL 10KH/100K compatible**
- **Up to 256 signal pins available**
- **3 levels of series gating**
- **PGA, LCC and LLCC packaging**
- **Daisy, Mentor, and Valid workstation support**
- **CML and ECL is speed/power programmable**

PRODUCT DESCRIPTION

Siemens utilizes a third generation bipolar ECL process to produce a family of high speed, high density ECL/CML gate arrays. The family of gate arrays ranges in density from 1,500 gates for the smallest member and up to 16,000 for the largest member. These gate arrays operate with a cut-off frequency (f_T) of 7 GHz and obtain their high density and design flexibility by allowing the design engineer to mix ECL and CML macros on the same chip. This feature allows the designer to utilize maximum speed ECL technology for critical paths and CML elsewhere for power conservation. In addition, ECL 10KH/100K or TTL on the smaller family members allow the designer added flexibility. Power management also is easier using the wide range of speed/power programming options with this gate array family. Siemens allows you not only to program the current sources, but also the emitter followers independently, thus allowing optimal speed/power combinations.

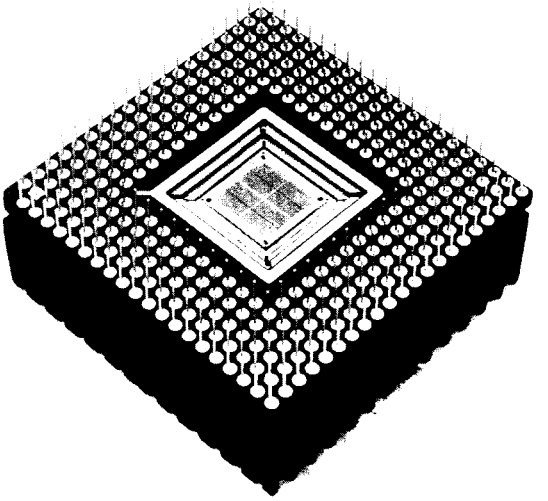
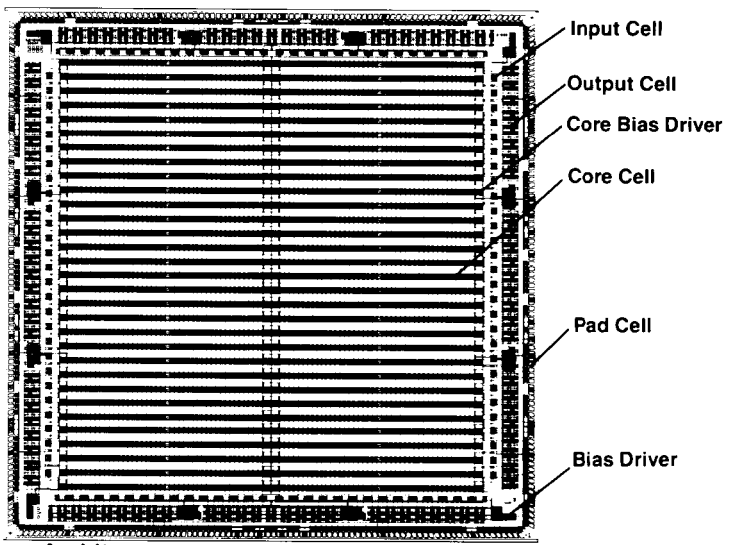


Figure 1. Array Architecture



Array Architecture

The row based architecture shown in Figure 1 above for the 10K/16K gate array is characteristic of all SH100E array masters. The array cores of each master are designed with rows of cells separated by routing channels allowing 25 tracks or metal lines each. The bias drivers are located at the ends of each row and also in the center of the rows in the larger arrays.

Product Family Members

Table 1 shows the relative gate counts, core cell counts, and I/O counts of all four SH100E family members. The maximum ECL complexity which can be accommodated is indicated by the gate count for each master.

Since CML type macros do not require the output emitter followers, they are smaller in cell area than their ECL counterparts. Thus, a larger number of CML macros can be placed on a given master array. For example, if CML macros are used in entirety, the SH100E7 gate counts will be about 16,000.

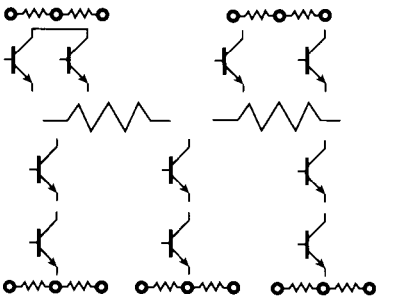
Table 1. Key Architecture Data for SH100E Gate Array Family

Option	SH100E4	SH100E5	SH100E6	SH100E7
Complexity	1,500	2,500	5,000	10,000
Number of Rows	12	16	22	31
Cells/Row	32	40	54	84
Core Cell Number	384	640	1,188	2,604
ECL Gate Number	1,818	2,950	5,000	10,780
CML Gate Number	2,727	4,425	7,500	16,170
I/O Number	84	120	160	256
Maximum TTL I/O Number	84	120	160	N/A
Pad Count	132	172	224	360
Power Pads	48	52	64	104

Core Cell

The internal core cell structure is shown in Figure 2. It contains 10 transistors, 6 current source resistors, 4 load resistors, 1 pinch resistor and 1 level shift resistor for a total device count of 22. Eight of the 10 transistors can be used universally as switching, level shifting, or current source transistors.

Figure 2. Core Cell



I/O Cells

The I/O cells shown in Figures 3 and 4 illustrate the transistor/resistor arrangements and counts necessary to construct input receivers, level shifters, and output transmitters. These cells also can be used to construct complex macros such as multiplexers which then can drive the output pads. This allows for a more efficient use of silicon area.

In the case of the SH100E7, there are 224 input cells and a maximum of 200 output cells.

Additional design flexibility is afforded the design engineer with the use of 10KH ECL or 100K ECL I/Os.

Also available are TTL I/Os where required on the E4, E5, and E6 family members. Inputs and outputs can be mixed at any I/O location without restriction.

In addition, ECL outputs are available with on chip series termination resistors programmable to 0, 20, or 40 ohms.

Figure 3. Input Cell

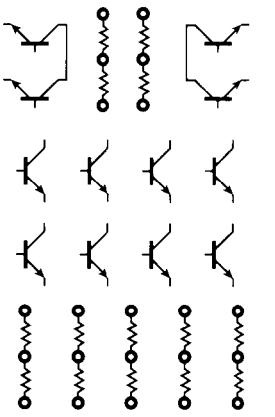
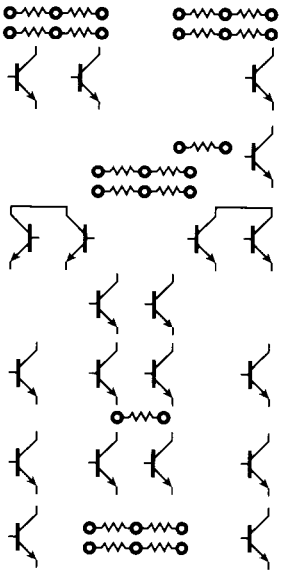
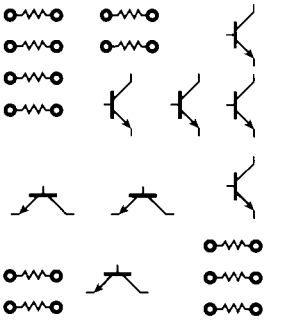


Figure 4. Output Cell

Logic Section



Transmitter Section



Speed/Power Programming

As suggested in Table 2, speed/power trade-off flexibility is provided through many options. With CML, 4 power levels are possible. With ECL, there are 3 intra-macro power levels and 6 independently adjustable emitter follower power levels. Three examples at middle speed/power and both extremes are shown in Table 2. The resistor network used to control the speed/power programming is suggested in Figure 5, with Table 3 describing the different current levels available at each point.

Figure 5. Speed-Power Programming Resistors

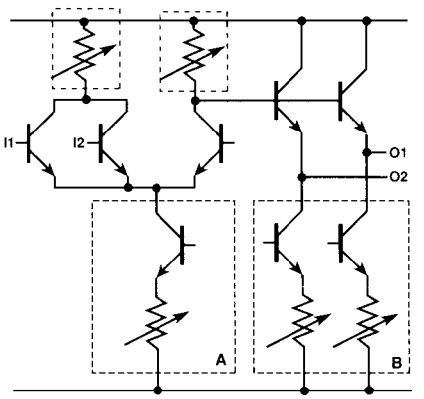


Table 2. Speed/Power Programming Trade-Off for OR/NOR Gate Loaded with F.O.=3, and 2 mm each of 1st and 2nd Metal as Lumped Capacitance

Macro Circuit Type	CML				ECL		
Speed/Power Program	L	S	H	HH	LL	SS	HHH
Macro Size (in core cells)	1				2		
Avg. Delay from I to O [ps]	1,839	959	517	260	802	455	239
Avg. Drive Factor [ps/pF]	1,390	685	330	165	550	260	80
Total Current [mA]	0.275	0.55	1.1	2.2	0.55	1.1	3.3

Table 3. Cascode Current Source Alternatives

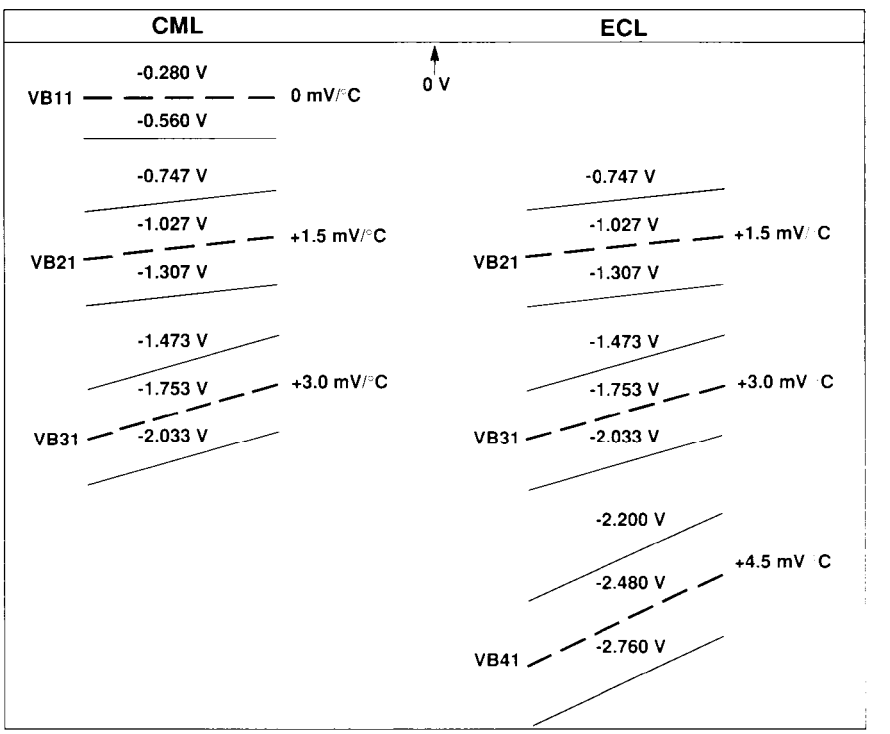
Type	Current Source	Low	Medium	High
A	Cascode I_{SW}	0.275 mA	0.55 mA	1.1 mA
B	Emitter Follower I_{SW}	0.275 mA	0.275 mA	0.275 mA
		0.55 mA	0.55 mA	0.55 mA
			1.1 mA	1.1 mA
				1.375 mA
				1.65 mA
				2.2 mA

CML = Type A only.

Mixing ECL and CML

A main innovation of the SH100E family lies in its capability of accepting both ECL and CML macros on the same chip. The resulting 4 bias voltages for 3 levels of series gating are shown in Figure 6.

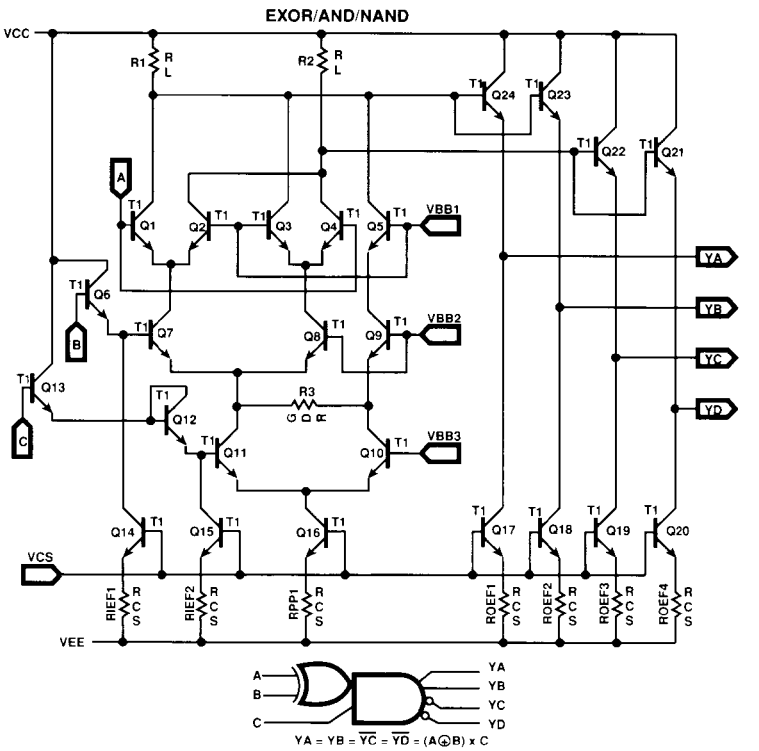
Figure 6. ECL/CML Bias Levels of the SH100E Family



Series Gating

An EXOR/AND/NAND macro circuit diagram is shown in Figure 7 to illustrate the application of three levels of series gating. Up to three levels of series gating can be used in a 10KH or 100K I/O levels with VEE = −5.2 V, nominal. If VEE = −4.5 V, nominal, then only 2-levels of series gating can be used for operation over the full temperature range.

Figure 7. An Example of 3 Levels of Series Gating



Macro Libraries

To support both the ECL and CML circuits, Siemens offers two distinct macro libraries.

Presently there are over 200 ECL and CML macros in the library. This number will grow with time as customers desire different macro logic functions. The macros range in complexity from simple OR/AND functions to the more complex multiplexers, adders, and decoders. A listing of currently available macros is provided in Table 4.

Table 4. ECL and CML Macros

Name	Function
Single Stage Gates	
ELOR1	Dual 2 Input OR
ELOR6	5 x 2 Input OR
ELOR2	2 Input OR (4 Outputs)
ELOR3	4 Input OR Gate (Twin Outputs)
ELOR4	Dual 4 Input OR
ELOR5	12 Input OR
ELNR1	Dual 2 Input NOR
ELNR5	2 Input NOR
ELNR2	Dual 4 Input NOR
ELNR3	4 Input NOR (Twin Outputs)
ELNR4	12 Input NOR
ELONR1	2 Input OR/NOR (Twin TRUE)
ELONR2	2 Input OR/NOR (Twin Complement)
ELONR3	2 Input OR/NOR
ELONR15	2 Input OR plus 2 Input NOR
ELONR12	2 Input OR/NOR 3 Input OR/NOR
ELONR4	4 Input OR/NOR (Single Outputs)
ELONR5	4 Input OR/NOR
ELONR13	4 Input OR plus 4 Input NOR
ELONR14	4 Input NOR plus 4 Input OR
ELONR6	5 Input OR/NOR
ELONR7	6 Input OR/NOR
ELONR8	8 Input OR/NOR
ELONR9	8 Input OR/NOR
ELONR10	12 Input OR/NOR
ELONR11	12 Input OR/NOR
ELNR01	2 Input NOR plus 2 Input OR
ELAN1	2 Input AND Gate (Single Output)
ELAN2	Dual 2 Input AND
ELAND1	2 Input AND plus 2 Input NAND
ELNDA1	2 Input NAND plus 2 Input AND
ELND1	2 Input NAND Gate (Single Output)
ELND2	Dual 2 Input NAND
CLOR1	2 Input OR, Differential
CLONR1	2 Input OR/NOR
CLONR2	4 Input OR/NOR
CLONR3	Triple 4 I/P OR/NOR w/Inhibit
CLONR4	Triple 4 I/P OR/NOR, Dual Inhibit
CLONR5	8 Input OR/NOR w/Inhibit
CLONR6	16 Input OR/NOR w/Inhibit
CLONR7	8 Input OR/NOR
Output Macros	
EOEONR1	2 Input OR/NOR
EOEOR1	2-2 OR Gate
EOEOR2	2-2 OR Gate
EOEONR2	25 ohm OR/NOR Driver
EOEONR3	4 Input OR/NOR
EOEONR4	5 Input OR/NOR
EOEONR5	8 Input OR/NOR
EOEOA1	2-2 OR/AND
EOEAO1	Dual AND/OR
EOEAO2	Dual AND/OR
EOEOXR1	2-2 OR/EXOR
EOEMX1	2:1 MUX
EOEMX2	Dual 2:MUX
Output Macros (Cont.)	
EOEMX3	2:1 MUX w/Enable (Low)
EOEMX4	4:1 MUX
EOEBF1	Differential Buffer
EOTBF1	TTL Output Converter (ECL to TTL)
EOTBF2	TTL Tristate Output Converter
EOLA1	D Latch with Reset
EOLA2	D Latch with Reset
EOFFD1	D Flip-Flop w/Reset
EOFFD2	D Flip-Flop w/Reset
Two-Stage Gates	
ELGA1	2-2 OR/AND, Gated
ELOA1	2-2 OR/AND
ELOA2	2-2-1-1 OR/AND
ELOA19	2-2-2 OR/AND
ELOA3	3-3 OR/AND
ELOA29	3-2-1 OR/AND
ELOA4	3-3-3 OR/AND
ELOA22	3-3-3 OR/AND
ELOA5	3-2-2-2 OR/AND
ELOA20	3-3-3-3 OR/AND
ELOA21	4-4 OR/AND
ELOA25	4-2-3-2-3 OR/AND
ELOA6	4-2-4-2 OR/AND
ELOA7	4-3-3-3 OR/AND
ELOA8	4-3-3-3 OR/AND
ELOA28	4-4-4-4 OR/AND
ELOA9	2-2-2-2-1-1-1-1 OR/AND
ELOA10	2-2-3-3-3 OR/AND
ELOA11	4-2-3-2-3 OR/AND
ELOA12	5-4-3-2 OR/AND
ELOA26	5-4-3-2 OR/AND
ELOA13	5-4-3-2-1 OR/AND
ELOA27	5-4-3-2-1 OR/AND
ELOA14	4-4-4-4 OR/AND
ELOA15	4-2-4-2-4-2 OR/AND
ELOA16	4-2-4-2-4-2-4-2 OR/AND
ELOA17	5-4-3-2-1 OR/AND
ELOA18	6-6-4-4-2-2 OR/AND

Continued

Name	Function
Two Stage Gates (Cont.)	
ELOA24	6-5-4-3-2-1 OR / AND
ELOA30	2 Input OR, 2 Input AND
ELAO1	3-3 AND / OR
ELAO11	3-3 AND / OR
ELAO2	2-3-4-4 AND / OR w/Enable
ELAO13	2-3-4-4 AND / OR w/Enable
ELAO6	3-2-2 AND / OR
ELAO3	3-3-3 AND / OR
ELAO10	3-3-3 AND / OR
ELAO4	3-3-2-1 AND / OR
ELAO12	3-3-2-1 AND / OR
ELAO5	3-3-3-3 AND / OR
ELAO9	3-3-3-3 AND / OR
ELAO7	3-2-2-2-2-3 AND / OR
ELAO14	3-2-2-2-2-3 AND / OR
ELAO15	4-3-3-3-2 AND / OR
ELAO8	5-5-5-5 AND / OR
ELGO1	Gated OR
CLOA1	OR-AND Gate (2 OR, 1 AND)
CLOA3	3-3-3 AND / OR
CLOAND1	OR-AND / NAND Gate (2×4)
CLOAND2	OR-AND / NAND Gate (2×4)
Exclusive OR Functions	
ELXR1	3 Input EXOR / EXNOR
ELXR4	3 Input EXOR / EXNOR
ELXR2	4 Input EXOR
ELXR3	6 Input EXOR
ELOXR1	2-2 OR / EXOR
ELAXNR1	2-1-1-2 OR / AND / XNOR
ELAXNR2	Dual 2-2 OR / AND / EXNOR
ELAXNR3	Dual 2-2 OR / AND / EXNOR
ELXNR1	4 Input EXNOR
ELXNR2	6 Input EXNOR
ELOAXR1	2-1-1-2 OR / AND / XOR
ELXRA1	2-1 XOR / AND / NAND
ELXRA2	2-1 XOR / AND / NAND
ELAXR1	2-1 AND / EXOR
CLXR1	2 Input EXOR
CLXRXR1	2-2 OR / EXOR
CLONRXR1	8 Input OR / NOR / EXOR
Multiplexers	
ELMX1	2:1 MUX
ELMX2	2:1 MUX w/Active Low Enable
ELMX10	2:1 MUX w/Enable (Low)
ELMX11	2:1 MUX w/Enable (High)
ELMX3	2:1 MUX w/Gated Inputs
ELMX4	2:1 MUX w/Different Inputs and Different MUX Control
ELMX5	Dual 2:1 MUX w/Common Select
ELMX6	Dual 2:1 MUX w/Common Select
ELMX13	Dual 2:1 MUX w/Enable (Low)
ELMX7	Dual Differential 2:1 MUX
ELMX15	Expandable 2:1 MUX
ELMX16	Expandable 2:1 MUX
ELMX17	Expandable 2:1 MUX
ELMX18	Expandable 2:1 MUX (Coder) and Dual 2:1 MUX
ELMX14	Triple 2:1 MUX w/Common Select
ELMX12	Triple 2:1 MUX
ELMX8	Quad 2:1 MUX
ELMX9	Quad 2:1 MUX
ELMX20	4:1 MUX
ELMX21	4:1 MUX w/Enable (Low)
ELMX22	4:1 MUX w/Enable (Low)
ELMX23	4:1 MUX w/Enable (High)
ELMX26	4:1 MUX w/Enable (High)
ELMX24	4:1 MUX w/Differential Select
ELMX25	Dual 4:1 MUX
ELMX27	Expandable 4:1 MUX
ELMX28	Expandable 4:1 MUX
ELMX29	Expandable 4:1 MUX
ELMX40	8:1 MUX w/Enable (High)
ELMX41	8:1 MUX w/Enable (High)
ELMX42	Expandable 8:1 MUX
ELMX43	Expandable 8:1 MUX

Name	Function
Multiplexers (Cont.)	
ELMX44	Expandable 8:1 MUX
CLMX1	2-Bit MUX
CLMX2	2-Bit MUX (Diff. Addrs.)
CLMX3	2-Bit MUX (Diff. Data)
CLMX21	4-Bit MUX
CLMX22	4-Bit MUX (Diff. Data)
CLMX23	2×4-Bit MUX
CLMX41	8-Bit MUX (Inverted O / P)
CLMX42	8-Bit MUX (Diff. I / P)
Decoders	
ELDC1	1-of-4 Decoder w/Enable (Low)
ELDC5	1-of-4 Decoder w/Enable (Low)
ELDC2	1-of-4 Decoder w/Enable (High)
ELDC4	1-of-4 Decoder w/Enable (High)
ELDC3	1-of-4 Decoder (High)
ELDC6	1-of-4 Decoder w/Enable (Low)
ELDC7	1-of-4 Decoder w/Enable (High)
ELDC8	Expandable 4-1 MUX (Coder) w/Enable
ELDC9	8-3 Encoder
ELDC10	Expandable 8:1 MUX (Coder)
CLDMX1	Demultiplexer 1-of-4 w/2 I / Ps
CLDMX2	Demultiplexer 1-of-2 w/Inhibit
Latches	
ELLA1	D Latch w/Reset
ELLA2	D Latch w/Clk Enable and Reset
ELLA3	3 Data Input D Latch
ELLA4	D Latch w/Data MUX and Reset
ELLA14	D Latch w/MUX
ELLA5	D Latch w/Gated Data and Reset
ELLA12	D Latch w/ASYN Set
ELLA6	D Latch w/Reset
ELLA7	Gated 4-Way D Latch
ELLA8	Dual D Latch, Common Clock, Transparent High
ELLA9	Dual D Latch, Common Clock, Transparent Low
ELLA10	Dual D Latch w/Reset
ELLA13	3 D Latches, w/Common Clk and Reset
ELLA15	3 D Latches, w/Common Clk and Set
ELLA11	Scan D Latch w/ASYNC Set
ELSR1	NOR Latch
CLLA1	D Latch-Positive Clock Cntl
CLLA2	D Latch-Negative Clock Cntl
CLLA3	2 Bit D Latch-Positive Clock Cntl
CLLA4	2 Bit D Latch-Positive Clock Cntl w/Inverted Outputs and Reset
CLLA5	2 Bit D Latch-Negative Clock Cntl
CLLA6	2 Bit D Latch-Negative Clock Cntl w/Inverted Outputs and Reset
CLLA7	4 Bit D Latch-Positive Clock Cntl
CLLA8	4 Bit D Latch-Negative Clock Cntl
CLLA9	8 Bit D Latch-Positive Clock Cntl
CLLA10	8 Bit D Latch-Negative Clock Cntl
CLLA11	2 Bit D Latch with Reset
CLLA12	2 Bit D Latch w/Set
CLSR1	Unclocked RS Latch
Flip-Flops	
ELFFD1	D Flip-Flop, Positive Edge Triggered
ELFFD2	D Flip-Flop, Negative Edge Triggered
ELFFD16	D Flip-Flop w/Set
ELFFD17	D Flip-Flop w/Set
ELFFD18	D Flip-Flop w/Set
ELFFD3	D Flip-Flop w/Set and Reset
ELFFD4	D Flip-Flop w/MUX
ELFFD5	D Flip-Flop w/EXOR
ELFFD6	D Flip-Flop w/Set and Reset
ELFFD7	D Flip-Flop w/Reset
ELFFD8	D Flip-Flop w/MUX
ELFFD9	D Flip-Flop, Neg. Edge Trig. w/Reset
ELFFD19	D Flip-Flop w/Reset
ELFFD10	D Flip-Flop, Neg. Edge Trig. w/Data MUX and Reset
ELFFD20	D Flip-Flop w/MUX

Name	Function
Flip-Flops (Cont.)	
ELFFD11	Scan D Flip-Flop
ELFFD12	D Flip-Flop w/ASYN Set and Enable
ELFFD13	D Flip-Flop w/Diff. Clock
ELFFD14	D Flip-Flop w/Diff. Clock
ELFFD15	D Flip-Flop w/Diff. Clock and Data
CLFFD1	D M-S Flip-Flop w/Reset Input
CLFFD2	D M-S Flip-Flop w/2-Bit MUX, Set
CLFFD3	2 D M-S Flip-Flops w/Separate Set and Common Clock
CLFFD4	Positive Edge Trig. 2 D M-S Flip-Flop w/Separate Set and Common Clock
CLFFD6	4 Bit Neg. Edge Trig. M-S Flip-Flop
CLFFD5	4 Bit Neg. Edge Trig. M-S Flip-Flop
CLFFD8	8 Bit Neg. Edge Trig. M-S Flip-Flop
CLFFD7	8 Bit Neg. Edge Trig. M-S Flip-Flop
CLFFD9	Differential D - M-S Flip-Flop w/Reset
CLFFD10	Differential MUX - D - M-S Flip-Flop w/Reset and Set Inputs
ELFFD11	D Flip-Flop w/Reset and Diff. Clock
ELFFD12	D Flip-Flop w/Set and Diff. Clock
Adders and Carry Look Ahead	
ELAD1	Full Adder
ELAD2	Full Adder, Gated Inputs
ELAD3	Half Adder, Gated Inputs
ELAD4	3-Bit Adder, Gated Inputs
ELAD8	3-Bit Adder
ELAD5	3-Bit Adder, Gated Inputs
ELAD6	Gated Adder
ELAD7	Triple Full Adder
ELCL1	2 Bit Look Ahead Carry
CLAD1	Full Adder
CLAD2	2×2-Bit Full Adder
CLAD3	Half-Sum Generator, Dual Propagate
CLAD4	2-Bit Sum Generator
CLCL1	4-Bit Carry Look Ahead
CLCL2	8-Bit Carry Look Ahead
Buffers/Drivers	
ELBF1	Driver Buffer, 6 Outputs
ELBF2	Differential Drvr Buffer, 3 Diff. Outputs
ELBF3	Differential Line Rcvr
ELBF4	Differential Line Rcvr, Clk Pulse Generators
ELBF5	Differential Clk Generator (5 Gates)
ELBF6	Differential Clk Generator (6 Gates)
ELBF7	Differential Clk Generator (6 Gates plus Ext. Gates)
CLBF1	3-Input Buffered OR / NOR
CLBF2	Differential Buffer
CLBF3	Differential Amplifier
ELEC1	Dual ECL-CML Converter
CLCE1	Triple CML-ECL Converter
Low Power 25 ohm Cutoff Drivers	
EOEOR3	2 Input OR
EOEOR4	4 Input OR
EOEOR5	2-2 OR Gate
EOEOR6	2-2 OR Gate
EOEOR7	5 Input OR
EOEOR8	8 Input OR
EOEOA2	2-2 OR / AND
EOEAO3	Dual AND / OR
EOEMX5	2:1 MUX
EOEMX6	Dual 2:MUX
EOEMX7	4:1 MUX
EOEBF2	Differential Buffer
COEOR1	50 ohms OR / NOR - O / P Converter w/4 I / Ps
COEOR2	25 ohms OR / NOR - O / P Converter w/4 I / Ps
COEOR3	50 ohms 4 Input OR / NOR
COEOR4	50 ohms 4 Input OR / NOR
COEMX1	2-Bit MUX with Additional Output Converter
COEONR1	OR / NOR w/4 Inputs and Additional O / P Converter

Continued

Name	Function
Low Power 25 ohm Cutoff Drvrs (Cont.)	
COEMX2	Diff. MUX w/ O/P Converter
COTBF1	CML to TTL O/P Converter
COTBF2	TTL Tristate O/P Converter
Input Macros	
EIEO1	2-Input OR
EIENR1	2-Input NOR
EIEONR1	2-Input OR/NOR
EIEBF1	Input Buffer
EIEBF2	Input Buffer
EIEBF3	Differential Buffer
EIEBF4	Differential Buffer
EIEBF5	Differential Buffer
EIEBF6	Input Buffer
EITBF1	TTL Input Converter (TTL to ECL)
CIEBF1	ECL 100k/ECL 10 kH Input Converter
CIEBF2	Input Differential Amplifier
CIEONR1	ECL 100k/ECL 10 kH Input Converter w/2-Input OR/NOR
CITBF1	TTL Input Converter (TTL to CML)
Pad Macros, Output	
EPEOT1	25 ohm Pad Macro
EPEOT2	50 ohm Pad Macro
EPEBI3	50 ohm Bidirectional Pad Macro
EPEBI4	25 ohm Bidirectional Pad Macro
EPEOT5	STECL Pad Macro - 0 ohms Series
EPEOT6	STECL Pad Macro - 20 ohms Series
EPEOT7	STECL Pad Macro - 40 ohms Series
EPTOT1	TTL Output Pad Macro
EPTOT2	TTL Open Collector Output Pad Macro
EPTBI1	TTL Bidirectional Pad Macro
CPEOT1	ECL 10 kH/100 k - 50 ohms Pad Macro
CPEOT2	ECL 10 kH/100 k - 50 ohms Pad Macro w/additional Delay
CPEOT3	ECL 10 kH/100 k - 25 ohms Pad Macro
CPEOT4	ECL 10 kH/100 k - 25 ohms Pad Macro w/additional Delay
CPEOT5	Source Terminated ECL 10 kH/100 k - 50 ohm Pad Macro
CPEOT6	Edge Delayed ECL 10 kH/100 k - 50 ohm Source Terminated Pad Macro
CPEBI1	ECL 10 kH/100 k Bidirectional - 50 ohm Pad Macro
CPEBI2	Edge Delayed ECL 10 kH/100 k - 50 ohm Bidirectional
CPTOT1	TTL Output Pad Macro
CPTOT2	TTL Open Collector Output Pad Macro
CPTBI1	TTL Bidirectional Pad Macro
Pad Macros, Input	
EPEIN1	ECL 10 kH/100 k Input Pad Macro
EPEIN2	ECL 10 kH/100 k Input Pad Macro used for Diff. Structures
EPEIN3	ECL 10 kH/100 k Input Pad Macro with High ESD Protection
EPEIN4	ECL 10 kH/100 k Differential Input Pad Macro w/High ESD Protection
EPTIN1	TTL Input Pad Macro
CPEIN1	ECL 10 kH/100 k Input Pad Macro
CPEIN2	ECL 10 kH/100 k Input Pad Macro for Diff. Structures
CPEIN3	ECL 10 kH/100 k Input Pad Macro w/High ESD Protection
CPEIN4	ECL 10 kH/100 k Differential Input Pad Macro w/High ESD Protection
CPTIN1	TTL Input Pad Macro

CAD

Siemens offers a comprehensive CAD system resident on an internal VAX8700/8550 mainframe cluster.

The interface to the system can be either a captured schematic or a fully simulated netlist generated from a Daisy, Mentor or Valid workstation. As shown in Figure 8, the CAD system supports the following design activities.

1. Schematic Capture
2. Logic Simulation, including Timing Verification
3. Placement and Routing
4. Fault Simulation
5. Speed/Power Programming
6. Test Program generation
7. Back Annotation of actual wiring delays
8. Mask tape generation

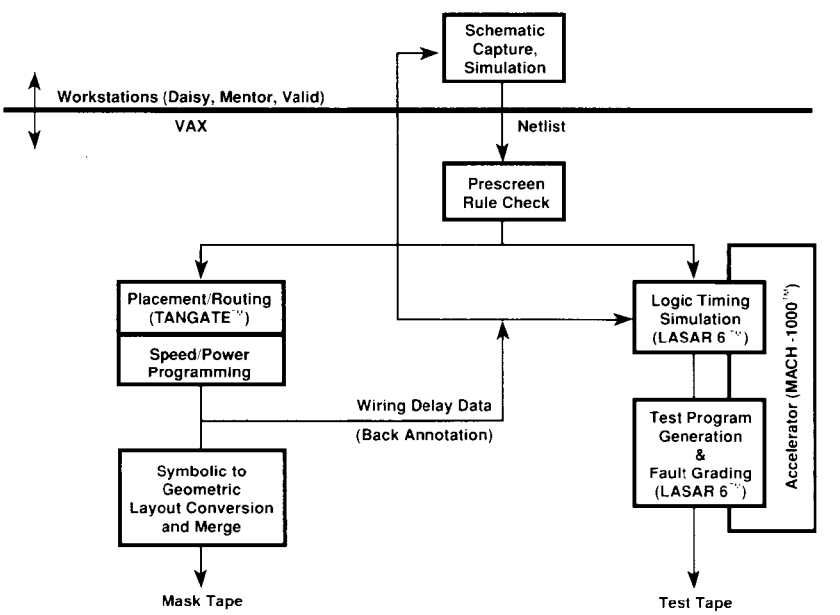
Upon receipt of your captured schematic or simulated netlist, a prescreen rule check is performed to insure that the design adheres to all logic rules surrounding fanout, I/O usage and similar items. Next logic/timing simulation is performed and/or verified depending upon your input using the LASAR 6 reference simulator.

Subsequently, test patterns are created, fault grading performed, and a test program is generated in the manner indicated in Figure 8. Depending upon the projected run times to accomplish the simulation and fault grading tasks, Siemens also may use the MACH 1000 hardware accelertor tied to the VAX computers in the CAD system. This dedicated accelerator realizes run time improvements of up to 1000X, greatly reducing the time required for such computer intensive activities as fault grading.

Once the logic has been verified and critical path analysis completed, the layout program accesses the models for the macros contained in your schematic first placing each macro and then routing the interconnect wiring. The resistor network used for desired speed/power management is then implemented. At this point, the actual delays due to the interconnect wiring are known, and this data is back annotated into either the LASAR 6 simulator or your workstation for further confirmation that all critical speed paths have been met.

Beyond this point, all that remains is the conversion of the layout to actual geometric data and the creation of a mask tape used for the creation of your personalized set of masks for wafer fabrication. Also a test program is generated using simulation and I/O data of the design.

Figure 8. Siemens ECL CAD System



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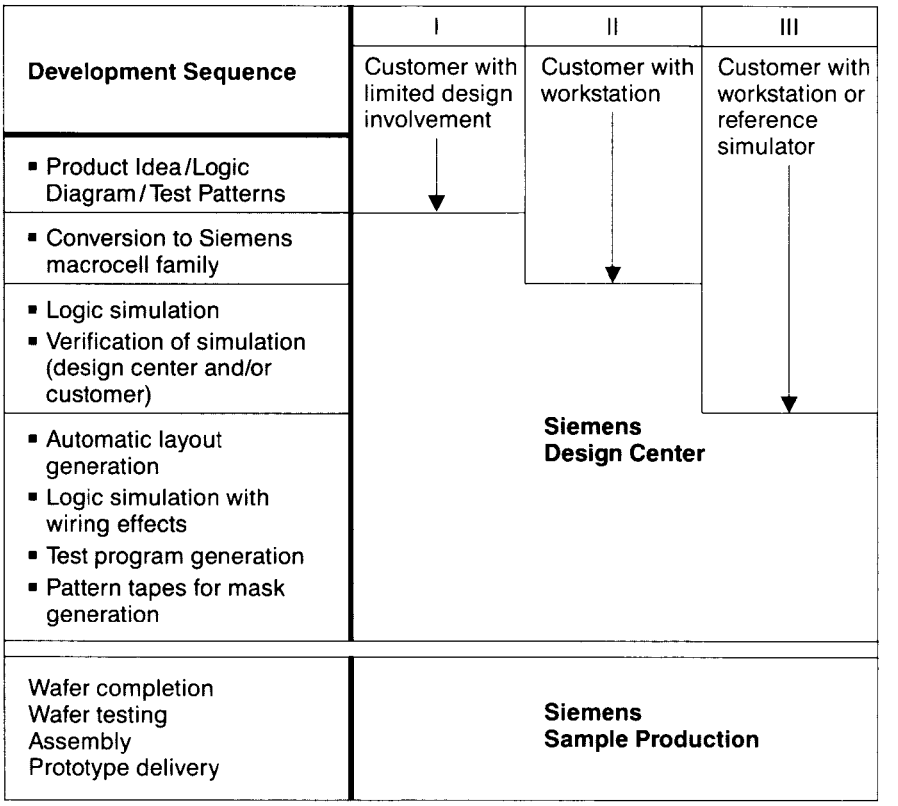
TANGATE is a trademark of the Cadence Design Systems, Inc.
MACH 1000 is a trademark of the Zycad Corporation.

Design Interface

Customer engineers can interface with Siemens in three basic modes. These three modes, as illustrated in Figure 9, are:

1. A customer may wish limited design involvement and provide us with a product idea and/or logic diagram with test vectors but no EWS captured schematic simulation results.
2. Alternatively, the customer may provide the above (1) plus a netlist capturing his logic diagram using Siemens macros.
3. Again alternatively, the customer may interface with us following his own schematic capture, logic/timing simulation, and perhaps fault grading.

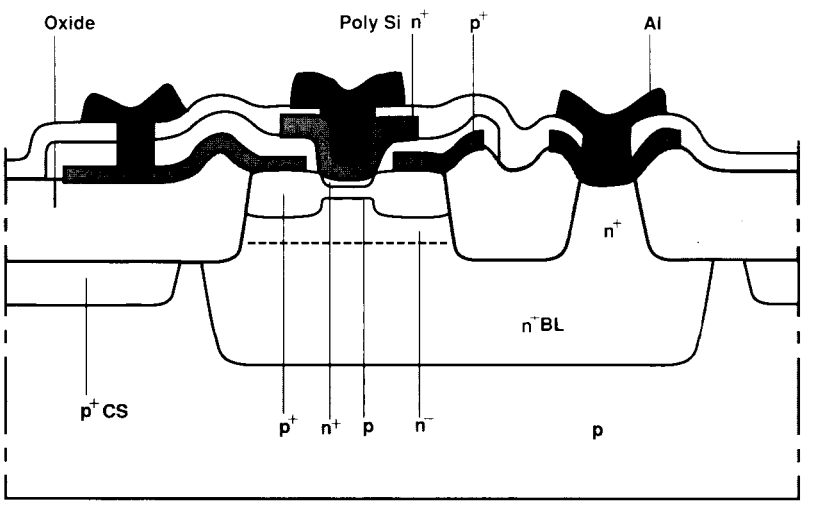
Figure 9. Customer Interfaces to the Siemens Design Center



FAB Process

The Siemens OXIS-IIIH device cross section is shown in Figure 10. OXIS IIIH is a third generation oxide isolated process featuring double poly, self-aligned transistors with polysilicon contacts for collector, base, and emitter regions. These features provide low base-collector region capacitance and low base resistance and together with a small emitter area contribute to a high gain band width product, f_T of 7 GHz.

Figure 10. Cross Section of npn Transistor OXIS IIIH



Packaging

Siemens packaging allows for good thermal resistivity as shown in Figure 11, along with excellent electrical characteristics for pins (inductive, resistive, and capacitive coupling). Table 5 shows actual and planned packages for the SH100E family. An example diagram of the Siemens 319 CPGA (Ceramic Pin Grid Array) is shown in Figure 12.

Table 5. Actual and Planned Packages for SH100E Family Members

Complexity	1,500	2,500	5,000	10,000
Pad Count	132	172	224	360
PGA	88	144	224	319
LCC	X	X		
LLCC	X	X	X	X

X = Planned

Power Dissipation

The power dissipation depends upon the selection of the master array, the mix of CML and ECL macros, their speed/power programming and the population of the chip. The relationships for detailed power calculations are provided in the Siemens ECL/CML Design Manual.

Figure 11. SH100E7 Package Thermal Characterization (319 CPGA)

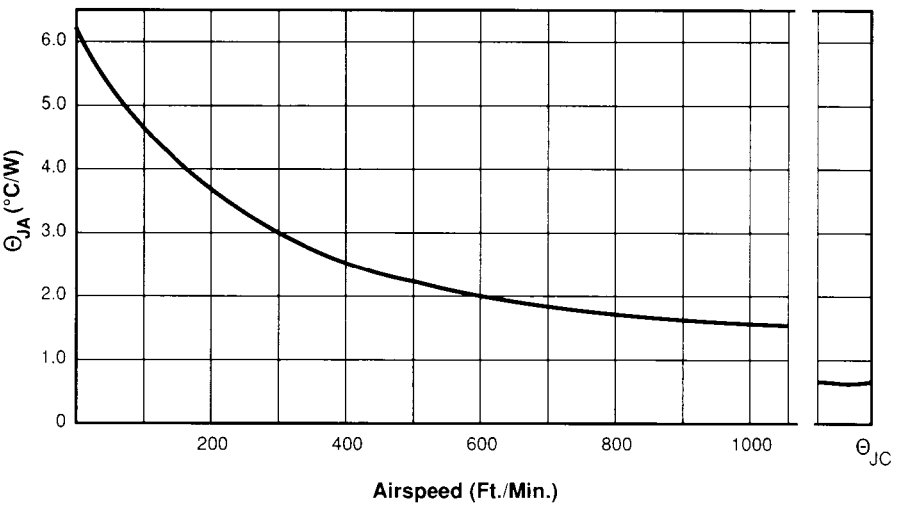
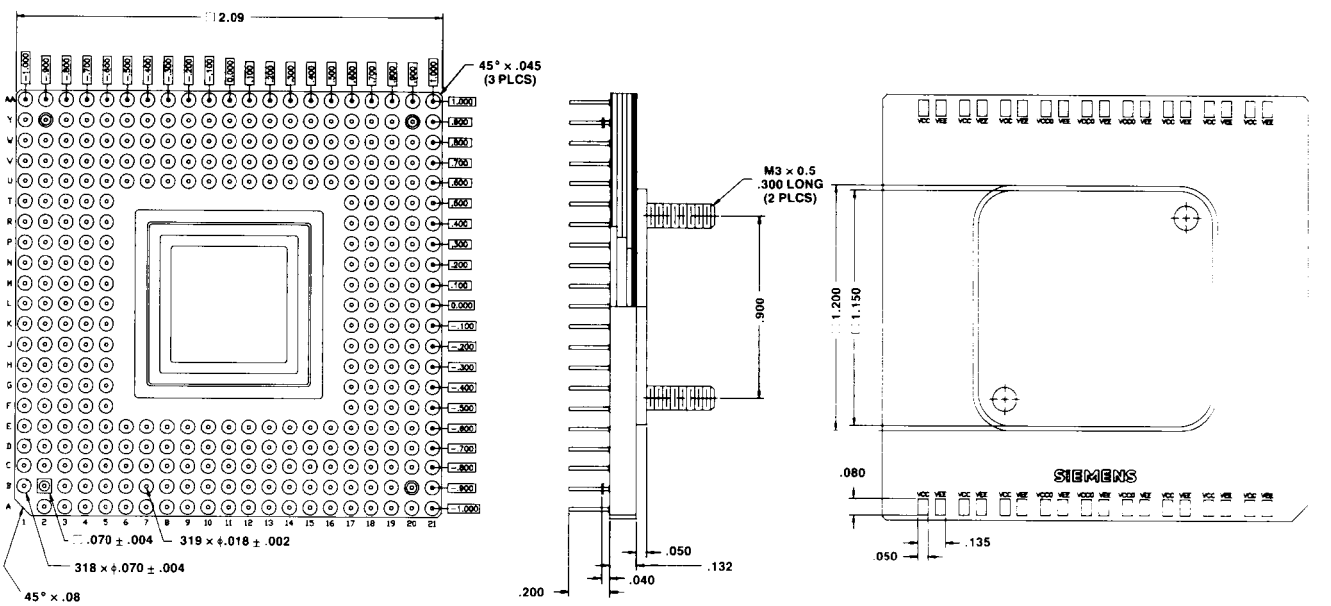


Figure 12. 319 Ceramic Pin Grid Array



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