SIEMENS

256 x 8-Bit Static CMOS RAM

SAB 81C50
SAB 81C51

CMOS IC

Type	Ordering Code	Package	Chip Select
SAB 81C50-P	Q67100-H8113	P-DIP-16	$\overline{CS}$
SAB 81C51-P	Q67100-H8114	P-DIP-16	CS

The SAB 81C50/51 are 2048-bit static random access memories (RAM), organized as 256 words by 8 bits, manufactured using CMOS silicon gate technology. The multiplexed address and data bus allows to interface directly with the 8-bit organized processors and microcomputers, for example with SAB 8085, SAB 8086, SAB 8088, SAB 8048, SAB 80C48, SAB 8051. Low standby power dissipation minimizes system power requirements.

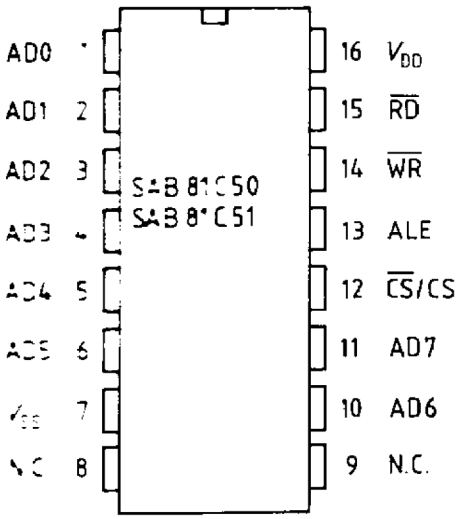
Features

- 256 x 8-bit organization
- Multiplexed address and data bus
- Tristate address/data lines
- Address latches on-chip
- Very low power consumption

  Standby: 1 µA at 6 V
  Operation: 500 µA typically
- Wide supply voltage range: 2.5 V to 6 V
- Data retention: 1 V
- SAB 81C50 Chip select low active
- SAB 81C51 Chip select high active

Pin Configurations

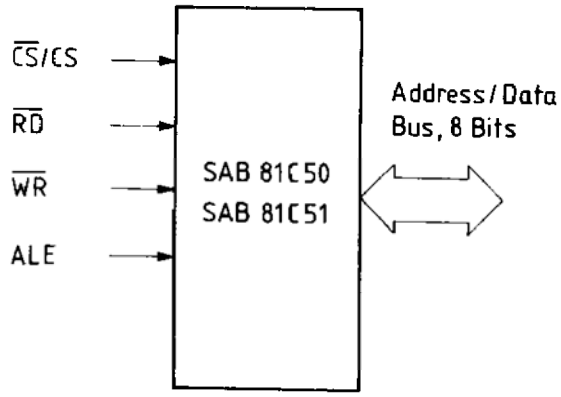
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1...6, 10, 11	AD0 to AD7	**Address** and data lines (multiplexed)
12	$\overline{CS}$, CS	**Chip Select** $\overline{CS}$ = active low; (SAB 81C50) CS = active high (SAB 81C51)
13	ALE	**Address Latch Enable**
14	$\overline{WR}$	**Write Enable**
15	$\overline{RD}$	**Read Enable**
16	V_{DD}	Power supply (2.5 V...6 V)
7	V_{SS}	Ground (0 V)
8, 9	N.C.	Not connected

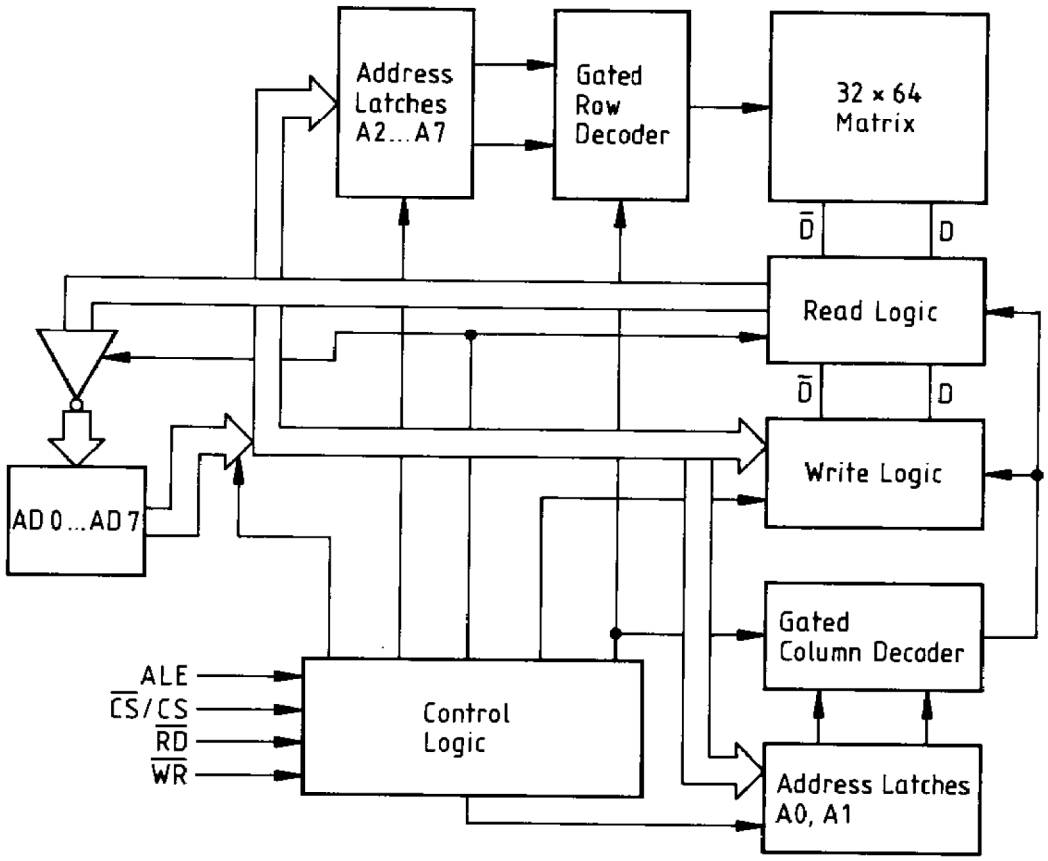
Logic Symbol



Truth Table for Control and Data Bus Pin Status

CS	CS	RD	WR	AD0...AD7 during data portion of cycle	Function
H	L	X	X	tristate	none
L	H	L	H	data from memory	read
L	H	H	L	data to memory	write
L	H	H	H	tristate	none

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	−20 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C
Supply voltage referred to GND (V_{SS})	V_S	0 to 7	V
Total power dissipation	P_{tot}	250	mW
All input and output voltages		−0.8 to V_{DD} +0.8	V

DC Characteristics

$T_A = -25\,°C$ to $70\,°C$; $V_{DD} = 2.5$ V to 6 V; $V_{SS} = 0$ V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Standby supply current	I_{DD}			1	µA	$\overline{CS} = 0$ V, $CS = V_{DD}$, ALE = 0 V
Operating supply current	I_{DD}		500		µA	100 kHz ALE
Operating supply voltage	V_{DD}	2.5		6	V	
Standby voltage	V_{DD}	1.0			V	for data retention
Input leakage current	I_{IL}			1	µA	$V_I = 0$ to 6 V
Output leakage current	I_{OL}			1	µA	$V_O = 0$ to 6 V high impedance
L-input voltage	V_{IL}	−0.8		0.6	V	V_{DD}= 2.5 V to 4.5 V
L-input voltage	V_{IL}	−0.8		0.8	V	$V_{DD} = 4.5$ V to 6 V
H-input voltage	V_{IH}	0.6 x V_{DD}		V_{DD} +0.8	V	
H-input voltage	V_{IH}	2.0		V_{DD} +0.8	V	$V_{DD} = 5$ V
L-output voltage	V_{OL}			0.4	V	$I_{OL} = 2$ mA
H-output voltage	V_{OH}	0.75 x V_{DD}			V	$I_{OH} = 2$ mA

AC Characteristics

$T_A = -25\,°C$ to $70\,°C$; $V_{DD} = 2.5\ V$ to $4.5\ V$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit values		Unit
		min.	max.	
ALE pulse width	t_{LL}	400		ns
Address setup before ALE	t_{AL}	500		ns
Address hold from ALE	t_{LA}	150		ns
$\overline{RD}$, WR pulse width	t_{CC}	1000		ns
Data setup before $\overline{WR}\uparrow$	t_{DW}	1000		ns
Data hold after $\overline{WR}\uparrow$	t_{WD}	300		ns
Data hold after $\overline{RD}\uparrow$	t_{DR}	0		ns
$\overline{RD}\downarrow$ to data OUT	t_{RD}		900	ns
Address float to $RD\downarrow$	t_{AFC}	0		ns
CS or $\overline{CS}$ before ALE	t_{CS}	400		ns
CS or $\overline{CS}$ after $\overline{WR}$ or $\overline{RD}$	t_{SC}	400		ns
ALE to $\overline{RD}$ – $\overline{WR}$ control	t_{LC}	300		ns
$\overline{RD}$ – $\overline{WR}$ control to ALE high	t_{CL}	400		ns

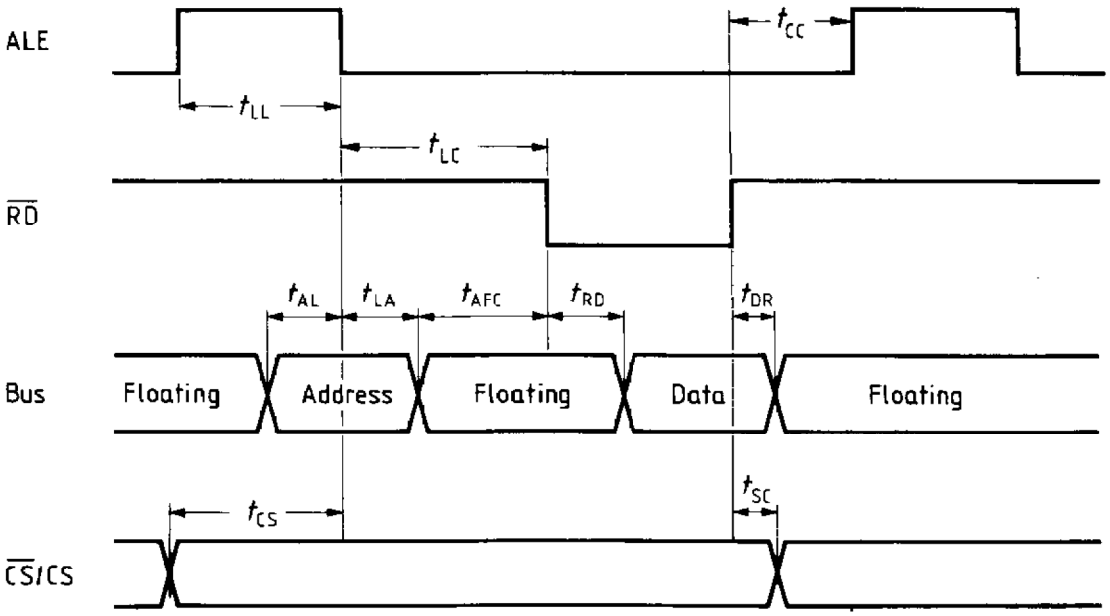
AC Characteristics

$T_A = -25\,°C$ to $70\,°C$; $V_{DD} = 4.5\ V$ to $6\ V$; $V_{SS} = 0\ V$

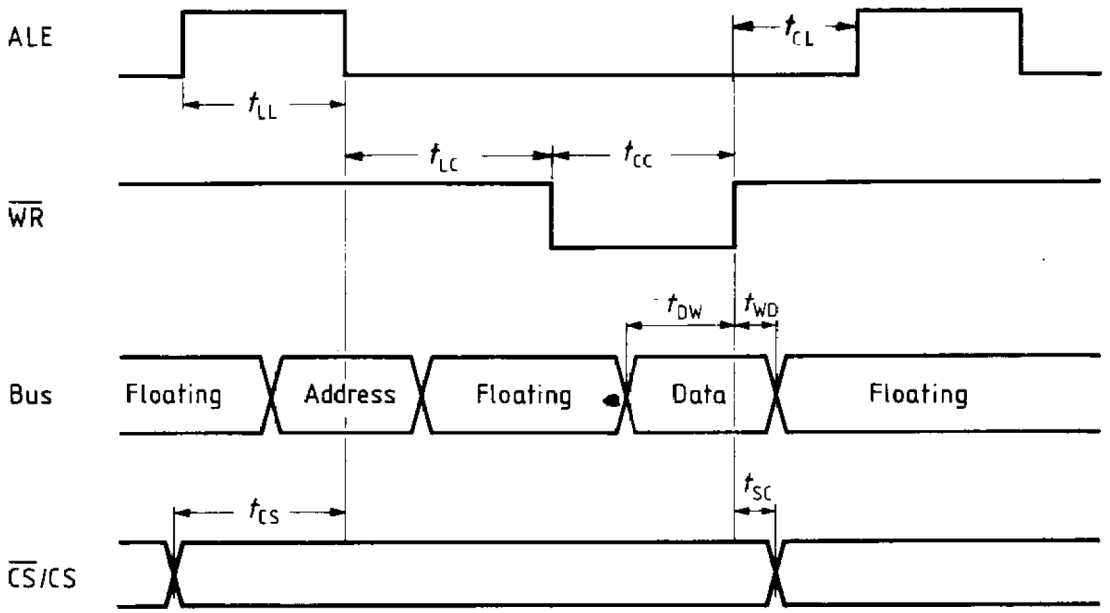
Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{LL}	60		ns
Address setup before ALE	t_{AL}	15		ns
Address hold from ALE	t_{LA}	40		ns
$\overline{WR}$ pulse width	t_{CC}	150		ns
Data setup before $\overline{WR}\uparrow$	t_{DW}	100		ns
Data hold after $\overline{WR}\uparrow$	t_{WD}	25		ns
Data hold after $\overline{RD}\uparrow$	t_{DR}	0	95	ns
$\overline{RD}\downarrow$ to data out	t_{RD}		150	ns
Address float to $\overline{RD}\downarrow$	t_{AFC}	0		ns
$\overline{CS}$ before ALE SAB 81C50-P	t_{CS}	30		ns
SAB 81C51-P	t_{CS}	60		ns
$\overline{CS}$ after $\overline{WR}$ or $\overline{RD}$	t_{SC}	30		ns
ALE to $\overline{RD}$ – $\overline{WR}$ control	t_{LC}	100		ns
$\overline{RD}$, $\overline{WR}$ control to ALE high	t_{CS}	30		ns

Timing Waveforms

Read



Write



SAB 81C50 as External Data Memory of SAB 8051