DATA SHEET

SAA7500
Digital satellite radio broadcasting tuner decoder (SAT-2)

Product specification
File under Integrated Circuits, IC01

September 1989

Philips
Semiconductors

PHILIPS

Digital satellite radio broadcasting tuner decoder (SAT-2)

SAA7500

GENERAL DESCRIPTION

The SAA7500 performs a decoder function for digital satellite sound broadcasting tuners. It is designed to decode one of 16 stereo channels broadcasting audio signals in accordance with the German standard - **Technische Richtlinie ARD/ZDF Nr. 3R1**.

Features

- Clock recovery
- Differential decoding
- Main frame synchronization
- Swapping half-frames in case of inversion
- Unscrambling
- Demultiplexing
- Subframe synchronization
- Error correction and concealment
- Scale factor decoding with error correction
- Shift into the original values using the scale factors
- Mute in case of synchronization loss

QUICK REFERENCE DATA

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	V_{DD}	4.5	5.5	V
Power dissipation	P_{tot}		500	mW
Clock frequency	T_{20N}	20.48		MHz

PACKAGE OUTLINE

68-lead plastic leaded chip carrier (PLCC); ‘pocket’ version (SOT188AA); SOT188-2; 1996 September 05.

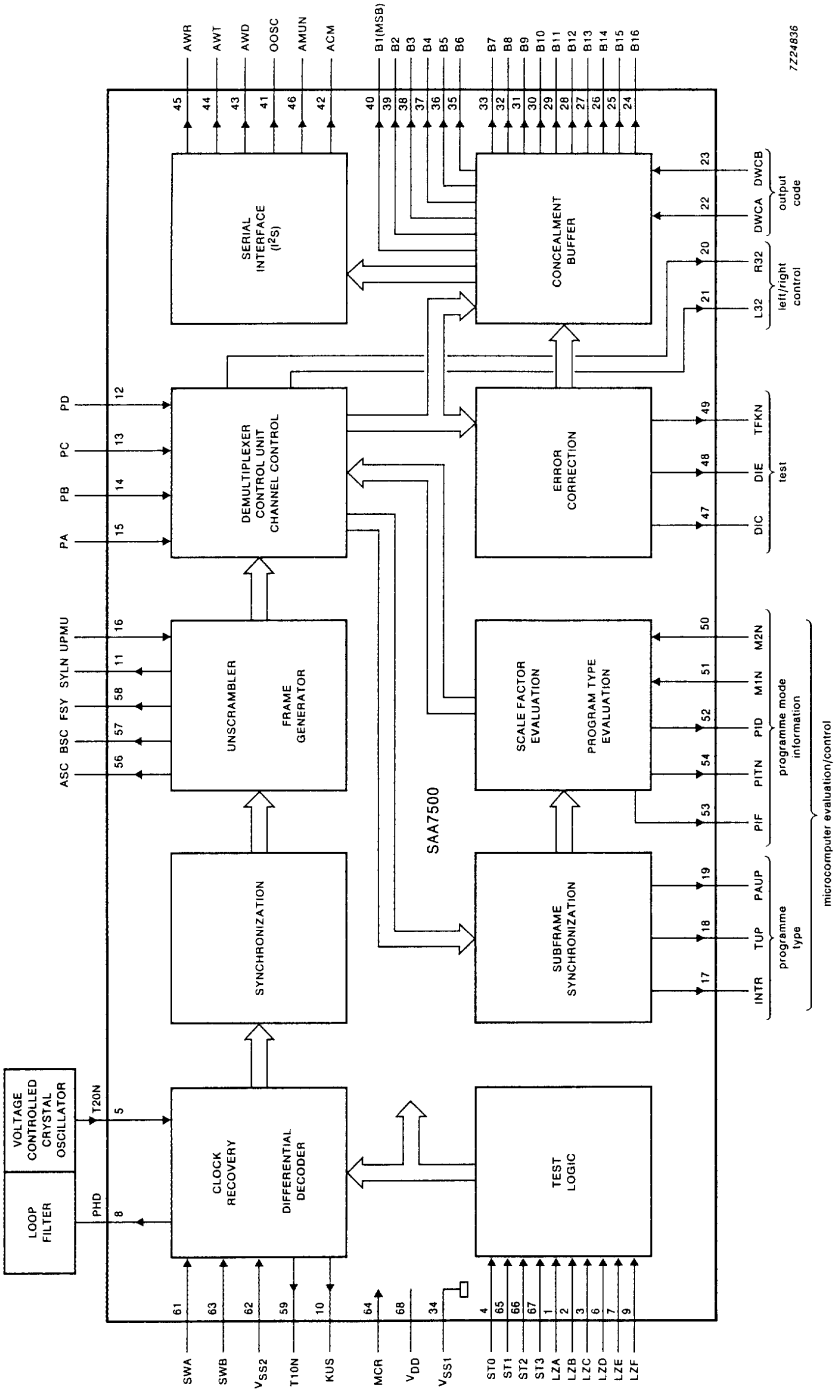


Fig.1 Block diagram.

PINNING

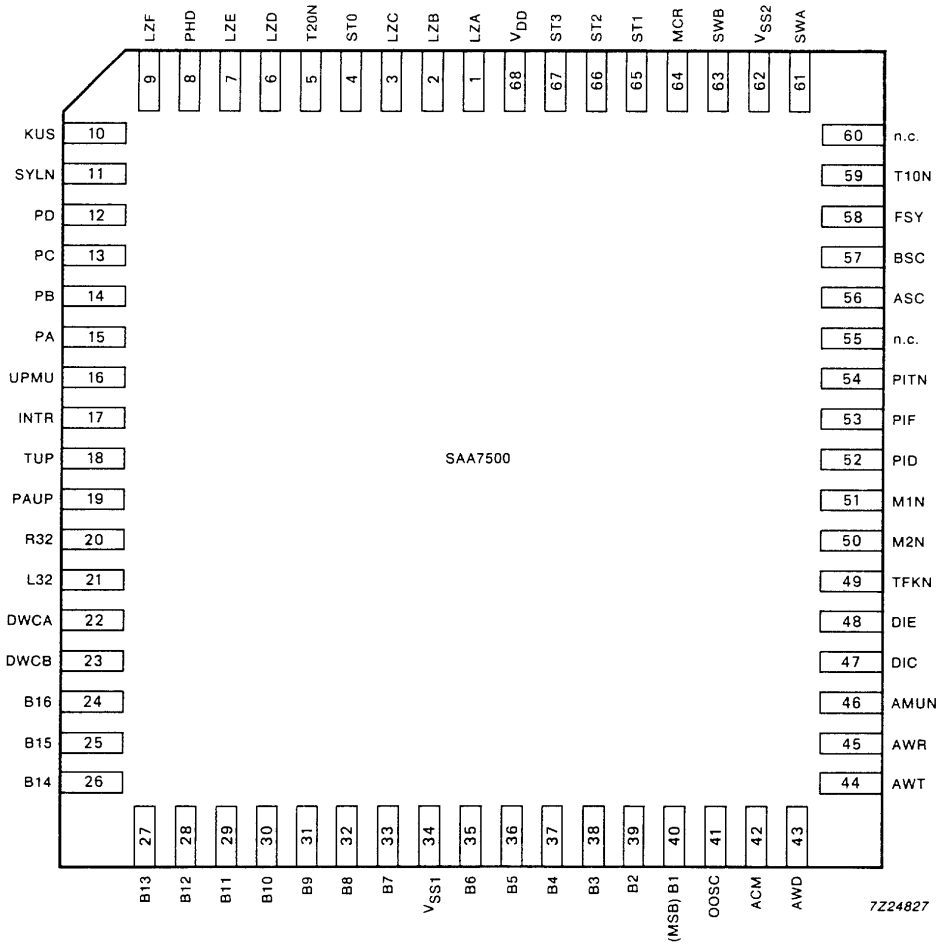


Fig.2 Pinning diagram; for pin functions see next page.

Pin functions

(1) = CMOS level input. (2) = TTL level input. (3) = CMOS level input with pull down resistor.

PIN NO.	MNEMONIC		DESCRIPTION
1	LZA	I(3)	phase adjustment for the internal clock.
2	LZB	I(3)	phase adjustment for the internal clock.
3	LZC	I(3)	phase adjustment for the internal clock.
4	STO	I(3)	control input for testing.
5	T20N	I(1)	20.48 MHz clock input from voltage controlled oscillator (VCX).
6	LZD	I(3)	control input for testing.
7	LZE	I(3)	control input for testing.
8	PHD	O	phase control signal for VCX.
9	LZF	I(3)	control input for testing.
10	KUS	O	test output (A'B' swap).
11	SYLN	O	synchronization indication flag.
12	PD	I(2)	programme number input selector (MSB).
13	PC	I(2)	programme number input selector.
14	PB	I(2)	programme number input selector.
15	PA	I(2)	programme number input selector (LSB).
16	UPMU	I(2)	mute input (controlled by microcomputer).
17	INTR	O	interrupt flag for microcomputer.
18	TUP	O	programme type interface (clock).
19	PAUP	O	programme type interface (data).
20	R32	O	multiplex control signal for right channel.
21	L32	O	multiplex control signal for left channel.
22	DWCA	I(3)	DA-converter mode select input.
23	DWCB	I(3)	DA-converter mode select input.
24-33	B16-7	O	audio data for parallel interface, bits 16 (LSB) to 7.
34	V_{SS1}	I	ground (supply).
35-40	B6-1	O	audio data for parallel interface, bits 6 to 1 (MSB).
41	OOSC	O	4.096 MHz clock output.
42	ACM	O	concealment flag (for SAA7220P/C).
43	AWD	O	audio data (for SAA7220P/C).
44	AWT	O	bit clock (for SAA7220P/C).
45	AWR	O	word select signal (for SAA7220P/C).
46	AMUN	O	mute signal (for SAA7220P/C).
47	DIC	O	data output for testing.
48	DIE	O	data output for testing.

PIN NO.	MNEMONIC		DESCRIPTION
49	TFKN	O	burst clock for test data.
50	M2N	I(2)	channel mode select input.
51	M1N	I(2)	channel mode select input.
52	PID	O	programme information (PI) interface output (data).
53	PIF	O	programme information (PI) interface output (window signal).
54	PITN	O	programme information (PI) interface output (clock).
55	n.c.		not connected.
56	ASC	O	data output for 10.24 Mbit/s interface.
57	BSC	O	data output for 10.24 Mbit/s interface.
58	FSY	O	window signal for 10.24 Mbit/s interface.
59	T10N	O	10.24 MHz clock output.
60	n.c.		not connected.
61	SWA	I(2)	10.24 Mbit/s data input.
62	V_{SS2}	I	ground (screen).
63	SWB	I(2)	10.24 Mbit/s data input.
64	MCR	I(1)	master reset.
65	ST1	I(3)	control input for testing.
66	ST2	I(3)	control input for testing.
67	ST3	I(3)	control input for testing and mode select for 10.24 Mbit/s interface.
68	V_{DD}	I	power supply.

FUNCTIONAL DESCRIPTION

General

The SAA7500 has been designed to decode 16 stereo channel sound broadcasting signals in accordance with the German standard - **Technische Richtlinie ARD/ZDF Nr. 3R1**. The channel carrying the sound broadcast programme is selected and converted into an intermediate frequency by a frontend. The signal is then amplified and demodulated (4 PSK (Phase Shift Keying) with carrier recovery). The outputs from the demodulator are two differential coded signals that are input into the SAA7500. The SAA7500 decoder outputs the audio data, of the selected stereo or mono channel, as linear quantized 16-bit audio samples.

Selection of the desired audio channel, as well as stereo or mono mode, is controlled by inputs PA, PB, PC and PD. These inputs may be driven directly by switches or controlled by a microcomputer.

When under the control of a microcomputer, the SAA7500 transmits serial data to the microcomputer on the type of programme (16 stereo or 32 mono). The corresponding synchronization of the subframe is partly performed by the SAA7500 (every 2 ms) and at a higher level by the microcomputer (every 16 ms). The SAA7500 also sends to the microcomputer, programme information code data together with its clock and window signal.

The circuit automatically performs the system error correction and concealment. In the transmit error rate range of 0 to 3×10^{-3} a theoretical C/N (carrier-to-noise ratio) gain of about 6 dB is obtained. The residual error rate is nearly zero for transmit error rates $\leq 3 \times 10^{-4}$.

The remaining functions, such as clock recovery, main and subframe synchronization and scale factor decoding, are protected in a similar manner so that they will not influence the residual error rate.

Clock recovery

The baseband signals A' and B' are connected to the SWA and SWB inputs of the SAA7500. For clock recovery, the phase of the incoming data streams is compared with T10N (half the oscillator frequency). The output of the phase comparator (PHD) controls, by means of the loop filter, the voltage controlled oscillator (both are external to the IC) and thus its output signal T20N.

For energy dispersal, for example, in modulation pauses or with constant signals, the data streams are scrambled during generation. The exceptions are the synchronization words and the special service bits. In order that the phase correspondence between the recovered system clock (T10N) and the input signals A' and B' can be adjusted to a minimum bit error rate (BER), a programmable phase shifter is provided (inputs LZA, LZB, LZC and ST3).

The differential decoder logic delivers the original data streams which may be exchanged depending on the number of mixer stages on the transmission channel. The polarity of the two synchronization words will indicate if this is necessary, if so the two data streams will be automatically switched over.

Synchronization

Using the synchronization circuit, the incoming data streams are first searched for 11-bit Barker codewords.
The synchronization circuit permits two errors for both synchronization words, which guards against failure of the synchronization word. If the synchronization word has been detected, the following data is examined at frame length intervals to see if the synchronization word is repeated. If it is repeated, it is acknowledged as a synchronization word (window check) and an internal frame pulse generator takes over further control. There is also synchronization word failure control which initiates a renewed synchronization word search and mutes the AF output if four successive synchronization word failures occur.

To enhance the performance the result from the error correction circuit is used as an additional input to the synchronization circuit. This is to avoid extra errors through synchronization loss in the case of relative high, but for reception acceptable, bit error rates. This will not affect the rapid detection of a very high bit error rate or the non-synchronization of the data stream. The decoder will function correctly with a bit error rate up to 3×10^{-3}.

Demultiplexer

After synchronization, the beginning of a frame is marked and the digital signals are defined as to their assignment. First the non-scrambled special service bit from the half frame A is taken out. The rest of both half frames are unscrambled and demultiplexed so that each half frame is split into two substreams with a rate of 5.12 Mbit/s (see Technische Richtlinie ARD/ZDF Nr. 3R1, main frame specification). Using the inputs from the synchronization circuit and the programme selector (inputs PA, PB, PC and PD) the demultiplexer locks on to the selected programme block and generates all the control signals required for further signal processing.

Error correction

The error correction circuit provides for exact identification of two errors in a 63/44 BCH block and correction of the incorrect bits. In the event of more than two errors the identification circuit can identify incorrect BCH blocks with up to five errors.

The BCH block is operated on by a syndrome calculator, the results controls the lines of an error correction matrix. The output of this matrix corrects (inverts) the incorrect bits when data is shifted out from its buffer. The BCH block is then fed through a second syndrome calculator. In the event of more than two errors the result of the whole calculation will be other than zero. This information provides the concealment in the next stages.

The two adjacent samples related to the detected incorrect sample are added and divided by two, the result replaces the incorrect sample (interpolation). In the event of successive bad samples the last corrected sample is held until a good sample is detected (hold function). A high error frequency in the event of synchronization loss will activate the muting function and set the output data to zero.

This information, if concealment is not active, is used in the synchronization circuit as described in that section. When the samples are correct it can be assumed that the synchronization is also correct.

Scale factor, programme type evaluation and shift sunction

The transmitted samples are returned to their original range of values by the scale factor, which is obtained by decoding the ZI-subframe. The start of this frame is coupled to the start of the special services frame, synchronization for this frame uses the same principle as for the main frame. In the scale factor evaluation unit the BCH 14/6 code words (three times transmitted) are fed into a majority selection circuit working at bit level. Subsequently the error check and the correction of a maximum of two errors is carried out.

The SAA7500 contains the synchronization word detection and error check for the subframe synchronization word with its repetition time of 2 ms. The programme type evaluation with its superior synchronization has to be performed external to the chip, for example, by a microcomputer. For this purpose data is available in 8-bit blocks at a serial interface (INTR, PAUP and TUP; block rate = 4000/s). The same microcomputer can also perform the programme selection (inputs PA, PB, PC and PD).

At the input to the concealment buffer the corrected 11 bits (MSB) are combined with the 3 unprotected transmitted bits (LSB). The scale factor determines the required shift-back operations needed to convert the transmitted values back into the original values. Voids that occur are filled with noughts or ones corresponding to the sign bit. The shift-back and filling of voids ensures that no incorrect bits occur above the range defined by the scale factor. The upper 16 bits represent the regenerated audio sample.

Digital-to-analogue conversion and interfaces

The SAA7500 enables different DAC systems to be used. For control of the SAA7220P/C and TDA1541 a 2.5 external divider must be connected to the 20.48 MHz clock signal to produce the required 8.192 MHz clock signal.

A serial interface is built in with the following outputs: bit clock (AWT), word select (AWR) and audio data (AWD). In addition the mute signal (AMUN) and the concealment flag (ACM) are also available. The SAA7220P/C and TDA1541 are equipped with a digital audio interface for domestic use equivalent to 'IEC proposal No. 84 (secretariat 28; from June 1985)'.
For DACs with a parallel interface in a multiplex mode the audio data are available at the B1(MSB)-B16 outputs. The multiplexing is controlled by the L32 and R32 outputs. Using the mode outputs DWCA and DWCB the code (offset binary or two's complement) and polarity can be selected.

Additional information, including the scale factor is available through the programme information (PI) interface (PID, PITN, and PIF). Another interface, using the ASC, BSC and T10N outputs, makes available signals from the differential decoder. These signals are used for bit error measurement and an optimized phase adjustment of the internal clock (refer to 'clock recovery' section).

An optional application of the control signals for mute and concealment operations is possible using the outputs AMUN and ACM. For the mute signal a different time relationship to the unwanted pulse with very low C/N values may be obtained.

The external application of the concealment signal is recommended; if an additional interpolation is required between additional samples with different levels in the external circuitry (such as the SAA7220P/C).

Truth tables

Table 1 Delay adjustment
pins 1 to 3

LZC	LZB	LZA	DELAY
0	0	0	$4 \times \tau$
0	0	1	$3 \times \tau$
0	1	0	$2 \times \tau$
0	1	1	$1 \times \tau$
1	0	0	$0 \times \tau$
1	0	1	$-1 \times \tau$
1	1	0	$-2 \times \tau$
1	1	1	$-3 \times \tau$

$\tau \approx 1.5 \times$ gate delay time (NAND)

Table 2 Master reset
pin 64

MCR	FUNCTION
0	operation
1	master reset

Table 3 Mute
pin 16

UPMU	FUNCTION
0	no
1	yes

Table 4 Programme number
pins 12 to 15

PD	PC	PB	PA	PROGRAMME NO.
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
.	.	.	.	.
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

Table 5 Phase control signal
pin 8

PHD	PHASE
0	lead phase
1	lag phase

Table 6 Synchronization indication
pin 11

SYLN	SYNCHRONIZATION
0	yes
1	no

Table 7 Mode select for data outputs ASC and BSC for 10.24 Mbit/s interface
pin 67

ST3	DATA ASC/BSC
0	after unscrambler
1	before unscrambler

Table 8 Data converter mode select B1 (MSB) to B16
pins 22 and 23

DWCB	DWCA	DA CONVERTER MODE
0	0	compl. offset binary
0	1	offset binary
1	0	compl. 2's complement
1	1	2's complement

Table 9 Channel mode select
pins 50 and 51

M2N	M1N	CHANNEL MODE
0	0	mono (1 + 2)
0	1	mono R(2)
1	0	mono L(1)
1	1	stereo

Table 10 Concealment
pin 42

ACM	FUNCTION
0	no
1	yes

Table 11 Mute
pin 46

AMUN	MUTE
0	yes
1	no

Table 12 Interrupt
pin 47

INTR	INTERRUPT
0	no
1	yes

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage range	V_{DD}	–0.5	7.0	V
Input voltage range(1)	V_I	–0.5	V_{DD}+0.5	V
Input current	I_I	–	± 10	mA
Output current	I_O	–	± 10	mA
Supply current in V_{SS}	I_{SS}	–	28	mA
Supply current in V_{DD}	I_{DD}	–	28	mA
Total power dissipation	P_{tot}	–	500	mW
Operating ambient temperature range	T_{amb}	–25	+85	°C
Storage temperature range	T_{stg}	–55	+150	°C

Note

1. $V_{DD} + 0.5$ must not exceed 7.0 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see Handling MOS Devices).

The PLCC-68 package can only be guaranteed with soldering temperatures up to a maximum of 235 °C.

DC CHARACTERISTICS

T_{amb} = 0 °C to + 70 °C; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current	Fig.10	I_{DD}	–	12.5	–	mA
Quiescent supply current	note 1	I_{DDq}	–	–	50	μA
Inputs I(1)						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input current LOW	note 2	$-I_{IL}$	–	–	10	μA
Input current HIGH	note 2	I_{IH}	–	–	10	μA
Inputs I(2)						
Input voltage LOW		V_{IL}	–	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	–	V
Input current LOW	note 2	$-I_{IL}$	–	–	10	μA
Input current HIGH	note 2	I_{IH}	–	-	10	μA
Inputs I(3)						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Pull down resistor		R_I	25	50	100	kΩ
Outputs O						
Output voltage LOW	$-I_{OL}$ = 1 mA	V_{OL}	–	–	0.5	V
Output voltage HIGH	I_{OH} = 1 mA	V_{OH}	4.0	–	–	V

Notes to DC characteristics

1. T_{amb} = 25 °C, all inputs at V_{SS} or V_{DD}, all outputs open.
2. At 25 °C max. 1 μA.

AC CHARACTERISTICS

T_{amb} = 0 to + 70 °C; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
T20N clock pulse	Fig.3					
Pulse width HIGH		t_{WH}	15	20	–	ns
Pulse width LOW		t_{WL}	15	22	–	ns
T20N pulse period		t_{P20}	48	48.8	–	ns
Data input timing	Fig.4					
Set-up time for data SWA and SWB to T10N	note 1	t_{SWL}	–	50	–	ns
T10N pulse period T_{PSW}	note 2	t_{P10}	–	97.6	–	ns
Main frame timing	Fig.5					
Main frame sync pulse		t_{SYNC}	–	$11t_{P10}$	–	ns
Audio data timing	Fig.6					
Audio sample repetition time		t_{SAMP}	–	31.25	-	µs
Load pulse width HIGH		t_{LPH}	–	6.25	-	µs
Audio data hold		t_{ADH}	–	1	-	µs
I^2S timing	Fig.7					
Frequency AWT signal		f_{AWT}	–	1.024	–	MHz
Audio sample repetition time		t_{SAMP}	–	31.25	–	µs
PI interface timing	Fig.8					
Frequency PITN signal		f_{PITN}	–	32	–	kHz
PITN pulse period		t_{PITN}	–	31.25	–	µs
PIF pulse width HIGH		t_{PIFH}	–	$22t_{PITN}$	–	µs
PIF pulse period		t_{ZI}	–	2	–	ms
Output timing Programme type interface	Fig.9					
INTR pulse period		t_{INTR}	–	250	–	µs
INTR pulse width HIGH		t_{PINH}	–	31.25	–	µs

Notes to the characteristics

1. Due to noise, the period t_{SWL} may occasionally vary between 30 and 70 ns.
2. Due to noise, the period time t_{PSW} may occasionally vary between 77.6 and 117.6 ns.

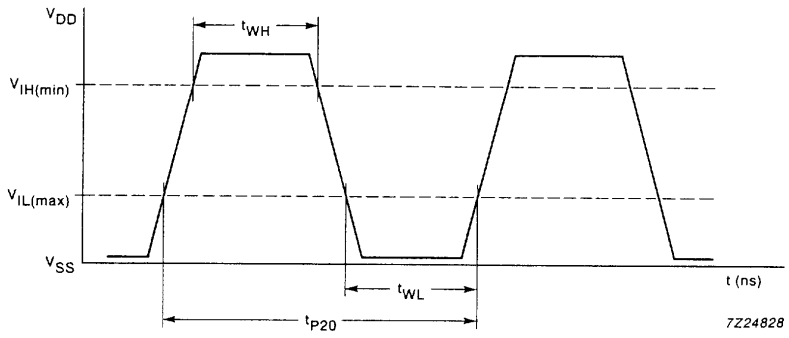


Fig.3 Waveform at clock input T20N (pin 5).

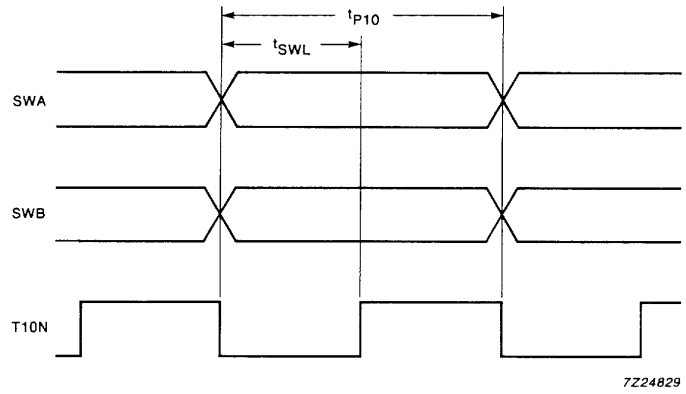


Fig.4 Data input timing (pins 59, 61 and 63).

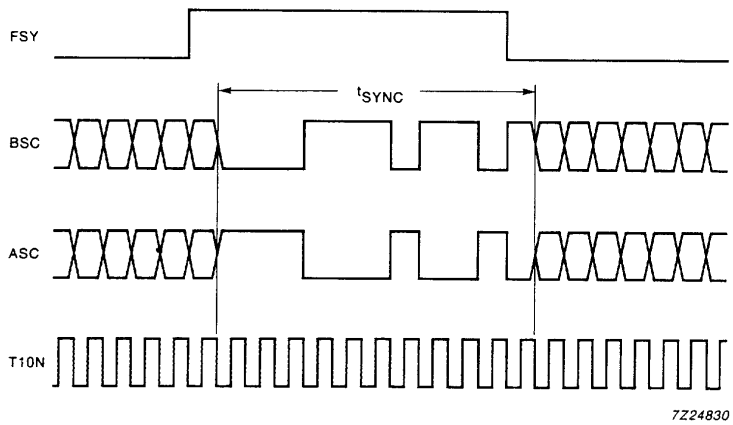


Fig.5 Output timing for 10.24 Mbit/s interface (pins 56, 57, 58 and 59).

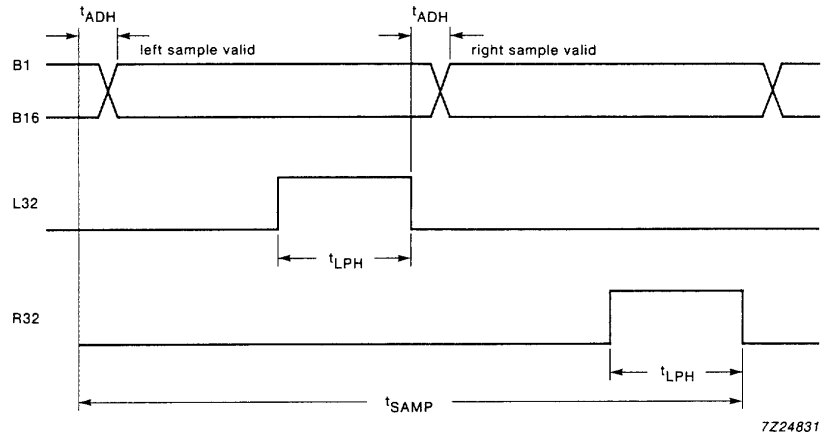


Fig.6 Audio data timing parallel out (pins 40 to 35, 33 to 24, 21 and 20).

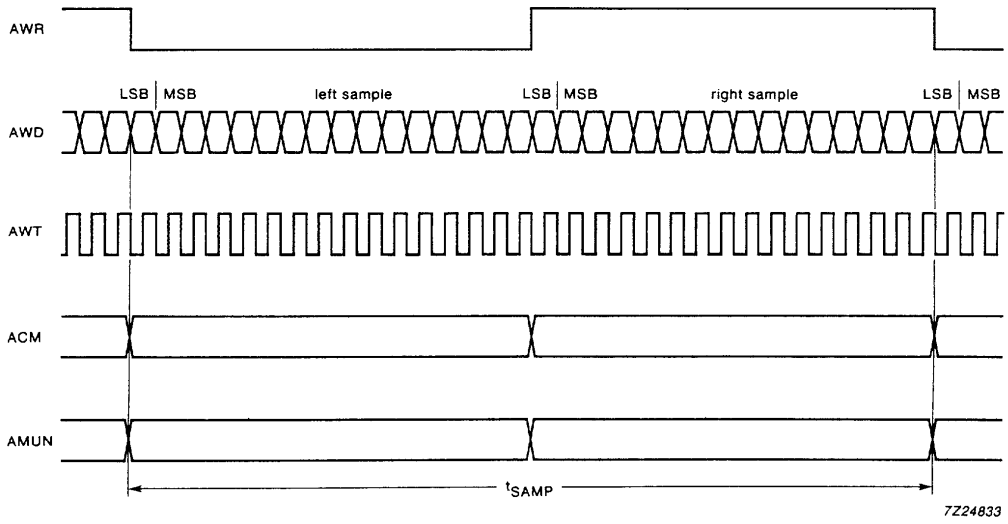


Fig.7 Inter-IC Sound (I^2S) timing and mute and interpolation flags (pins 42 to 46).

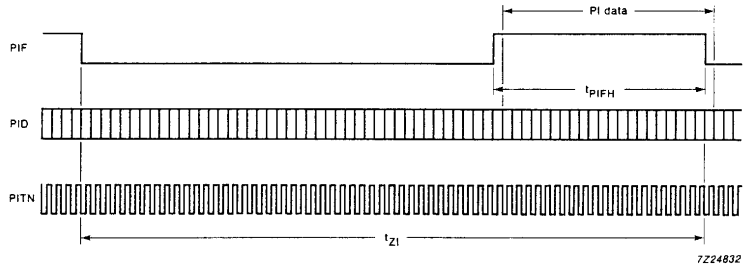
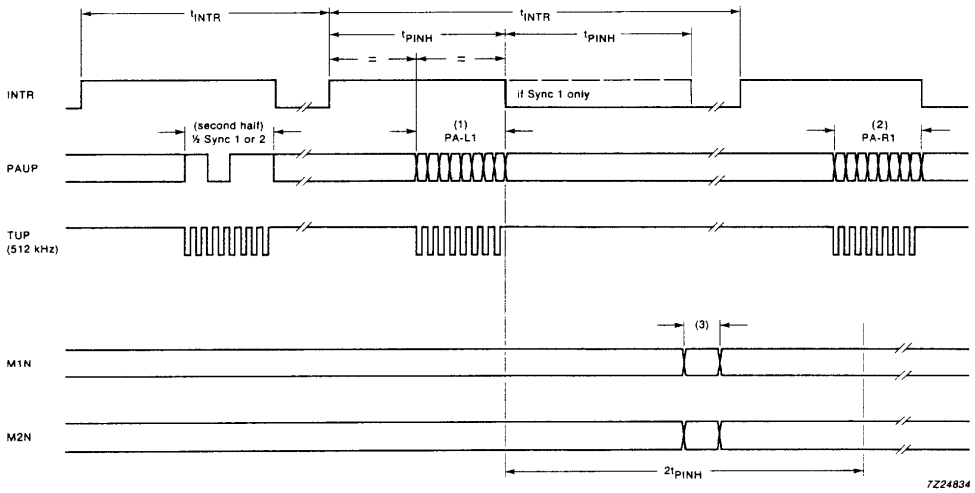


Fig.8 PI interface timing (pins 52 to 54).



(1) Programme type - left
(2) Programme type - right
(3) This time is approximately 10 μs

Fig.9 Output timing programme type interface (pins 17 to 19).

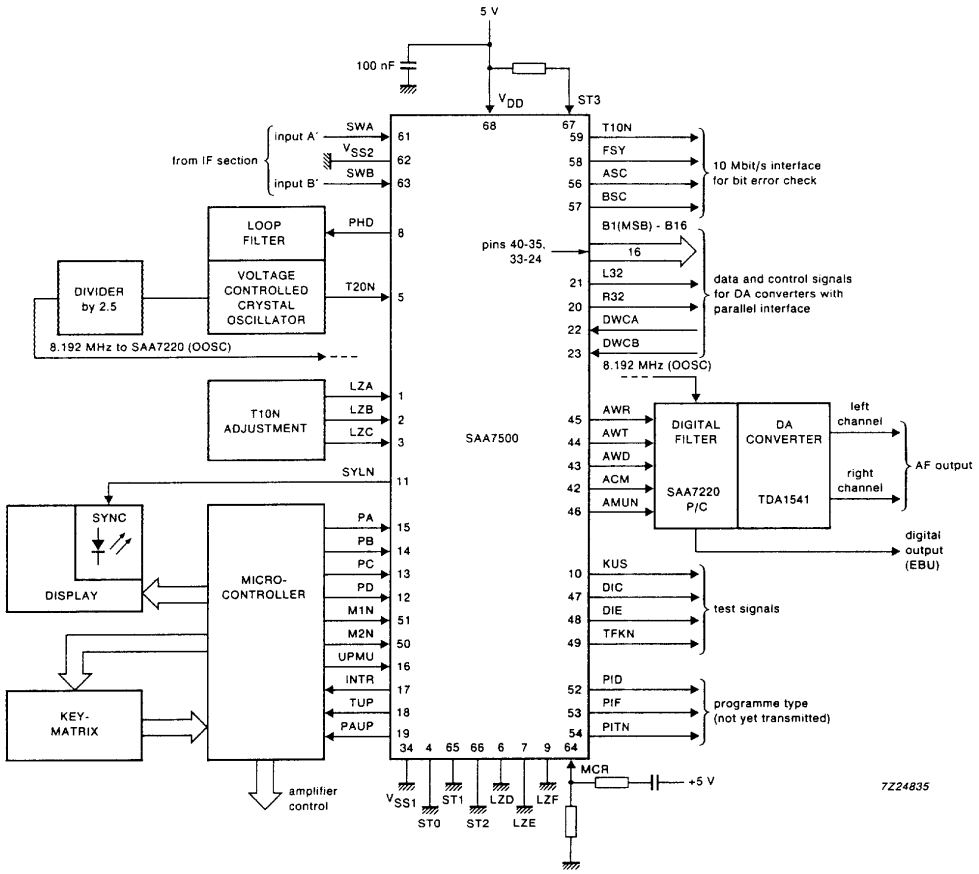
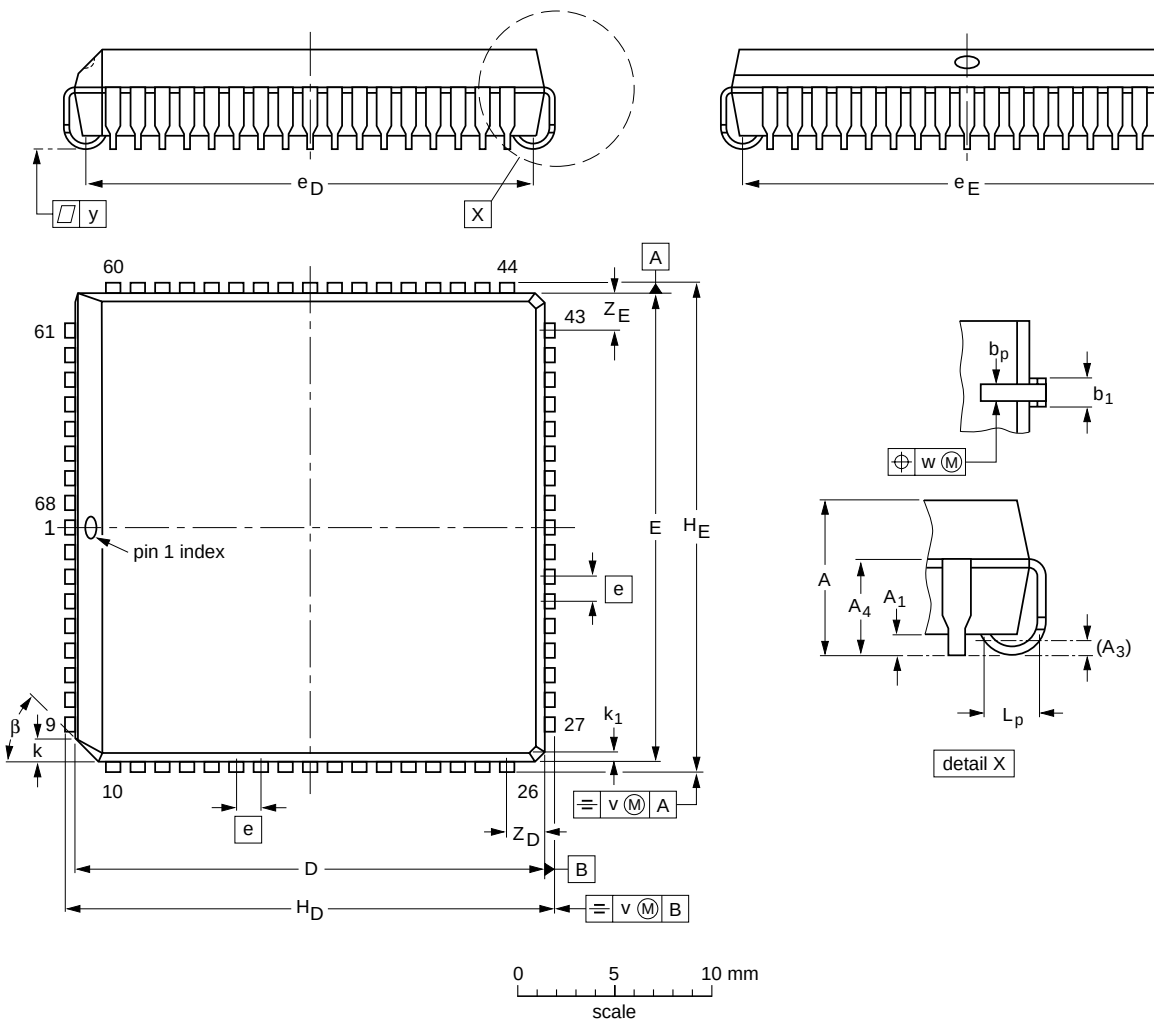


Fig.10 Application proposal.

PACKAGE OUTLINE

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.