35 MHz triple 9-bit D/A converter for high-speed video

SAA7169

Supercedes data of January 1992

FEATURES

- CMOS circuit to convert high-speed video data from digital to analog
- Three equal 9-bit digital-to-analog converters
- Input signals TTL-compatible
- Input registers for positive edge-triggered data signals
- Clock frequency for a conversion rate up to 35 MHz
- 20 MHz analog bandwidth
- 2 V (p-p) analog output voltage range without load on output (0.2 to 2.2 V DC)
- 1 V / 75 Ω outputs (0.1 to 1.1 V DC); Fig.1
- No de-glitching circuit required
- Typical 225 mW power dissipation

GENERAL DESCRIPTION

The triple high-speed D/A converter can be used in applications for

- desktop video processing
- digital television
- graphic displays
- television decoders
- general high frequency conversion

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
$I_{DD\ tot}$	total supply current	-	-	38	mA
V_I	data input levels	TTL-compatible			
f_{CLK}	conversion frequency	1	-	35	MHz
V_o	nominal output amplitude on pins 1, 3, 43 (peak-to-peak value)	-	2	-	V
B	bandwidth (–3 dB)	20	-	-	MHz
DNL	differential non-linearity	-	-	±0.5	LSB
INL	integral non-linearity	-	-	±0.2	%
α_{CR}	crosstalk attenuation	48	-	-	dB
R_o	internal serial output resistance	-	25	-	Ω
R_L	output load resistance	125	-	-	Ω
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7169	44	PLCC	plastic	SOT187

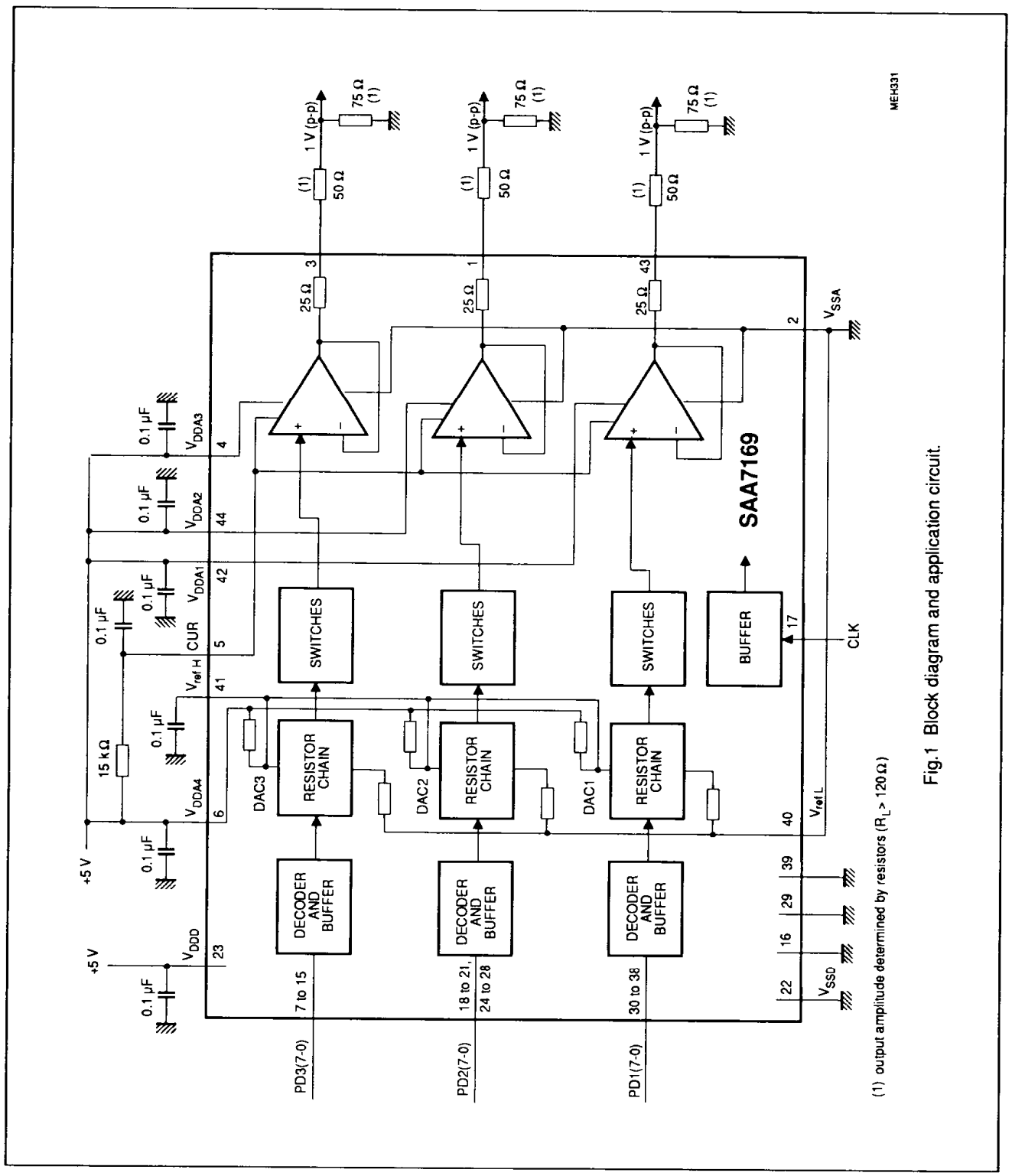

Fig.1 Block diagram and application circuit.

(1) output amplitude determined by resistors (R_L > 120 Ω)

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{o\,2}$	1	analog output voltage of channel 2
V_{SSA}	2	analog ground (0 V)
$V_{o\,3}$	3	analog output voltage of channel 3
V_{DDA3}	4	+5 V supply voltage for buffer amplifier of channel 3
CUR	5	current input for analog output buffers, decoupled to V_{SSA}
V_{DDA4}	6	+5 V supply voltage for analog reference part
PD3(8)	7	9-bit data input of channel 3
PD3(7)	8	
PD3(6)	9	
PD3(5)	10	
PD3(4)	11	
PD3(3)	12	
PD3(2)	13	
PD3(1)	14	
PD3(0)	15	
i.c.	16	connect to digital ground (input not used)
CLK	17	clock frequency input
PD2(8)	18	9-bit data input of channel 2 (bits PD2(8-5))
PD2(7)	19	
PD2(6)	20	
PD2(5)	21	
V_{SSD}	22	digital ground (0 V)
V_{DDD}	23	+5 V supply voltage for digital part
PD2(4)	24	9-bit data input of channel 2 (bits PD2(4-0))
PD2(3)	25	
PD2(2)	26	
PD2(1)	27	
PD2(0)	28	
i.c.	29	connect to digital ground (input not used)
PD1(8)	30	9-bit data input of channel 1 (bits PD1(8-4))
PD1(7)	31	
PD1(6)	32	
PD1(5)	33	
PD1(4)	34	

SYMBOL	PIN	DESCRIPTION
PD1(3)	35	9-bit data input of channel 1 (bits PD1(3-0))
PD1(2)	36	
PD1(1)	37	
PD1(0)	38	
i.c.	39	connect to digital ground (input not used)
$V_{ref\ L}$	40	reference voltage LOW; analog ground (V_{SSA})
$V_{ref\ H}$	41	internal generated reference voltage HIGH, decoupled to V_{SSA}
V_{DDA1}	42	+5 V supply voltage for buffer amplifier of channel 1
$V_{o\ 1}$	43	analog output voltage of channel 1
V_{DDA2}	44	+5 V supply voltage for buffer amplifier of channel 2

PIN CONFIGURATION

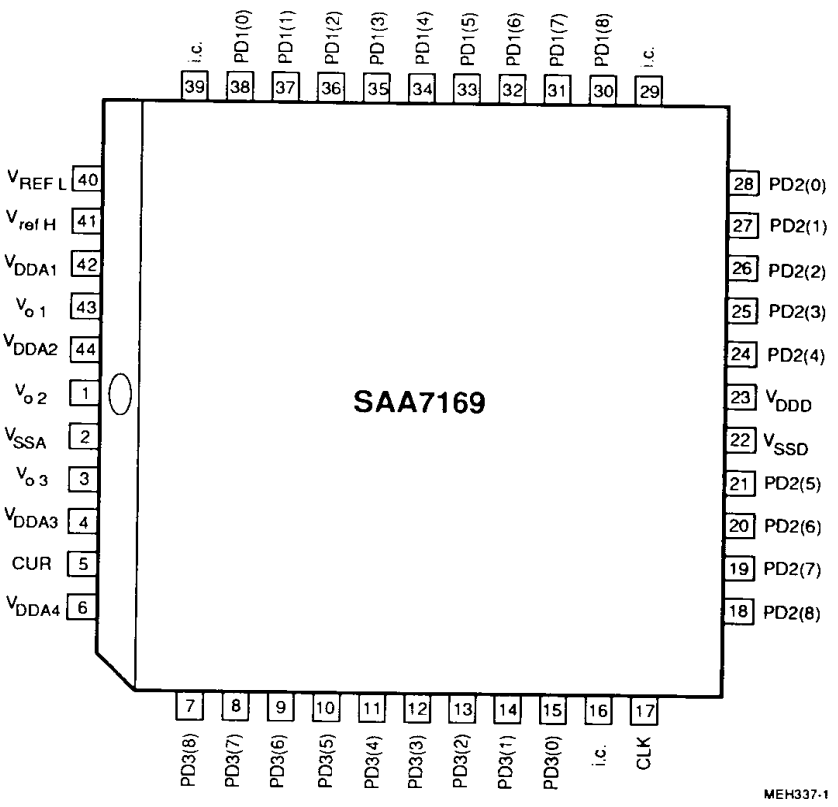

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The integrated monolithic CMOS circuit SAA7169 is a triple 9-bit digital-to-analog converter for high-speed video applications. Its three channels are equal. The maximum conversion rate is 35 MHz.

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Fig.1 shows the application for 1 V/ 75 Ω outputs, using the serial 25 Ω + 50 Ω resistors.

Each digital-to-analog converter has its own supply pin for purpose of decoupling. V_{DDA4} is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage influences directly the output amplitudes.
The current CUR into pin 5 is 0.3 mA (V_{DDA4} = 5 V, R_{5-6} = 15 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pin 23)	−0.3	7	V
V_{DDA1}	analog supply voltage range (pin 42)	−0.3	7	V
V_{DDA2}	analog supply voltage range (pin 44)	−0.3	7	V
V_{DDA3}	analog supply voltage range (pin 4)	−0.3	7	V
V_{DDA4}	analog supply voltage range (pin 6)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA(1\ to\ 4)}$	-	±100	mV
V_n	voltage on all input pins 7 to 15, 18 to 21 and 24 to 40	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{amb}	operating ambient temperature range	0	70	°C
T_{stg}	storage temperature range	−65	150	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; CLK = 35 MHz; f_{DATA} = 17.5 MHz (squarewave, full scale); T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage range (pin 23)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 42)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 44)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 4)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 6)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current	for digital part; note 1	-	-	20	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	without load on outputs	-	-	18	mA
9-bit data inputs (pins 7 to 15; 18 to 21, 24 to 28 and 30 to 38)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance		-	-	10	pF
I_{leak}	input leakage current		-	-	10	µA
t_{SU}	data set-up time	Fig.3	11	-	-	ns
t_{HD}	data hold time		3	-	-	ns
CLK input (pin 17)		Fig.3				
f_{CLK}	frequency range		1	-	35	MHz
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance		-	-	10	pF
I_{leak}	input leakage current		-	-	10	µA
t_{CLK}	cycle time		28.5	-	-	ns
t_{pH}	duty factor	$t_{CLK\,H}$ / t_{CLK}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Digital-to-analog converters (pins 5, 6 and 40)						
V_{DDA4}	reference input voltage for internal resistor chains (pin 6)		4.75	5	5.25	V
I_{CUR}	input current (pin 5)	R_{6-5} = 15 kΩ	-	-	400	µA
Analog outputs V_{o1}; V_{o2} and V_{o3} (pins 43, 1 and 3)						
V_o	nominal output signal (peak-to-peak value)	without load	-	2	-	V
$V_{43, 1, 3}$	minimum output voltage	without load; V_{DDA4} = 5 V	0.16	-	0.24	V
	maximum output voltage	without load; V_{DDA4} = 5 V	2.1	-	2.3	V
DTDM	DAC to DAC matching	between all channels	-	-	|30|	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	output signal bandwidth	-3 dB	20	-	-	MHz
α_{CR}	crosstalk attenuation	note 2	48	-	-	dB
DNL	differential non-linearity	9-bit data; R_L = 125 Ω	-	-	±0.5	LSB
INL	integral non-linearity	9-bit data; R_L = 125 Ω	-	-	±0.2	%
$R_{43, 1, 3}$	internal serial output resistor		-	25	-	Ω
$R_{L\ 43, 1, 3}$	load resistance on output		125	-	-	Ω

Notes to the characteristics

1. With f_{CLK} = 35 MHz; f_{DATA} = 17.5 MHz (squarewave, full scale)
2. Crosstalk from channel to channel. One DAC with digital 5 MHz (sinusoidal, full scale) input signal, the other input data LOW. Measurements taken on outputs with 5.46 MHz filters (–3 dB at 5.87 MHz and –45 dB at 7.24 MHz).

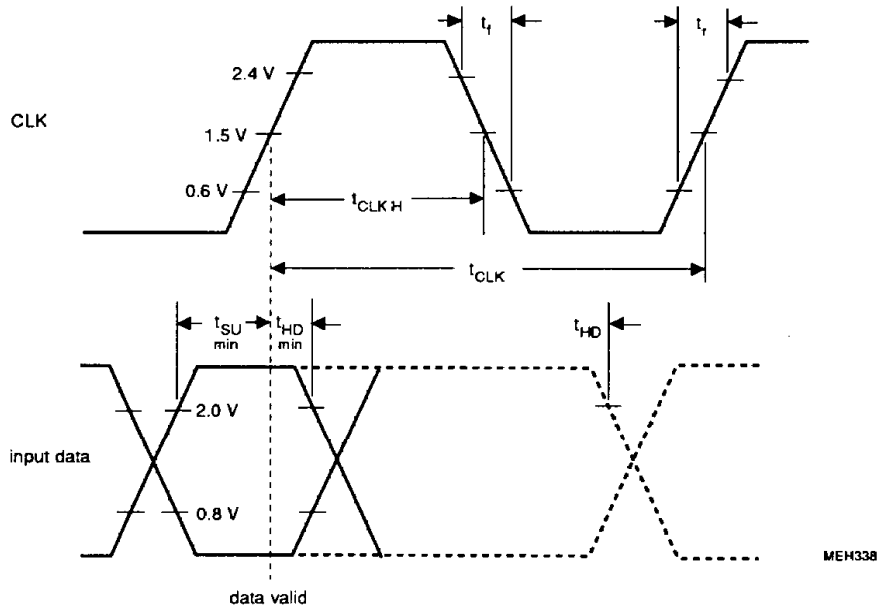

Fig.3 Input data timing.