SUN MICROELECTRONICS

July 1997

SEC

DATA SHEET

SBus-to-EBus Controller

DESCRIPTION

The STP2014 SBus-to-EBus Controller (SEC) is an interface between the SBus and the EBus that is used for slow I/O devices such as TOD, EPROM, serial port, and keyboard/mouse. The STP2014 also houses the interrupt control and steering logic, the timer/counter registers, reset logic, and miscellaneous registers. The STP2014 is physically located on the SBus. However, the STP2104 does not follow the SBus protocol completely. For instance, in order to save pins on chip, address and data are multiplexed. Therefore, all references to the SBus in this document really refer to the pseudo SBus implementation.

FEATURES

- Supports byte, halfword, word, and doubleword transfers
- Built in scan capability
- Supports early write acknowledge
- 160-pin PQFP package

BLOCK, LOGIC, AND TYPICAL APPLICATION DIAGRAMS

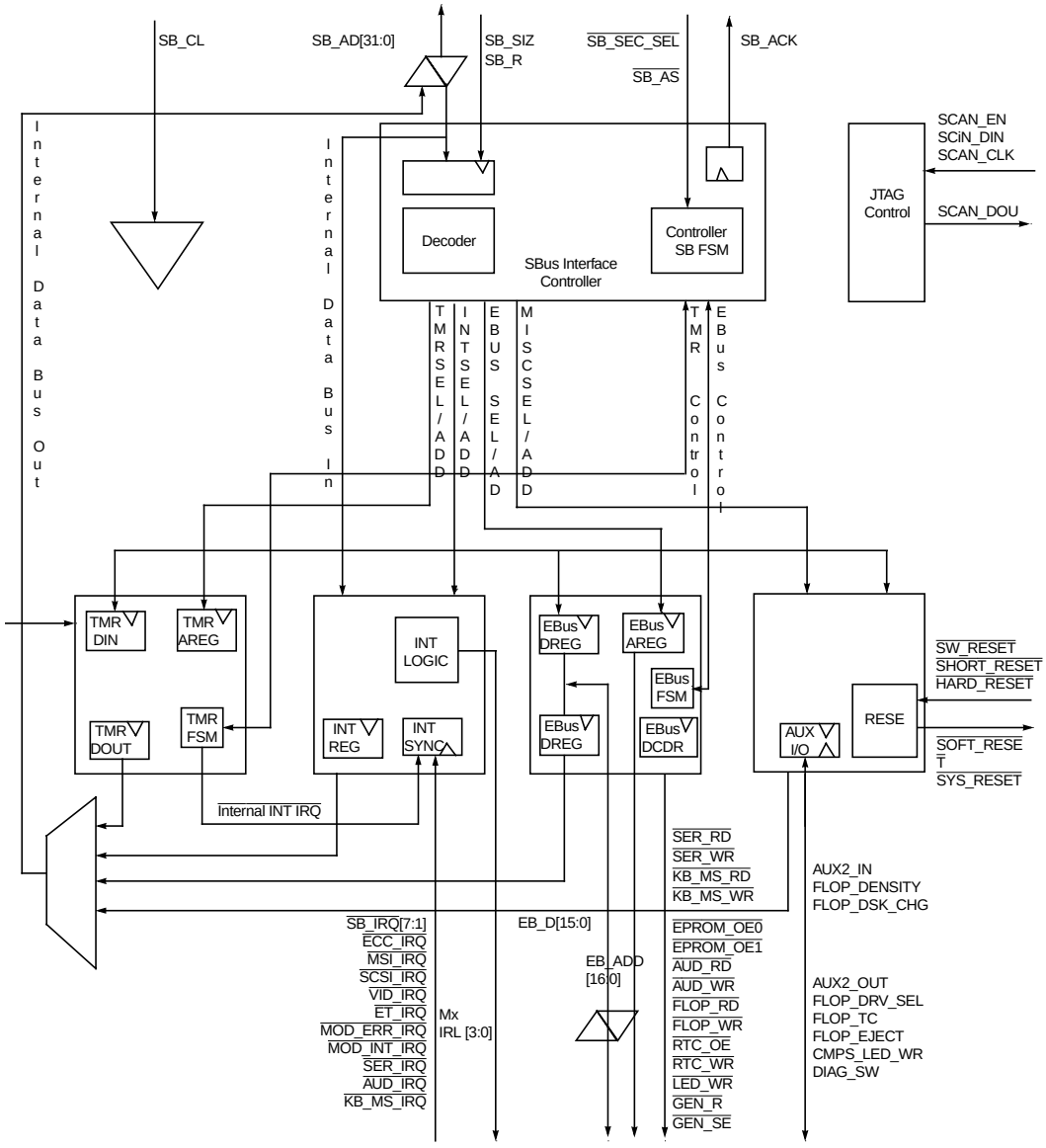


Figure 1. STP2014 Block Diagram

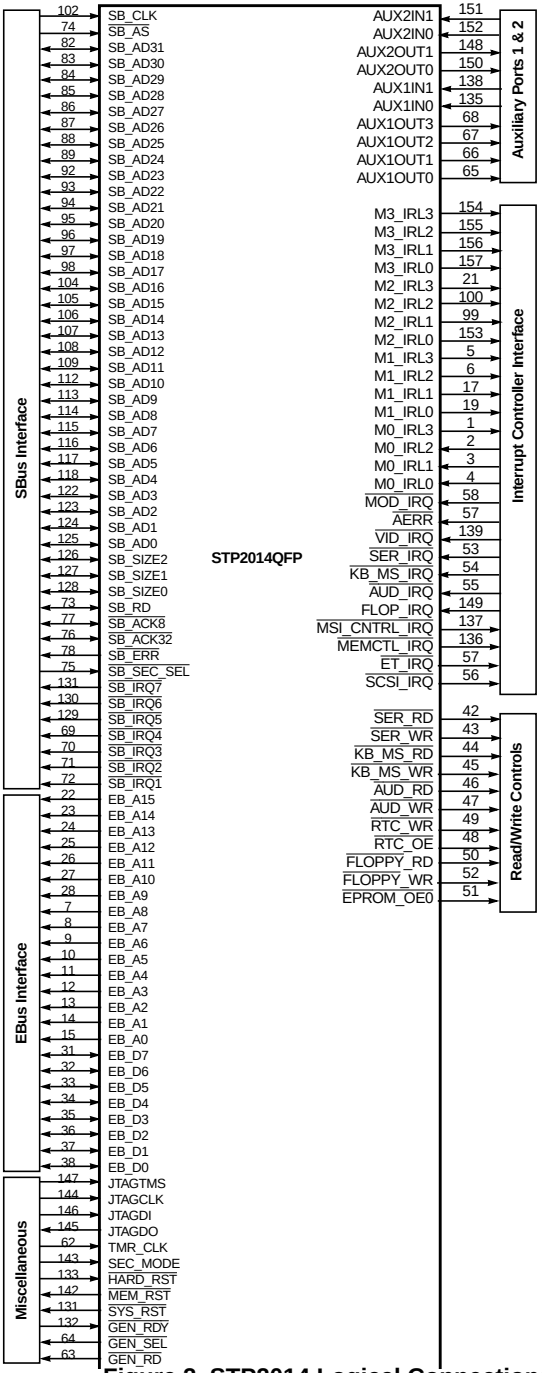


Figure 2. STP2014 Logical Connections

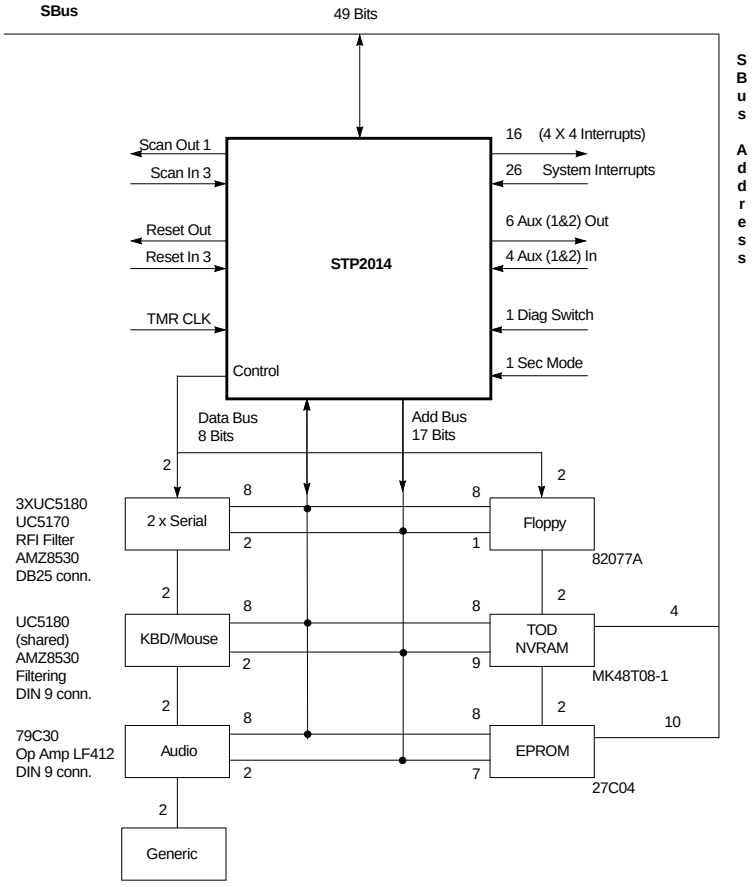


Figure 3. STP2014 Typical Application

SIGNAL DESCRIPTIONS

SBus Interface

Signal	Type	Description
SB_CLK	Input	SBus clock
$\overline{\text{SB\_AS}}$	Input	SBus address strobe
SB_AD[31:0]	Input/Output	SBus data bus
SB_SIZE[2:0]	Input/Output	SBus size
$\overline{\text{SB\_RD}}$	Input/Output	SBus read
$\overline{\text{SB\_ACK}}$[8, 32]	Input/Output	SBus acknowledge
$\overline{\text{SB\_ERR}}$	Output	SBus error
$\overline{\text{SB\_SEC\_SEL}}$	Input	SBus slave select
$\overline{\text{SB\_IRQ}}$[7:1]	Output	SBus interrupt request

External Bus Interface

Signal	Type	Description
EB_A[15:0]	Output	External bus address
EB_D[7:0]	Input/Output	External bus data

Auxiliary Ports 1 and 2

Signal	Type	Description
AUX2IN[1:0]	Input	Auxiliary register 2 input
AUX2OUT[1:0]	Output	Auxiliary register 2 output
AUX1IN[1:0]	Input	Auxiliary register 1 input
AUX1OUT[3:0]	Output	Auxiliary register 1 output

Interrupt Controller Interface

Signal	Type	Description
M3_IRL[3:0]	Output	Processor 3 interrupt lines
M2_IRL[3:0]	Output	Processor 2 interrupt lines
M1_IRL[3:0]	Output	Processor 1 interrupt lines
M0_IRL[3:0]	Output	Processor 0 interrupt lines
$\overline{\text{MOD\_IRQ}}$	Input	Module interrupt request
$\overline{\text{AERR}}$	Input	Asynchronous error
$\overline{\text{VID\_IRQ}}$	Input	Video interrupt request
$\overline{\text{SER\_IRQ}}$	Input	Serial interrupt request
$\overline{\text{KB\_MS\_IRQ}}$	Input	Keyboard/mouse interrupt request
$\overline{\text{AUD\_IRQ}}$	Input	Audio interrupt request
$\overline{\text{FLOP\_IRQ}}$	Input	Floppy interrupt request
$\overline{\text{MSI\_CNTRL\_IRQ}}$	Input	Mbus/SBus controller interrupt request
$\overline{\text{MEMCTL\_IRQ}}$	Input	Memory controller interrupt request
$\overline{\text{ET\_IRQ}}$	Input	Ethernet interrupt request
$\overline{\text{SCSI\_IRQ}}$	Input	SCSI interrupt request

Read/Write Controls

Signal	Type	Description
$\overline{\text{SER\_RD}}$	Output	Serial port read
$\overline{\text{SER\_WR}}$	Output	Serial port write
$\overline{\text{KB\_MS\_RD}}$	Output	Keyboard/mouse read
$\overline{\text{KB\_MS\_WR}}$	Output	Keyboard/mouse write
$\overline{\text{AUD\_RD}}$	Output	Audio read
$\overline{\text{AUD\_WR}}$	Output	Audio write
$\overline{\text{RTC\_WR}}$	Output	TOD write
$\overline{\text{RTC\_OE}}$	Output	TOD output enable
$\overline{\text{FLOPPY\_RD}}$	Output	Floppy read
$\overline{\text{FLOPPY\_WR}}$	Output	Floppy write
$\overline{\text{EPROM\_OE0}}$	Output	EPROM output enable

Miscellaneous

Signal	Type	Description
JTAGTMS	Input	JTAG mode select
JTAGCLK	Input	JTAG clock
JTAGDI	Input	JTAG data input
JTAGDO	Output	JTAG data output
TMR_CLK	Input	Counter timer clock
SEC_MODE	Input	Mode: 0 = Reserved, 1 = System
$\overline{\text{HARD\_RST}}$	Input	System reset input
$\overline{\text{MEM\_RST}}$	Output	Memory reset output
$\overline{\text{SYS\_RST}}$	Output	System reset output
$\overline{\text{GEN\_RDY}}$	Input	Generic port ready
$\overline{\text{GEN\_SEL}}$	Output	Generic port write
$\overline{\text{GEN\_RD}}$	Output	Generic port read

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply voltage	–0.5	7.0	V
V_{IN}	Input voltage	–0.5[1]	7.0	V
T_{ST}	Storage termperature	–65	150	C
T_{CASE}	Operating temperature	0	85	C

1. V_{IN} MIN = –3.0 V for pulse width less than 15 ns.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	DC supply	4.75	5.25	V
T_A	Ambient temperature	0	70	C

Capacitance

Symbol	Parameter	Min	Max	Units
	Pin loading capacitance	20	45	pF

DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	Voltage input low		–	0.8	V
V_{IH}	Voltage input high		2.0	–	V
V_{OL}	Voltage output low	I_{OL} = 1.0 mA I_{OL} = 2.0 mA I_{OL} = 4.0 mA I_{OL} = 6.0 mA I_{OL} = 8.0 mA	–	0.4	V
V_{OH}	Voltage output high	I_{OH} = -1.0 mA I_{OH} = -2.0 mA I_{OH} = -4.0 mA I_{OH} = -6.0 mA I_{OH} = -8.0 mA	2.4	–	V
I_{IL}	Input leakage current low T_{TL} input, without pullup T_{TL} input, with pullup Bidirect 1 mA, with pullup Bidirect 2 mA, hold amp Bidirect 4 mA Bidirect 6 mA, hold amp	 V_{IN} = 0.0 V, V_{DD} V_{IN} = 0 V V_{IN} = 0.0 V V_{IN} = 0.40 V V_{IN} = 0.0 V V_{IN} = 0.40 V	 –10 –175 –290 45 –10 45	 – – –45 160 – 160	A
I_{IH}	Input leakage current high TTL input, without pullup TTL input, with pullup Bidirect 1 mA, with pullup Bidirect 2 mA, holding amp Bidirect 4 mA Bidirect 6 mA, holding amp	 V_{IN} = V_{DD} V_{IN} = 3.5 V V_{IN} = V_{DD} V_{IN} = 2.40 V V_{IN} = V_{DD} V_{IN} = 2.40 V	 – – NA –175 NA –175	 10 –2.00 40 –715 10 –715	A
I_{OZ}	3-state output leakage current, w/ pullup	V_O = GND, V_O = V_{CC}	–10	10	A
I_{OSN}	3-state bidirect or output buffer 1 mA drive 2 mA drive 4 mA drive 6 mA drive 8 mA drive	 V_{OUT} = V_{DD} 	 7.50 15.00 30.00 45.00 60.00	 35.00 70.00 140.00 210.00 280.00	 mA
I_{OSP}	3-state bidirect or output buffer 1 mA drive 2 mA drive 4 mA drive 6 mA drive 8 mA drive	 V_{OUT} = 0 V 	 –6.25 –12.50 –25.00 –37.50 –50.00	 –35.00 –70.00 –140.00 –210.00 –280.00	 mA
I_{CC}	Dynamic supply current			160	mA
I_{CC}	Quiescent current	V_{IN} = V_{CC} or GND, V_{CC} = Max		2.0	mA

AC Characteristics: SBus Interface Signals

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{si}	$\overline{SB\_AS}$	SB_CLK	Min		15	120
T_{hi}	SB_SIZ[2:0]	SB_CLK	Min		0	60
	SB_RD	SB_CLK				
T_{si}	$\overline{SB\_SEC\_SEL}$	SB_CLK	Min		15	
T_{hi}		SB_CLK	Min		0	
T_{si}	SB_D[31:0]	SB_CLK	Min		15	120
T_{hi}		SB_CLK	Min		0	60
T_{do}		SB_CLK	Max		30	120
T_{ho}		SB_CLK	Min		0	60
T_{do}	$\overline{SB\_ACK32}$	SB_CLK	Max		30	120
T_{ho}	$\overline{SB\_ACK8}$	SB_CLK	Min		0	60
	$\overline{SB\_ERR}$					
T_{si}	$\overline{SB\_RESET}$	SB_CLK	Min		15	120
T_{hi}	Applicable only for deassertion	SB_CLK	Min		0	6
	$\overline{SB\_IRQ}$[7:1]	ASYNC				

AC Characteristics: EBus Interface Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	EB_A[16:0]	SB_CLK	Max		25	125.5
T_{ho}		SB_CLK	Min		0	
T_{do}	EB_D[15:0]	SB_CLK	Max		25	158.5
T_{ho}		SB_CLK	Min		0	
T_{si}		SB_CLK	Min		10	
T_{hi}		SB_CLK	Min		0	

1. 37.5 pF trace load

AC Characteristics: Serial Port Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	$\overline{SER\_RD}$	SB_CLK	Max		25	47.5
T_{ho}	$\overline{SER\_WR}$	SB_CLK	Min		0	
	$\overline{SER\_IRQ}$	ASYNC				

1. 37.5 pF trace load

AC Characteristics: Keyboard/Mouse Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	$\overline{KB\_MS\_RD}$	SB_CLK	Max		25	47.5
T_{ho}	$\overline{KB\_MS\_WR}$	SB_CLK	Min		0	
	$\overline{KB\_MS\_IRQ}$	ASYNC				

1. 37.5 pF trace load assumed

AC Characteristics: EPROM Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	$\overline{EPROM\_OE0}$	SB_CLK	Max		25	77.5
T_{ho}	$\overline{EPROM\_OE1}$	SB_CLK	Min		0	

1. 37.5 pF trace load assumed

AC Characteristics: Audio Port Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	$\overline{AUD\_WR}$	SB_CLK	Max		25	47.5
T_{ho}	$\overline{AUD\_RD}$	SB_CLK	Min		0	
	$\overline{AUD\_IRQ}$	ASYNC				

1. 37.5 pF trace load assumed

AC Characteristics: Floppy Port Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	$\overline{\text{FLOP\_RD}}$	SB_CLK	Max		25	47.5
T_{ho}	$\overline{\text{FLOP\_WR}}$	SB_CLK	Min		0	
	$\overline{\text{FLOP\_IRQ}}$	ASYNC				

1. 37.5 pF trace load assumed

AC Characteristics: AUX 1 and 2 I/O Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
	FLOP_DENSITY FLOP_DSK_CHG AUX2_OUT	ASYNC				
T_{do}	FLOP_DRV_SEL	SB_CLK	Max		25	47.5
T_{ho}	FLOP_TC FLOP_EJECT LED_WR AUX2_OUT	SB_CLK	Min		0	

1. 37.5 pF trace load assumed

AC Characteristics: TOD Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	$\overline{\text{RTC\_OE}}$	SB_CLK	Max		25	44.5
T_{ho}	$\overline{\text{RTC\_WR}}$	SB_CLK	Min		0	

1. 37.5 pF trace load assumed

AC Characteristics: LED Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	$\overline{\text{LED\_WR}}$	SB_CLK	Max		25	47.5
T_{ho}		SB_CLK	Min		0	

1. 37.5 pF trace load assumed

AC Characteristics: Generic Port Signals [1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	$\overline{GEN\_RD}$	SB_CLK	Max		25	–47.5
T_{ho}	$\overline{GEN\_SEL}$	SB_CLK	Min		0	
	$\overline{GEN\_RDY}$	ASYNC				

1. 37.5 pF trace load assumed

AC Characteristics: Interrupt Signals (not previously listed)

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
	$\overline{VME\_IRQ}$[7:1] $\overline{MSI\_CTRL\_IRQ}$ $\overline{ECC\_IRQ}$ $\overline{SCSI\_IRQ}$[1:0] $\overline{ET\_IRQ}$ $\overline{MOD\_INT\_IRQ}$ $\overline{MOD\_ERR\_IRQ}$ $\overline{VID\_IRQ}$	ASYNC				
T_{do} T_{ho}	M0_IRL[3:0] M1_IRL[3:0] M2_IRL[3:0] M3_IRL[3:0]	SB_CLK SB_CLK	Max Min		30 0	20

TIMING DIAGRAMS

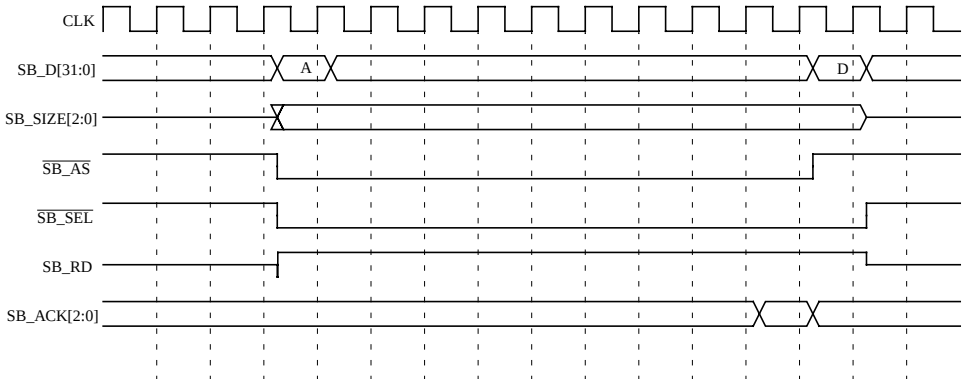


Figure 4. EPROM Byte Read

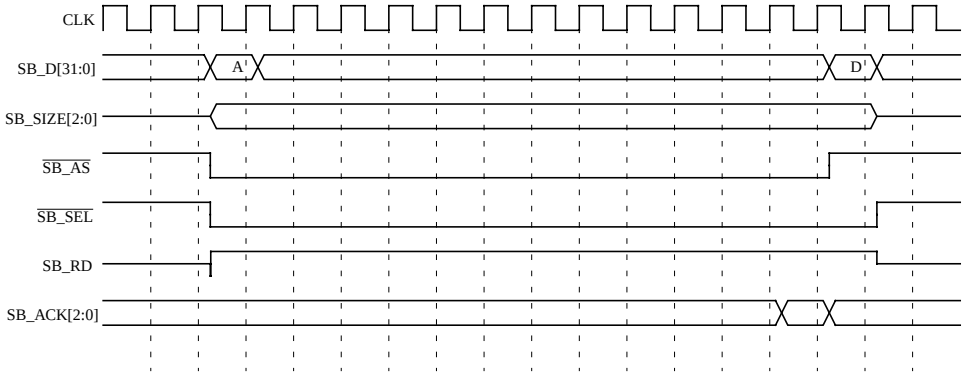


Figure 5. EPROM Word Read

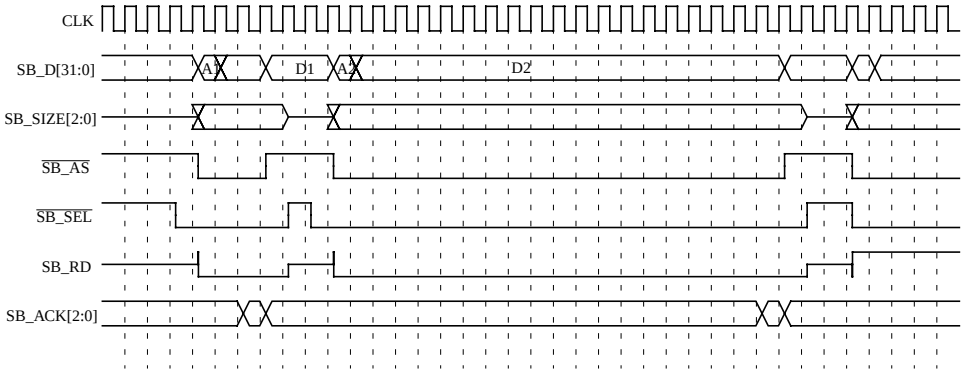


Figure 6. Serial Port (Keyboard) Back-to-Back Write

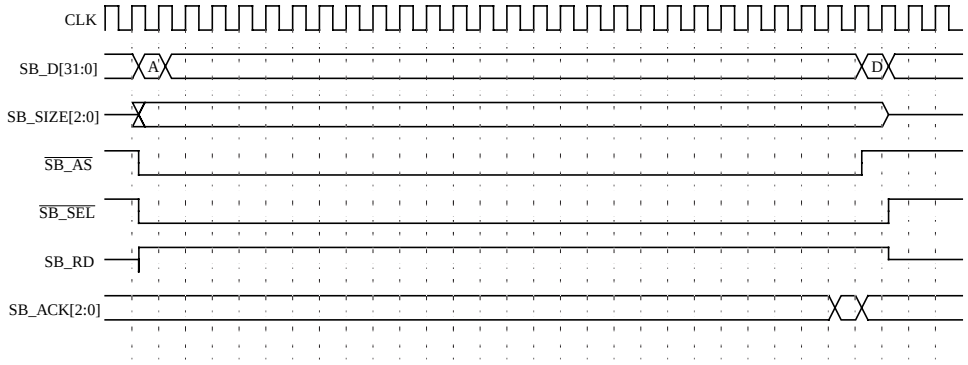


Figure 7. Serial Port (Keyboard) Read After Write (Write Not Shown)

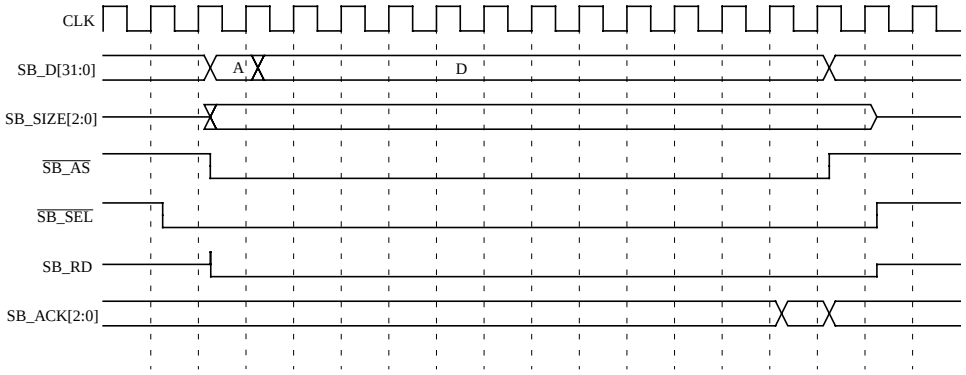


Figure 8. RTC (NVRAM, TOD) Write

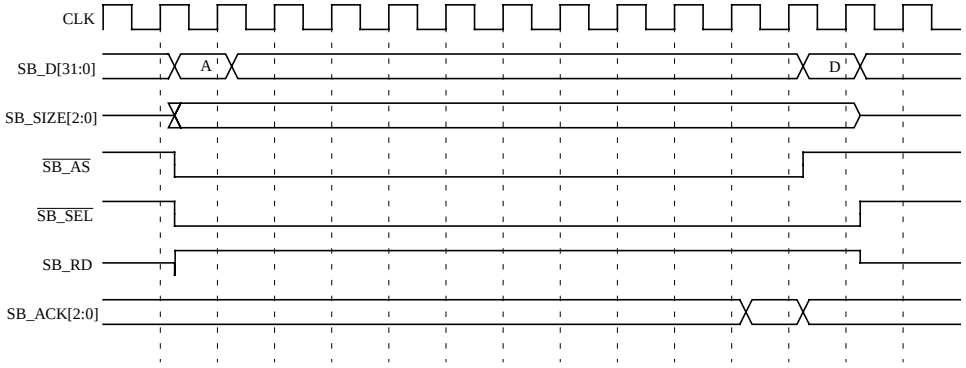


Figure 9. NTC (NVRAM, TOD) Read

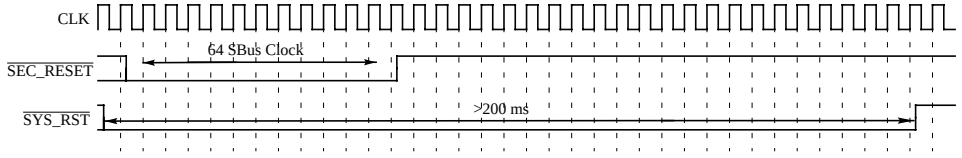


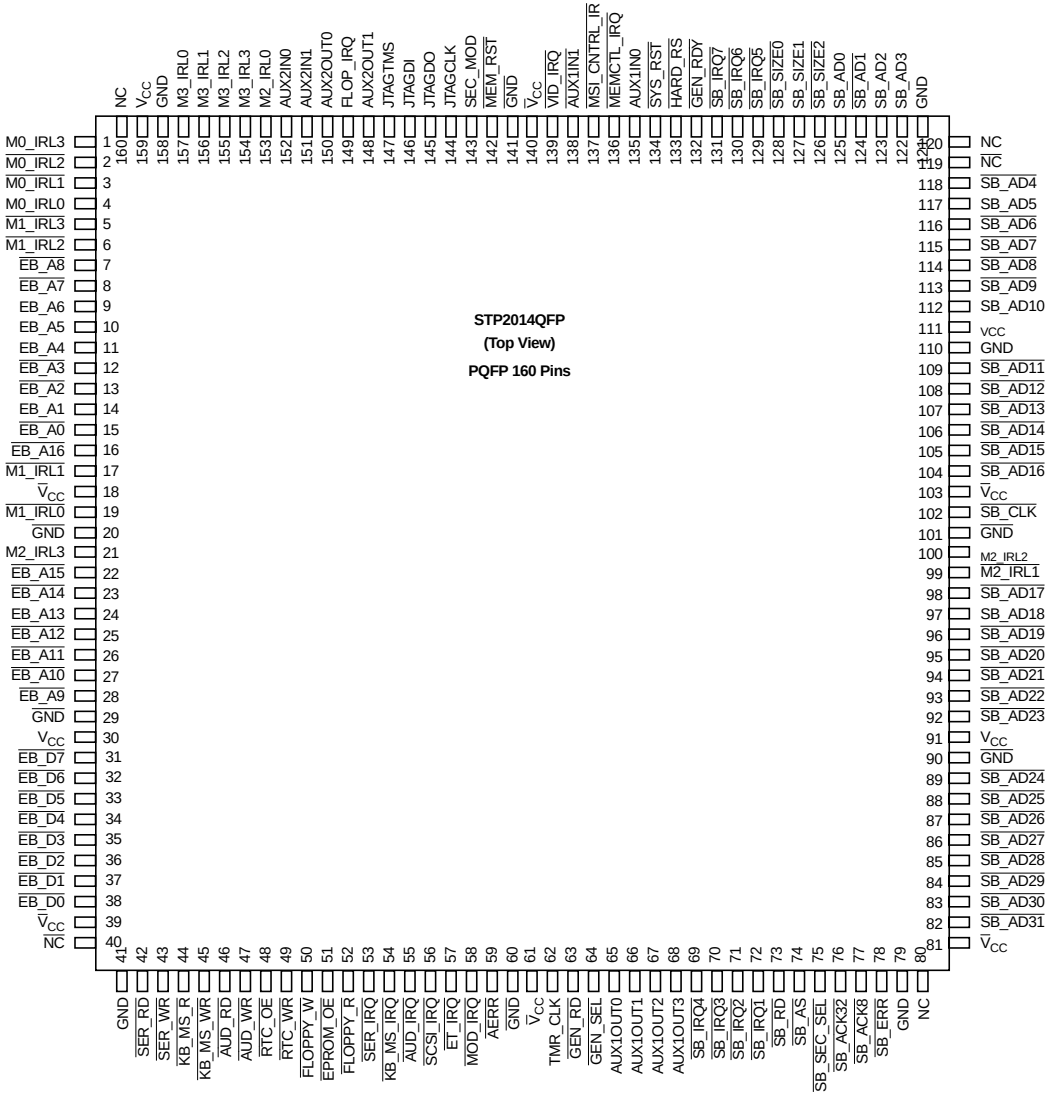
Figure 10. Hard Reset (Not Drawn to Scale)

PACKAGE INFORMATION

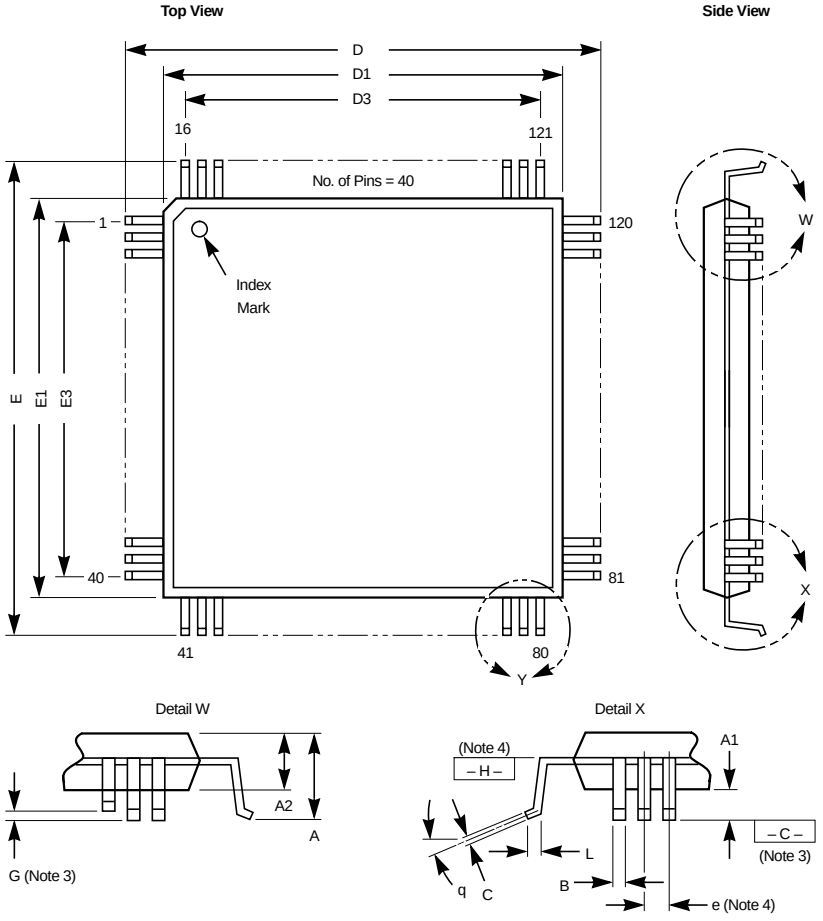
160-Pin PQFP Pin Assignments

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	M0_IRL3	33	$\overline{EB\_D5}$	65	AUX1OUT0	97	SB_AD18	129	$\overline{SB\_IRQ5}$
2	M0_IRL2	34	$\overline{EB\_D4}$	66	AUX1OUT1	98	SB_AD17	130	$\overline{SB\_IRQ6}$
3	M0_IRL1	35	$\overline{EB\_D3}$	67	AUX1OUT2	99	M2_IRL1	131	$\overline{SB\_IRQ7}$
4	M0_IRL0	36	$\overline{EB\_D2}$	68	AUX1OUT3	100	M2_IRL2	132	$\overline{GEN\_RDY}$
5	M1_IRL3	37	EB_D1	69	$\overline{SB\_IRQ4}$	101	GND	133	$\overline{HARD\_RST}$
6	M1_IRL2	38	$\overline{EB\_D0}$	70	$\overline{SB\_IRQ3}$	102	SB_CLK	134	$\overline{SYS\_RST}$
7	EB_A8	39	V_{CC}	71	$\overline{SB\_IRQ2}$	103	V_{CC}	135	AUX1IN0
8	EB_A7	40	N/C	72	$\overline{SB\_IRQ1}$	104	SB_AD16	136	$\overline{MEMCTL\_IRQ}$
9	EB_A6	41	GND	73	SB_RD	105	SB_AD15	137	$\overline{MSI\_CNTRL\_IRQ}$
10	EB_A5	42	$\overline{SER\_RD}$	74	$\overline{SB\_AS}$	106	SB_AD14	138	$\overline{AUX1IN1}$
11	EB_A4	43	$\overline{SER\_WR}$	75	$\overline{SB\_SEC\_SEL}$	107	SB_AD13	139	$\overline{VID\_IRQ}$
12	EB_A3	44	$\overline{KB\_MS\_RD}$	76	$\overline{SB\_ACK32}$	108	SB_AD12	140	V_{CC}
13	EB_A2	45	$\overline{KB\_MS\_WR}$	77	$\overline{SB\_ACK8}$	109	$\overline{SB\_AD11}$	141	GND
14	EB_A1	46	$\overline{AUD\_RD}$	78	$\overline{SB\_ERR}$	110	GND	142	$\overline{MEM\_RST}$
15	$\overline{EB\_A0}$	47	$\overline{AUD\_WR}$	79	GND	111	V_{CC}	143	SEC_MODE
16	EB_A16	48	$\overline{RTC\_OE}$	80	N/C	112	SB_AD10	144	JTAGCLK
17	$\overline{M1\_IRL1}$	49	$\overline{RTC\_WR}$	81	V_{CC}	113	SB_AD9	145	JTAGDO
18	$\overline{V_{CC}}$	50	$\overline{FLOPPY\_WR}$	82	SB_AD31	114	SB_AD8	146	JTAGDI
19	M1_IRL0	51	$\overline{EPROM\_OE0}$	83	SB_AD30	115	SB_AD7	147	JTAGTMS
20	GND	52	$\overline{FLOPPY\_RD}$	84	SB_AD29	116	SB_AD6	148	AUX2OUT1
21	M2_IRL3	53	$\overline{SER\_IRQ}$	85	SB_AD28	117	SB_AD5	149	FLOP_IRQ
22	EB_A15	54	$\overline{KB\_MS\_IRQ}$	86	SB_AD27	118	SB_AD4	150	AUX2OUT0
23	EB_A14	55	$\overline{AUD\_IRQ}$	87	SB_AD26	119	N/C	151	AUX2IN1
24	EB_A13	56	$\overline{SCSI\_IRQ}$	88	SB_AD25	120	N/C	152	AUX2IN0
25	EB_A12	57	$\overline{ET\_IRQ}$	89	SB_AD24	121	GND	153	M2_IRL0
26	EB_A11	58	$\overline{MOD\_IRQ}$	90	GND	122	SB_AD3	154	M3_IRL3
27	EB_A10	59	$\overline{AERR}$	91	V_{CC}	123	SB_AD2	155	M3_IRL2
28	EB_A9	60	$\overline{GND}$	92	SB_AD23	124	$\overline{SB\_AD1}$	156	M3_IRL1
29	GND	61	V_{CC}	93	SB_AD22	125	SB_AD0	157	M3_IRL0
30	V_{CC}	62	TMR_CLK	94	$\overline{SB\_AD21}$	126	SB_SIZE2	158	GND
31	$\overline{EB\_D7}$	63	$\overline{GEN\_RD}$	95	SB_AD20	127	SB_SIZE1	159	V_{CC}
32	EB_D6	64	$\overline{GEN\_SEL}$	96	SB_AD19	128	SB_SIZE0	160	N/C

Pinout Information



160-Pin PQFP Package Dimensions



Dimension		mm
A	Max	4.01
A1	Min	0.25
	Max	0.36
A2	Min	3.17
	Nom	3.42
	Max	3.65
B	Min	0.22
	Max	0.38
C	Min	0.13
	Max	0.23
D	Min	31.60
	Nom	32.00
	Max	32.40
D1	Min	27.90
	Nom	28.00
	Max	28.10
D3	Ref	25.35
e	BSC	0.65
E	Min	31.60
	Nom	32.00
	Max	32.40
E1	Min	27.90
	Nom	28.00
	Max	28.10
E3	Ref	25.35
L	Min	0.65
	Nom	0.80
	Max	0.95
q	Min	0
	Max	7

Note::
1.Total number of pins is 160.
2.Drawing is not to scale.
3.Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4.Datum plane – H – is located at mold parting line and is coincident with the bottom of the lead, where the lead exits the plastic body. Lead pitch determined at – H –.
5.Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. These dimensions to be determined at – H –.
6.Dimensions D3 and E3 to be centered relative to dimensions D1 and E1, respectively, ±0.200 mm.

ORDERING INFORMATION

Part Number	Description
STP2014PQFP	160-Pin Plastic Quad Flat Package (PQFP)

Document Part Number: STP2014