STP2012QFP

SUN MICROELECTRONICS

July 1997

DMA2

DATA SHEET

SBus DMA Controller

DESCRIPTION

The STP2012 SBus DMA Controller (DMA2) provides three channels for DMA transfers over the SBus. It has three external interfaces designed to provide DMA access to one AMD Am7990 Local Area Network Controller for the Ethernet (LANCE), one NCR 53C90 SCSI controller (ESP), and one programmable Centronics-type parallel port. The STP2012 contains internal buffering for these DMA channels in the form of a cache for the LANCE interface and FIFOs for the ESP and parallel port interfaces. It also contains control/status registers for each of the three interfaces, several ESP and parallel port support registers, and a write buffer for slave accesses to the LANCE.

The STP2012 incorporates a number of features for increasing performance and allowing different modes of operation from earlier versions. Software enables additional features by changing the default values of appropriate mode bits in the control/status registers. By default, the STP2012 is software compatible with earlier versions.

FEATURES

- Supports 10 Mbyte/sec ESP transfers, 1.25 Mbyte/sec Ethernet transfers, and 4 Mbyte/sec parallel port transfers
- Supports 4-word, 8-word, and “no burst” SBus burst modes
- 64-byte internal cache for Ethernet data buffering
- 64-byte internal FIFOs for ESP and parallel port data buffering
- 16-bit write buffer for slave writes to LANCE
- Improved cache and FIFO draining algorithms for better SBus utilization
- Internal address and byte count registers and “NEXT” address/byte count features for data block chaining on ESP and parallel port interfaces
- JTAG test interface
- 160-pin PQFP package

BLOCK, LOGIC, AND TYPICAL APPLICATION DIAGRAMS

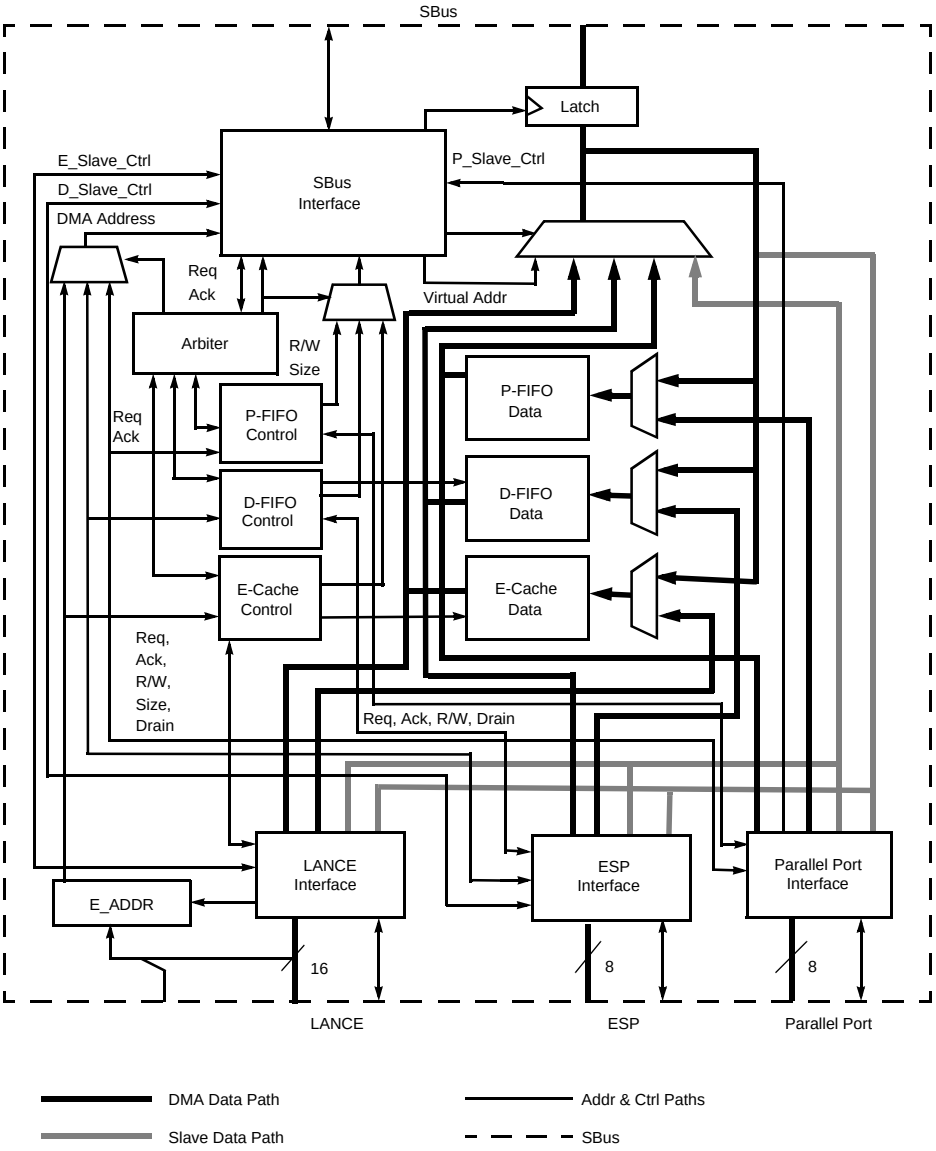


Figure 1. STP2012 Block Diagram

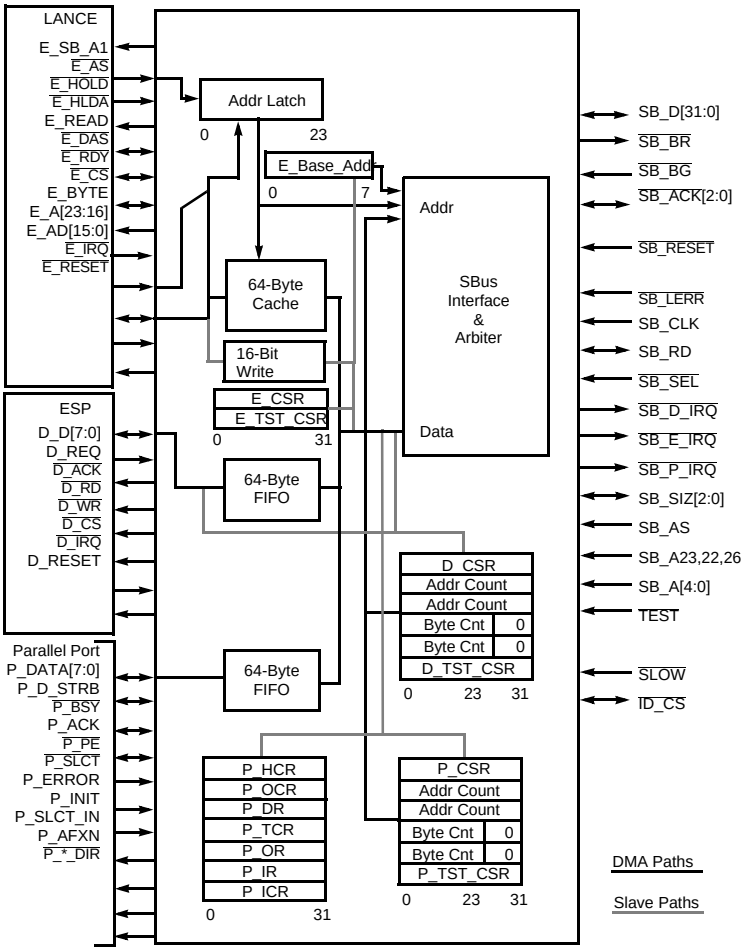


Figure 2. STP2012 Logical Connections

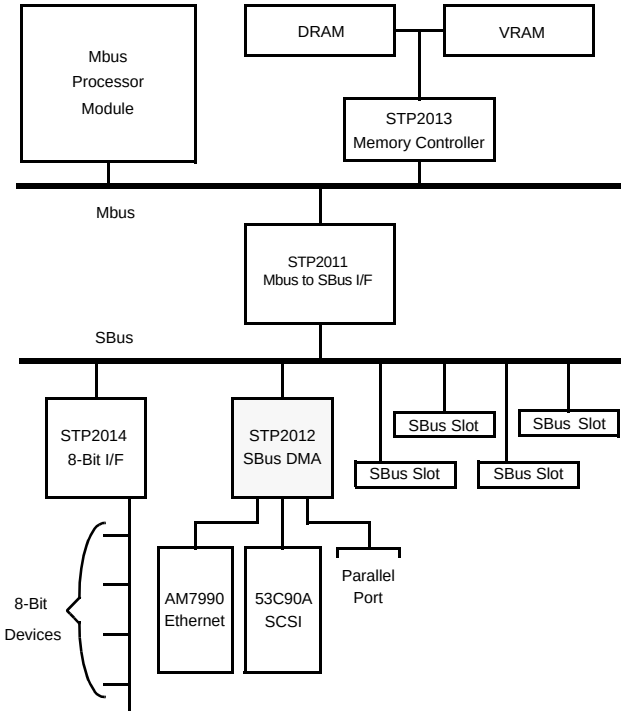


Figure 3. STP2012 Typical Application

SIGNAL DESCRIPTIONS

SBus Interface

Signal	Type	Description
SB_A[4:0]	Input	Low order physical address bits
$\overline{\text{SB\_ACK}}$[2:0]	Input/Output	SBus acknowledge
$\overline{\text{SB\_AS}}$	Input	SBus address strobe
SB_AX	Input	High-order physical address bit (for slave decodes)
SB_AY	Input	High-order physical address bit
SB_AZ	Input	High-order physical address bit
$\overline{\text{SB\_BG}}$	Input	SBus bus grant
$\overline{\text{SB\_BR}}$	Output	SBus bus request
SB_CLK	Input	SBus clock
SB_D[31:0]	Input/Output	SBus data bus
$\overline{\text{SB\_D\_IRQ}}$	Input/Output	SBus interrupt for ESP transfers
$\overline{\text{SB\_E\_IRQ}}$	Input/Output	SBus interrupt for LANCE transfers
$\overline{\text{SB\_LERR}}$	Input	SBus late error (INT15)
$\overline{\text{SB\_P\_IRQ}}$	Input/Output	SBus interrupt for parallel port transfers
SB_RD	Input/Output	SBus read/write
$\overline{\text{SB\_RESET}}$	Input	SBus reset
$\overline{\text{SB\_SEL}}$	Input	SBus select
SB_SIZ[2:0]	Input/Output	SBus transfer size

LANCE Interface

Signal	Type	Description
E_A[23:16]	Input	LANCE high order address
E_AD[15:0]	Input/Output	LANCE address/data bus
$\overline{\text{E\_AS}}$	Input	LANCE address strobe
E_BYTE	Input	LANCE byte marker
$\overline{\text{E\_CS}}$	Output	LANCE chip select
$\overline{\text{E\_DAS}}$	Input/Output	LANCE data strobe
$\overline{\text{E\_HLDA}}$	Output	LANCE hold acknowledge
$\overline{\text{E\_HOLD}}$	Input	LANCE hold
$\overline{\text{E\_IRQ}}$	Input	LANCE interrupt request
$\overline{\text{E\_RDY}}$	Input/Output	LANCE ready
E_READ	Input/Output	LANCE read
$\overline{\text{E\_RESET}}$	Output	LANCE reset
E_SB_A1	Output	Buffered version of SBA1 for LANCE

ESP Interface

Signal	Type	Description
$\overline{\text{D\_ACK}}$	Output	ESP DMA acknowledge
$\overline{\text{D\_CS}}$	Output	ESP chip select
D_D[7:0]	Input/Output	ESP data bus
$\overline{\text{D\_IRQ}}$	Input	ESP interrupt request
$\overline{\text{D\_RD}}$	Output	ESP read strobe
D_REQ	Input	ESPI DMA request
D_RESET	Output	ESP reset
$\overline{\text{D\_WR}}$	Output	ESP write strobe
$\overline{\text{ID\_CS}}$	Input/Output	Secondary device select (boot PROM)

Parallel Port Interface

Signal	Type	Description
P_ACK	Input/Output	Parallel port acknowledge
$\overline{\text{P\_ACK\_DIR}}$ [1]	Output	Parallel port acknowledge direction
P_AFXN	Output	Parallel port auto feed
$\overline{\text{P\_BSY}}$	Input/Output	Parallel port busy
$\overline{\text{P\_BSY\_DIR}}$ [1]	Output	Parallel port busy direction
P_DATA[7:0]	Input/Output	Parallel port data bus
$\overline{\text{P\_D\_DIR}}$[1]	Output	Parallel port data direction
$\overline{\text{P\_DS\_DIR}}$[1]	Output	Parallel port data strobe direction
P_DS_TRB	Input/Output	Parallel port data strobe
P_ERROR	Input	Parallel port error
P_INIT	Output	Parallel port initialize
$\overline{\text{P\_PE}}$	Input	Parallel port paper error
$\overline{\text{P\_SLCT}}$	Input	Parallel port select
P_SLCT_IN	Output	Parallel port select in

1. The parallel port direction bits, $\overline{\text{P\_ACK\_DIR}}$, $\overline{\text{P\_BSY\_DIR}}$, $\overline{\text{P\_D\_DIR}}$, and $\overline{\text{P\_DS\_DIR}}$, have the following polarity: asserted ($\overline{\text{P\_*\_DIR}}$=0) sets transfer direction toward the STP2012, unasserted ($\overline{\text{P\_*\_DIR}}$=1) sets transfer direction away from the STP2012.

Miscellaneous

Signal	Type	Description
B_SB_CLK	Output	Buffered SBus clock output
CONFIG	Input	Package selection
JTAGCLK	Input	JTAG clock
JTAGDI	Input	JTAG data input
JTAGDO	Output	JTAG data output
JTAGTMS	Input	JTAG test mode select
$\overline{\text{SLOW}}$	Input	Fast (high) or slow (low) DMA acknowledge cycles
$\overline{\text{TEST}}$	Input	Test control. Low enables BSBCLK as parametric test output and 3-states all 3-statable outputs and bidirectionals
$\overline{\text{TP\_AUI}}$	Output	Ethernet select output

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Symbol	Parameter	Min	Max	Units
V_{CC}	DC supply	-0.3	7.0	V
V_{IN}	Input voltage	-0.3	GND ≤ V_{IN} ≤ V_{CC}	V
I_{IN}	DC input current	-10	+10	mA
T_{STG}	Storage temperature range (plastic)	-40	125	°°C

1. Referenced to GND.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	DC supply	4.75	5.25	V
T_A	Ambient temperature	0	70	°°C

DC Characteristics

Symbol	Parameter	Conditions [1]	Min	Typ	Max	Units
V_{IH}	Voltage input high	$4.75 < V_{CC} < 5.25$	2.0	–	–	V
V_{IL}	Voltage input low	$4.75 < V_{CC} < 5.25$	–	–	0.8	V
V_{OH}	Voltage output high	I_{OH} = -4.0, -8.0 mA	2.4	4.5	–	V
V_{OL}	Voltage output low	I_{OL} = 4.0, 8.0 mA	–	0.2	0.4	V
I_{IL}	Current input leakage	V_{CC} = MAX, $V_{IN} = V_{CC}$ or GND	-10	±1	10	µA
I_{IPU}	Current input pull-up	V_{CC} = MAX, V_{IN} = GND or 3.5 V	-175	–	-2	µA
I_{IPD}	Current input pull-down	V_{CC} = MAX, V_{IN} = GND or 0.8 V	2	–	179	µA
I_{OZ}	Current 3-state output leakage	V_{CC} = MAX, V_{OUT} = GND or V_{CC}	-10	±1	10	µA
I_{OZU}	Current 3-state output w/ pull-up	V_{OUT} = GND or 3.5 V	-175	–	-2	µA
I_{OZD}	Current 3-state output w/ pull-down	V_{OUT} = GND or 0.8 V	2	–	179	µA
I_{OSP4}	Current P-channel output short circuit (4 mA output buffers) [2]	V_{CC} = MAX, V_{OUT} = GND	-140	-70	-25	mA
I_{OSN4}	Current N-channel output short circuit (4 mA output buffers) [2]	V_{CC} = MAX, $V_{OUT} = V_{CC}$	30	75	140	mA
I_{DD}	Quiescent supply current	$V_{IN} = V_{CC}$ or GND	–	–	2	mA
I_{CC}	Dynamic supply current	V_{CC} = MAX, f = 25 MHz	–	125	200	mA

1. Specified at V_{CC} equals 5V ± 5% at ambient temperature over the specified range.
2. Not more than one output may be shorted at a time for a maximum duration of one second.

Capacitance

Symbol	Parameter		Condition	Min	Max	Units
C_{IN}	Input capacitance	CLK input	V_{IN} = 5.0 V, T_A = 25°C, f = 1 MHz		12	pF
		All other inputs	V_{IN} = 5.0 V, T_A = 25°C, f = 1 MHz		6	pF
C_{OUT}	Output capacitance		V_{IN} = 5.0 V, T_A = 25°C, f = 1 MHz		5.5	pF
C_{BID}	Bidirectional capacitance		V_{IN} = 5.0 V, T_A = 25°C, f = 1 MHz		6	pF

AC Characteristics: Output Delay Timing

Signal Relative to SB_CLK	Output Delay (ns)
B_SB_CLK	39
$\overline{\text{D\_ACK}}$	30
$\overline{\text{D\_CS}}$	30
D_D[7:0]	30
$\overline{\text{D\_RD}}$	30
D_RESET	30
$\overline{\text{D\_WR}}$	30
E_AD[15:0]	30
$\overline{\text{E\_CS}}$	30
$\overline{\text{E\_DAS}}$	30
$\overline{\text{E\_HLDA}}$	30
$\overline{\text{E\_RDY}}$	30
E_READ	30
$\overline{\text{E\_RESET}}$	30
E_SB_A1	30
$\overline{\text{ID\_CS}}$	30
JTAGDO	30
$\overline{\text{TP\_AUI}}$	30
P_ACK	30
$\overline{\text{P\_ACK\_DIR}}$	30
P_AFXN	30
$\overline{\text{P\_BSY}}$	30
$\overline{\text{P\_BSY\_DIR}}$	30
P_DATA[7:0]	30
$\overline{\text{P\_DS\_DIR}}$	34
$\overline{\text{P\_D\_DIR}}$	30
P_D_STRB	30
P_INIT	30
P_SLCT_IN	30
$\overline{\text{SB\_ACK}}$[2:0]	26
$\overline{\text{SB\_BR}}$	26
SB_D[31:0]	26
$\overline{\text{SB\_D\_IRQ}}$	26
$\overline{\text{SB\_E\_IRQ}}$	26
$\overline{\text{SB\_P\_IRQ}}$	26
SB_RD	26
SB_SIZ[2:0]	26

The following table lists the minimum setup and hold time of each output or bidirectional signal relative to SB_CLK. The second and third columns contain the setup and hold time measured from the *rising* edge of each signal to the rising edge of SB_CLK. The fourth and fifth columns contain the same times but measured from the *falling* edge of each signal to the rising edge of SB_CLK.

AC Characteristics: Setup and Hold Times

	Rising Edge		Falling Edge	
Signal Relative to SB_CLK	**Setup (Min)**	**Hold (Min)**	**Setup (Min)**	**Hold (Min)**
CONFIG	15	3	15	3
D_D[7:0]	15	3	15	3
$\overline{\text{D\_IRQ}}$	15	3	15	3
D_REQ	15	3	15	3
E_A[23:16]	15	3	15	3
E_AD[15:0]	15	3	15	3
$\overline{\text{E\_AS}}$	15	10	15	10
E_BYTE	15	10	15	10
$\overline{\text{E\_DAS}}$	15	10	15	10
$\overline{\text{E\_HOLD}}$	15	10	15	10
$\overline{\text{E\_IRQ}}$	15	10	15	10
$\overline{\text{E\_RDY}}$	15	10	15	10
E_READ	15	10	15	10
$\overline{\text{ID\_CS}}$	15	3	15	3
JTAGCLK	15	3	15	3
JTAGDI	15	3	15	3
JTAGTMS	15	3	15	3
P_ACK	15	3	15	3
$\overline{\text{P\_BSY}}$	15	3	15	3
P_DATA[7:0]	15	3	15	3
P_D_STRB	15	3	15	3
P_ERROR	15	3	15	3
$\overline{\text{P\_PE}}$	15	3	15	3
$\overline{\text{P\_SLCT}}$	15	3	15	3
SB_A[4:0]	15	3	15	3
$\overline{\text{SB\_ACK}}$	15	3	15	3
$\overline{\text{SB\_AS}}$	15	3	15	3
SB_AX	15	3	15	3

AC Characteristics: Setup and Hold Times (Continued)

Signal Relative to SB_CLK	Rising Edge		Falling Edge	
	Setup (Min)	Hold (Min)	Setup (Min)	Hold (Min)
SB_AY	15	3	15	3
SB_AZ	15	3	15	3
$\overline{\text{SB\_BG}}$	15	3	15	3
SB_D[31:0]	15	3	15	3
$\overline{\text{SB\_D\_IRQ}}$	15	3	15	3
$\overline{\text{SB\_E\_IRQ}}$	15	3	15	3
$\overline{\text{SB\_LERR}}$	15	3	15	3
SB_RD	15	3	15	3
$\overline{\text{SB\_RESET}}$	38	1	38	1
$\overline{\text{SB\_SEL}}$	15	3	15	3
SB_SIZ[2:0]	15	3	15	3
$\overline{\text{SLOW}}$	15	3	15	3
$\overline{\text{TEST}}$	38	1	38	1

TIMING DIAGRAM

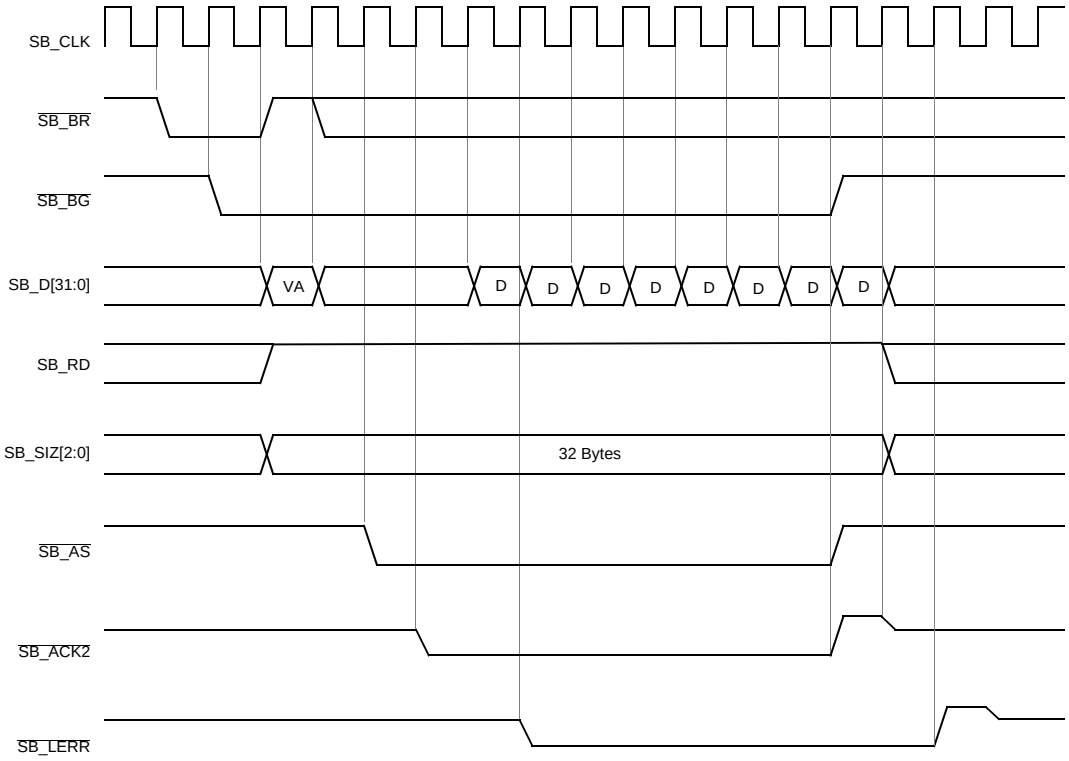
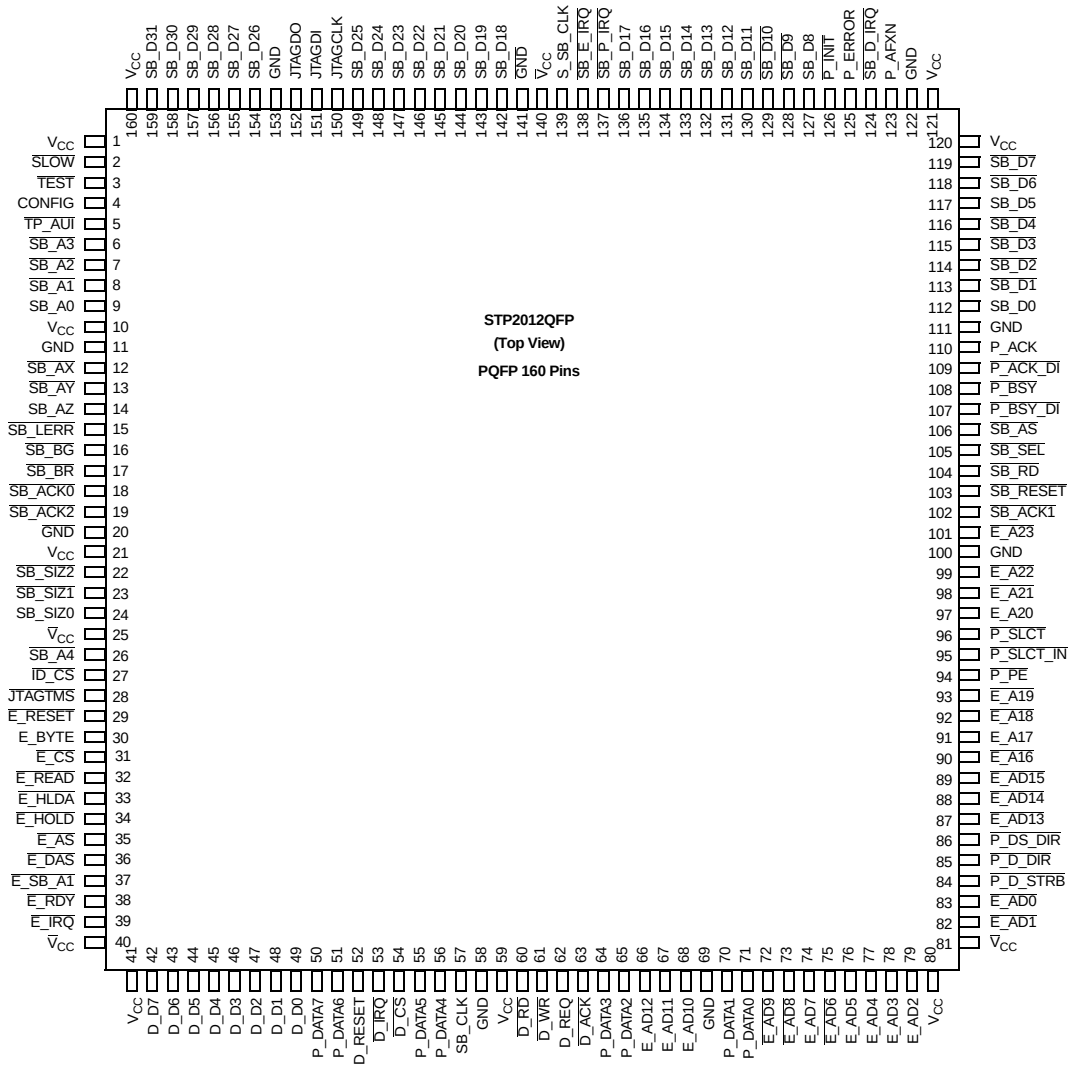


Figure 4. SBus DMA Burst Read

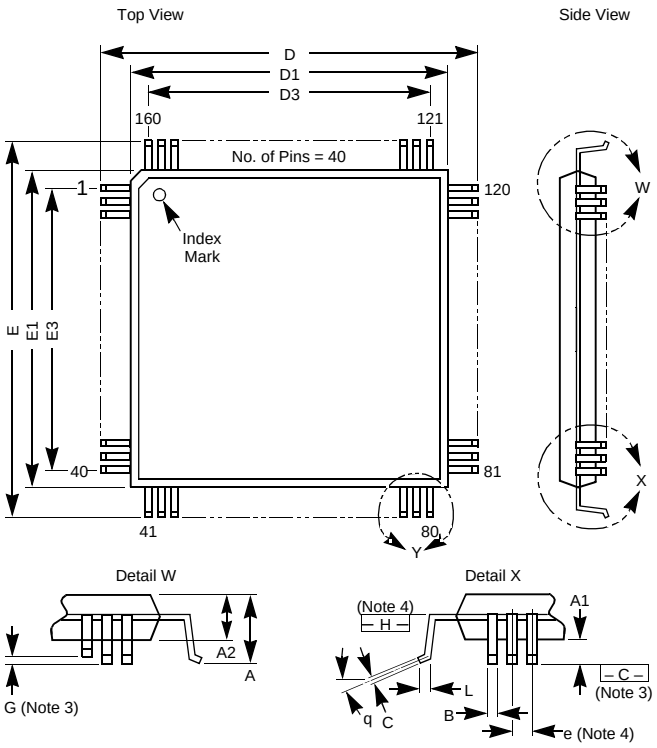
PACKAGE INFORMATION

160-Pin PQFP Pin Assignments

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	V_{CC}	33	$\overline{E\_HLDA}$	65	P_DATA2	97	E_A20	129	SB_D10
2	$\overline{SLOW}$	34	$\overline{E\_HOLD}$	66	E_AD12	98	E_A21	130	SB_D11
3	$\overline{TEST}$	35	$\overline{E\_AS}$	67	E_AD11	99	E_A22	131	SB_D12
4	CONFIG	36	$\overline{E\_DAS}$	68	E_AD10	100	GND	132	SB_D13
5	$\overline{TP\_AUI}$	37	E_SB_A1	69	GND	101	E_A23	133	SB_D14
6	SB_A3	38	$\overline{E\_RDY}$	70	P_DATA1	102	$\overline{SB\_ACK1}$	134	SB_D15
7	SB_A2	39	$\overline{E\_IRQ}$	71	P_DATA0	103	$\overline{SB\_RESET}$	135	SB_D16
8	SB_A1	40	V_{CC}	72	E_AD9	104	SB_RD	136	$\overline{SB\_D17}$
9	SB_A0	41	V_{CC}	73	E_AD8	105	$\overline{SB\_SEL}$	137	$\overline{SB\_P\_IRQ}$
10	V_{CC}	42	D_D7	74	E_AD7	106	$\overline{SB\_AS}$	138	$\overline{SB\_E\_IRQ}$
11	GND	43	D_D6	75	E_AD6	107	$\overline{P\_BSY\_DIR}$	139	S_SB_CLK
12	SB_AX	44	D_D5	76	E_AD5	108	$\overline{P\_BSY}$	140	V_{CC}
13	SB_AY	45	D_D4	77	E_AD4	109	$\overline{P\_ACK\_DIR}$	141	GND
14	SB_AZ	46	D_D3	78	E_AD3	110	P_ACK	142	SB_D18
15	$\overline{SB\_LERR}$	47	D_D2	79	E_AD2	111	GND	143	SB_D19
16	$\overline{SB\_BG}$	48	D_D1	80	V_{CC}	112	SB_D0	144	SB_D20
17	$\overline{SB\_BR}$	49	D_D0	81	V_{CC}	113	SB_D1	145	SB_D21
18	$\overline{SB\_ACK0}$	50	P_DATA7	82	E_AD1	114	SB_D2	146	SB_D22
19	$\overline{SB\_ACK2}$	51	P_DATA6	83	E_AD0	115	SB_D3	147	SB_D23
20	GND	52	D_RESET	84	P_D_STRB	116	SB_D4	148	SB_D24
21	V_{CC}	53	$\overline{D\_IRQ}$	85	$\overline{P\_D\_DIR}$	117	SB_D5	149	SB_D25
22	SB_SIZ2	54	$\overline{D\_CS}$	86	$\overline{P\_DS\_DIR}$	118	SB_D6	150	JTAGCLK
23	SB_SIZ1	55	P_DATA5	87	E_AD13	119	SB_D7	151	JTAGDI
24	SB_SIZ0	56	P_DATA4	88	E_AD14	120	V_{CC}	152	JTAGDO
25	V_{CC}	57	SB_CLK	89	E_AD15	121	V_{CC}	153	GND
26	SB_A4	58	GND	90	E_A16	122	GND	154	SB_D26
27	$\overline{ID\_CS}$	59	V_{CC}	91	E_A17	123	P_AFXN	155	SB_D27
28	JTAGTMS	60	$\overline{D\_RD}$	92	E_A18	124	$\overline{SB\_D\_IRQ}$	156	SB_D28
29	$\overline{E\_RESET}$	61	$\overline{D\_WR}$	93	E_A19	125	P_ERROR	157	SB_D29
30	E_BYTE	62	D_REQ	94	$\overline{P\_PE}$	126	P_INIT	158	SB_D30
31	$\overline{E\_CS}$	63	$\overline{D\_ACK}$	95	P_SLCT_IN	127	SB_D8	159	SB_D31
32	E_READ	64	P_DATA3	96	$\overline{P\_SLCT}$	128	SB_D9	160	V_{CC}


STP2012QFP
(Top View)
PQFP 160 Pins
1 VCC
2 SLOW
3 TEST
4 CONFIG
5 TP_AUI
6 SB_A3
7 SB_A2
8 SB_A1
9 SB_A0
10 VCC
11 GND
12 SB_AX
13 SB_AY
14 SB_AZ
15 SB_LERR
16 SB_BG
17 SB_BR
18 SB_ACK0
19 SB_ACK2
20 GND
21 VCC
22 SB_SIZ2
23 SB_SIZ1
24 SB_SIZ0
25 VCC
26 SB_A4
27 ID_CS
28 JTAGTMS
29 E_RESET
30 E_BYTE
31 E_CS
32 E_READ
33 E_HLDA
34 E_HOLD
35 E_AS
36 E_DAS
37 E_SB_A1
38 E_RDY
39 E_IRQ
40 VCC
41 VCC
42 D_D7
43 D_D6
44 D_D5
45 D_D4
46 D_D3
47 D_D2
48 D_D1
49 D_D0
50 P_DATA7
51 P_DATA6
52 D_RESET
53 D_IRQ
54 D_CS
55 P_DATA5
56 P_DATA4
57 SB_CLK
58 GND
59 VCC
60 D_RD
61 D_WR
62 D_REQ
63 D_ACK
64 P_DATA3
65 P_DATA2
66 E_AD12
67 E_AD11
68 E_AD10
69 GND
70 P_DATA1
71 P_DATA0
72 E_AD9
73 E_AD8
74 E_AD7
75 E_AD6
76 E_AD5
77 E_AD4
78 E_AD3
79 E_AD2
80 VCC
81 VCC
82 E_AD1
83 E_AD0
84 P_D_STRB
85 P_D_DIR
86 P_DS_DIR
87 E_AD13
88 E_AD14
89 E_AD15
90 E_A16
91 E_A17
92 E_A18
93 E_A19
94 P_PE
95 P_SLCT_IN
96 P_SLCT
97 E_A20
98 E_A21
99 E_A22
100 GND
101 E_A23
102 SB_ACK1
103 SB_RESET
104 SB_RD
105 SB_SEL
106 SB_AS
107 P_BSY_DI
108 P_BSY
109 P_ACK_DI
110 P_ACK
111 GND
112 SB_D0
113 SB_D1
114 SB_D2
115 SB_D3
116 SB_D4
117 SB_D5
118 SB_D6
119 SB_D7
120 VCC
121 VCC
122 GND
123 P_AFXN
124 SB_D_IRQ
125 P_ERROR
126 P_INIT
127 SB_D8
128 SB_D9
129 SB_D10
130 SB_D11
131 SB_D12
132 SB_D13
133 SB_D14
134 SB_D15
135 SB_D16
136 SB_D17
137 SB_P_IRQ
138 SB_E_IRQ
139 S_SB_CLK
140 VCC
141 GND
142 SB_D18
143 SB_D19
144 SB_D20
145 SB_D21
146 SB_D22
147 SB_D23
148 SB_D24
149 SB_D25
150 JTAGCLK
151 JTAGDI
152 JTAGDO
153 GND
154 SB_D26
155 SB_D27
156 SB_D28
157 SB_D29
158 SB_D30
159 SB_D31
160 VCC

160-Pin PQFP Package Dimensions



Dimension		mm
A	Max	4.01
A1	Min	0.25
	Max	0.36
A2	Min	3.17
	Nom	3.42
	Max	3.65
B	Min	0.22
	Max	0.38
C	Min	0.13
	Max	0.23
D	Min	31.60
	Nom	32.00
	Max	32.40
D1	Min	27.90
	Nom	28.00
	Max	28.10
D3	Ref	25.35
e	BSC	0.65
E	Min	31.60
	Nom	32.00
	Max	32.40
E1	Min	27.90
	Nom	28.00
	Max	28.10
E3	Ref	25.35
L	Min	0.65
	Nom	0.80
	Max	0.95
q	Min	0°
	Max	7°

Note:
1. Total number of pins is 160.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Datum plane – H – is located at mold parting line and is coincident with the bottom of the lead, where the lead exits the plastic body. Lead pitch determined at – H –.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. These dimensions to be determined at – H –.
6. Dimensions D3 and E3 to be centered relative to dimensions D1 and E1, respectively, ±0.200 mm.

ORDERING INFORMATION

Part Number	Description
STP2012PQFP	160-Pin Plastic Quad Flat Pack (PQFP)

Document Part Number: STP2012