

SERIAL 16K (2K x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
 - 4.5V to 5.5V for ST24164 version
 - 2.5V to 5.5V for ST25164 version
- HARDWARE WRITE CONTROL PIN
- TWO WIRE SERIAL INTERFACE
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES

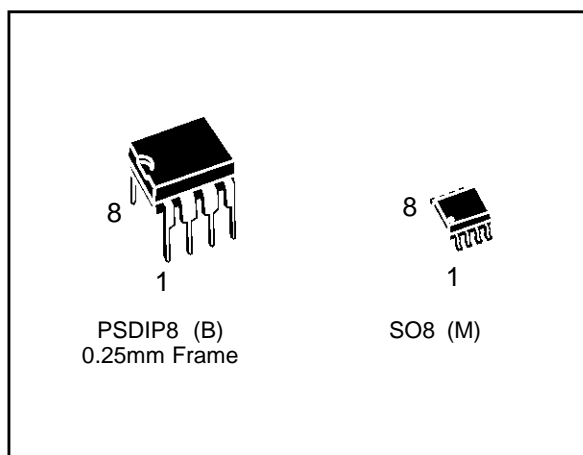


Figure 1. Logic Diagram

DESCRIPTION

The ST24/25164 are 16K bit electrically erasable programmable memories (EEPROM), organized as 2048 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
\overline{WC}	Write Control
V _{CC}	Supply Voltage
V _{SS}	Ground

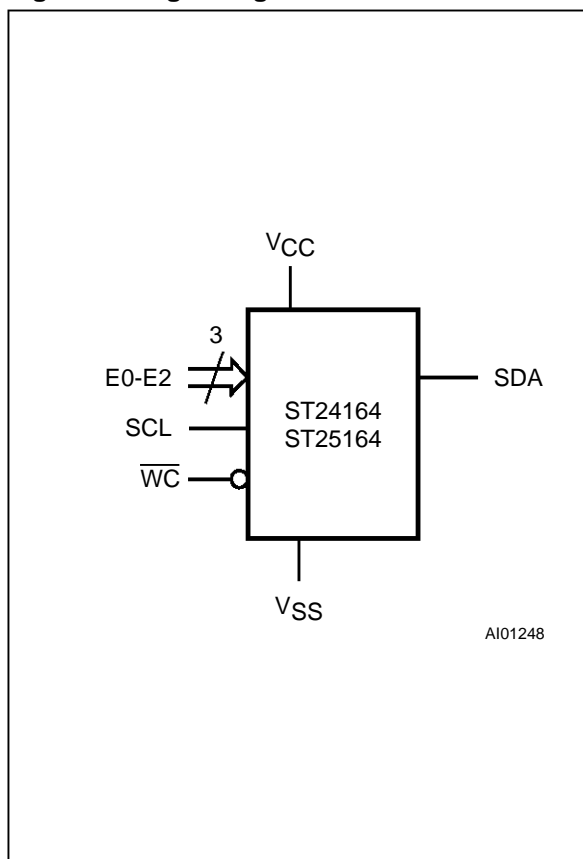


Figure 2A. DIP Pin Connections

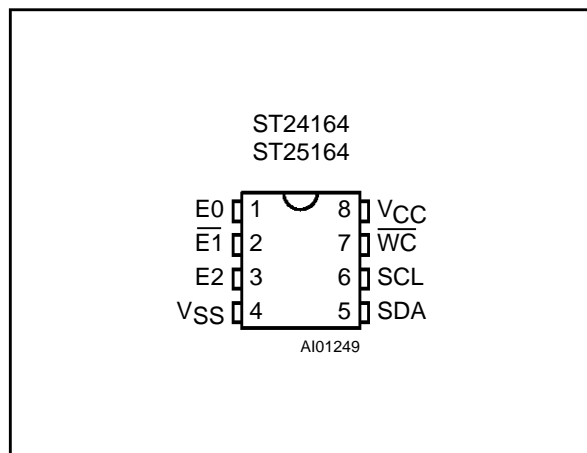


Figure 2B. SO Pin Connections

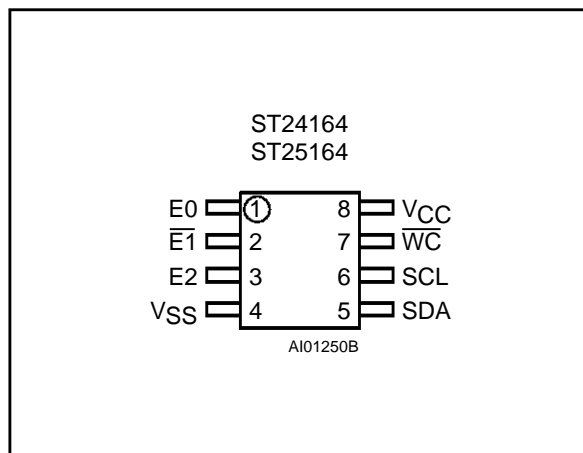


Table 2. Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	−40 to 125	°C
T _{STG}	Storage Temperature	−65 to 150	°C
T _{LEAD}	Lead Temperature, Soldering (SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V _O	Output Voltage	−0.6 to 6.5	V
V _I	Input Voltage	−0.6 to 6.5	V
V _{CC}	Supply Voltage	−0.3 to 6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model) ⁽²⁾	4000	V
	Electrostatic Discharge Voltage (Machine model) ⁽³⁾	500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).

3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the two wire serial interface which uses a bi-directional data bus and serial clock. The memories offer 3 chip enable inputs (E2, E1, E0) so that up to 8 x 16K devices may be attached to the bus and selected individually. The memories behave as a slave device with all memory operations synchronized by the serial clock.

Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits, plus one read/write bit and terminated by an acknowledge bit (see Table 3).

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Table 3. Device Select Code

		Chip Enable			MSB Address			R \overline{W}
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	E2	$\overline{E1}$	E0	A10	A9	A8	R \overline{W}

Note: The MSB b7 is sent first.

Table 4. Operating Modes ⁽¹⁾

Mode	R \overline{W} bit	\overline{WC} pin	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R \overline{W} = '1'
Random Address Read	'0'	X	1	START, Device Select, R \overline{W} = '0', Address,
	'1'			reSTART, Device Select, R \overline{W} = '1'
Sequential Read	'1'	X	1 to 2048	Similar to Current or Random Mode
Byte Write	'0'	V _{IL}	1	START, Device Select, R \overline{W} = '0'
Page Write	'0'	V _{IL}	16	START, Device Select, R \overline{W} = '0'

Notes: 1. X = V_{IH} or V_{IL}

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on

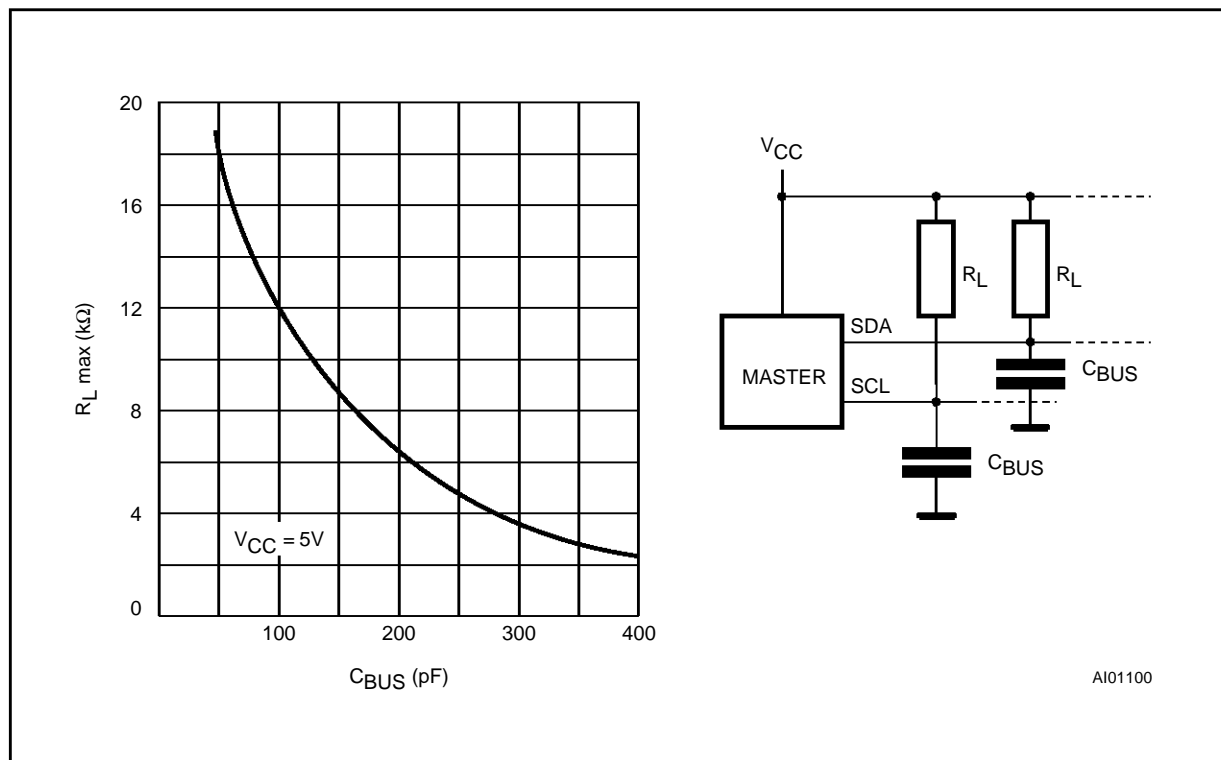
the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E2 - E0). These chip enable inputs are used to set 3 bits (b6, b5, b4) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Write Control (\overline{WC}). An hardware Write Control feature (\overline{WC}) is offered on pin 7. This feature is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (\overline{WC} = V_{IH}) or disable (\overline{WC} = V_{IL}) the internal write protection. \overline{WC} pin can be directly connected to V_{SS} pin, in order to run the ST24/25164 without the Write Control protection. When unconnected, the \overline{WC} input is internally read as V_{IL} (see Table 5).

When \overline{WC} = '1', Device Select and Address bytes are acknowledged; Data bytes are not acknowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for a Serial Bus

DEVICE OPERATION

Bus Background

The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25164 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25164 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25164 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25164 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25164, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a Read or Write bit (R/W).

Three out of the four most significant bits of the Device Select code are the Device Select bits (b6, b5, b4). They are matched to the chip enable signals applied on pins E2, E1, E0. Thus up to 8 x 16K memories can be connected on the same bus giving a memory capacity total of 128K bits.

Table 5. Input Parameters ⁽¹⁾ ($T_A = 25\text{ }^{\circ}\text{C}$, $f = 400\text{ kHz}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	\overline{WC} Input Impedance	$V_{IN} \leq 0.3 V_{CC}$	5	20	k Ω
Z_{WCH}	\overline{WC} Input Impedance	$V_{IN} \geq 0.7 V_{CC}$	500		k Ω
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics

($T_A = 0$ to $70\text{ }^{\circ}\text{C}$ or -40 to $85\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		± 2	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		± 2	μA
I_{CC}	Supply Current (ST24 series)	$V_{CC} = 5V$, $f_C = 100\text{kHz}$ (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	$V_{CC} = 2.5V$, $f_C = 100\text{kHz}$		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5V$		100	μA
		$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5V$, $f_C = 100\text{kHz}$		300	μA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 2.5V$		5	μA
		$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 2.5V$, $f_C = 100\text{kHz}$		50	μA
V_{IL}	Input Low Voltage (SCL, SDA)		-0.3	$0.3 V_{CC}$	V
V_{IH}	Input High Voltage (SCL, SDA)		$0.7 V_{CC}$	$V_{CC} + 1$	V
V_{IL}	Input Low Voltage (E0-E2, WC)		-0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, WC)		$V_{CC} - 0.5$	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage (ST24 series)	$I_{OL} = 3\text{mA}$, $V_{CC} = 5V$		0.4	V
	Output Low Voltage (ST25 series)	$I_{OL} = 2.1\text{mA}$, $V_{CC} = 2.5V$		0.4	V

Table 7. AC Characteristics(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t _{CH1CH2}	t _R	Clock Rise Time		1	μs
t _{CL1CL2}	t _F	Clock Fall Time		300	ns
t _{DH1DH2}	t _R	Input Rise Time		1	μs
t _{DL1DL1}	t _F	Input Fall Time		300	ns
t _{CHDX} ⁽¹⁾	t _{SU:STA}	Clock High to Input Transition	4.7		μs
t _{CHCL}	t _{HIGH}	Clock Pulse Width High	4		μs
t _{DLCL}	t _{HD:STA}	Input Low to Clock Low (START)	4		μs
t _{CLDX}	t _{HD:DAT}	Clock Low to Input Transition	0		μs
t _{CLCH}	t _{LOW}	Clock Pulse Width Low	4.7		μs
t _{DXCX}	t _{SU:DAT}	Input Transition to Clock Transition	250		ns
t _{CHDH}	t _{SU:STO}	Clock High to Input High (STOP)	4.7		μs
t _{DHDL}	t _{BUF}	Input High to Input Low (Bus Free)	4.7		μs
t _{CLQV} ⁽²⁾	t _{AA}	Clock Low to Next Data Out Valid	0.3	3.5	μs
t _{CLQX}	t _{DH}	Data Out Hold Time	300		ns
f _C	f _{SCL}	Clock Frequency		100	kHz
t _W	t _{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.

2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times ≤ 50ns

Input Pulse Voltages 0.2V_{CC} to 0.8V_{CC}Input and Output Timing Ref. Voltages 0.3V_{CC} to 0.7V_{CC}**DEVICE OPERATION (cont'd)**

After a START condition any memory on the bus will identify the device code and compare the 3 bits to its chip enable inputs E2, E1, E0.

The 8th bit sent is the Read or Write bit (R/W), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

The Write Operations are only possible when the Write Control pin is low (WC to ground).

Following a START condition the master sends a device select code with the RW bit reset to '0'. The memory acknowledges and waits for the lower byte address. After receipt of the byte address the device again responds with an acknowledge.

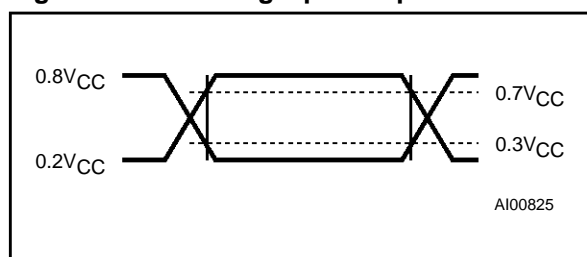
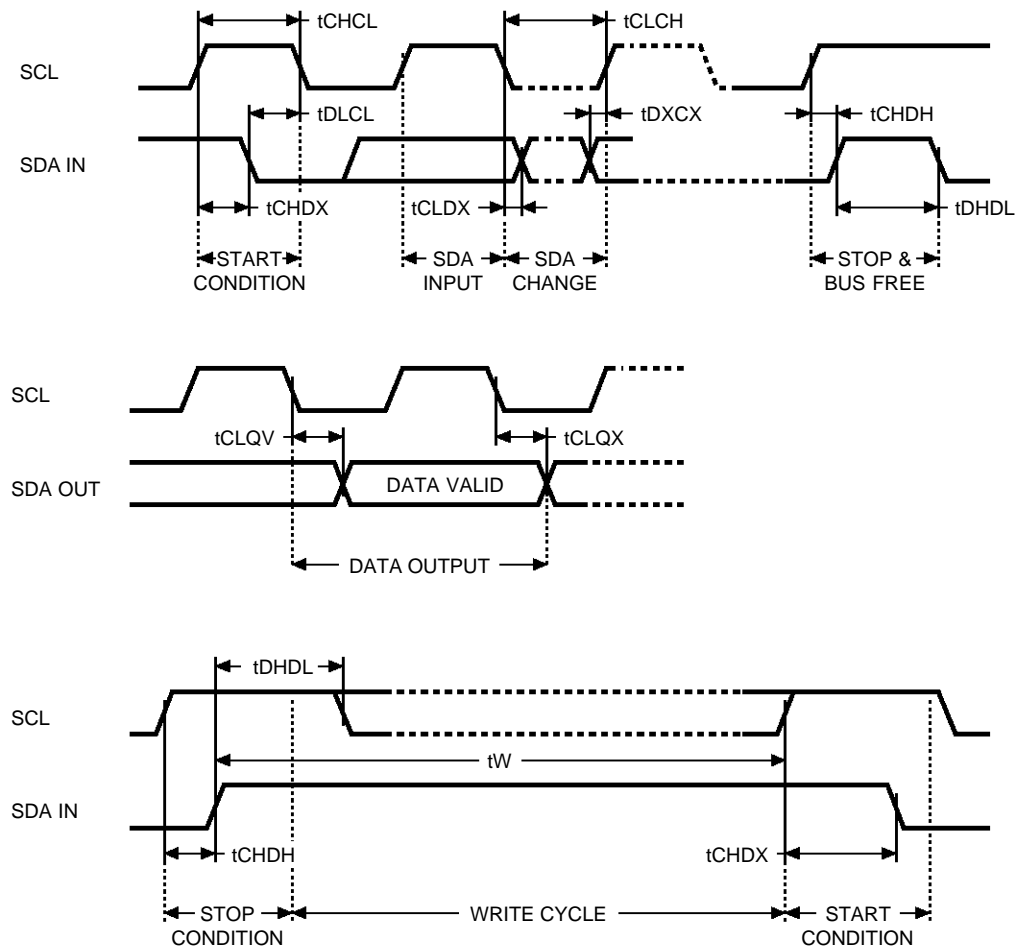
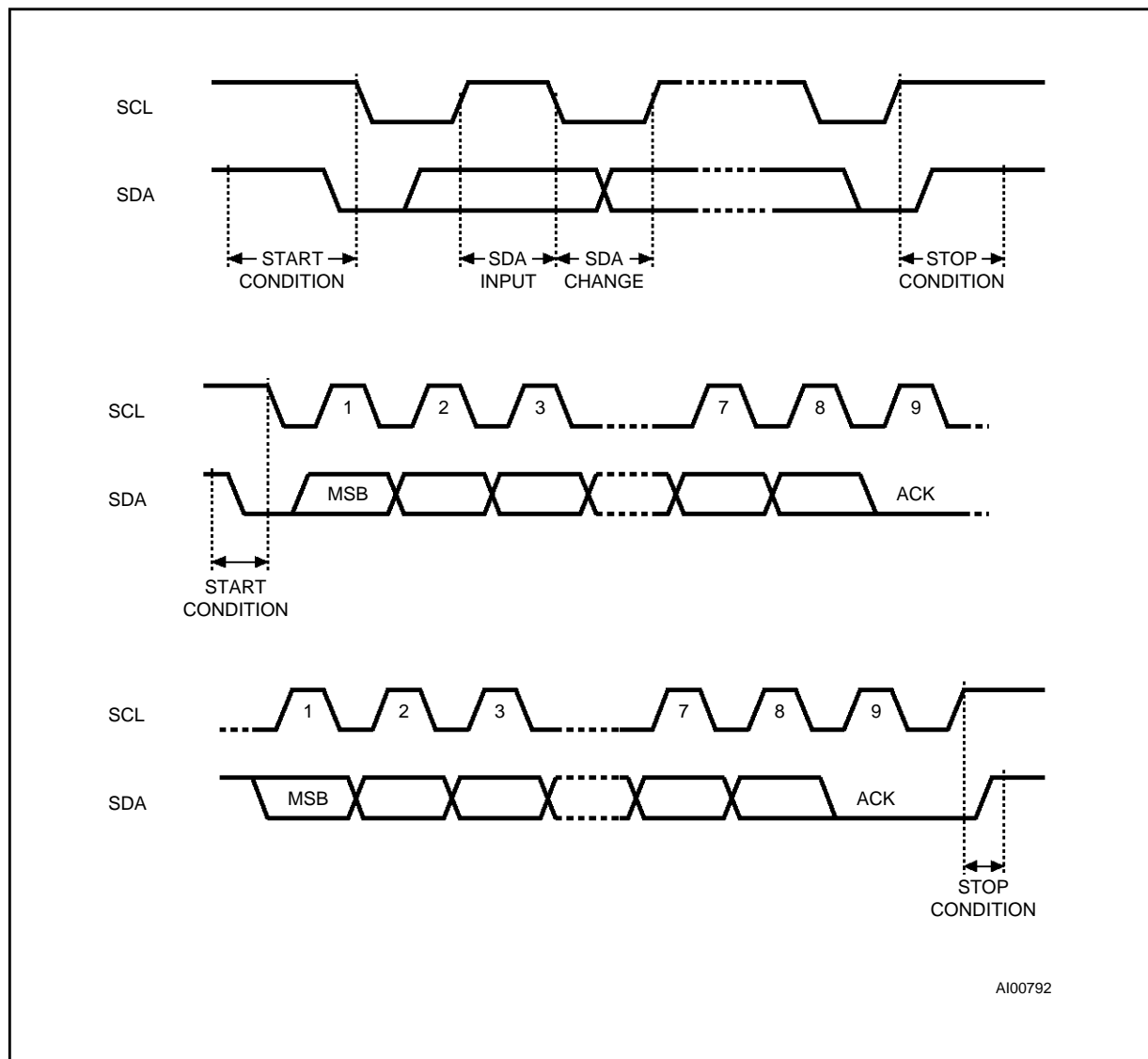
Figure 4. AC Testing Input Output Waveforms

Figure 5. AC Waveforms



AI00795

Figure 6. I²C Bus Protocol

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 4 most significant Byte Address bits (A7-A4) are the same. The master sends from one up to 16 bytes of data, which are each acknowledged by the memory. After each byte is transferred, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter

'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK.

During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_w) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

Read operations are independent of the state of the \overline{WC} pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Figure 7. Write Cycle Polling using ACK

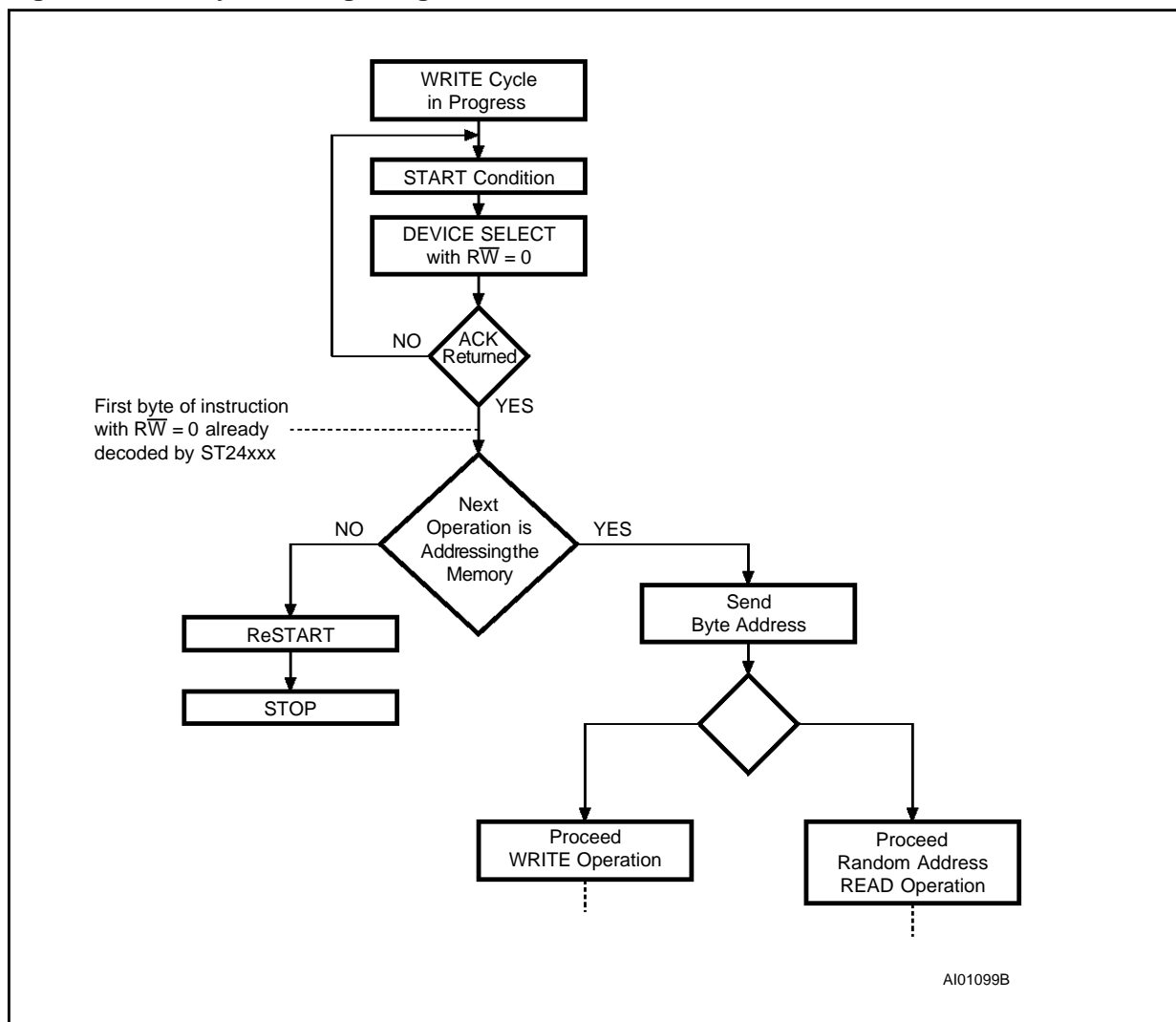
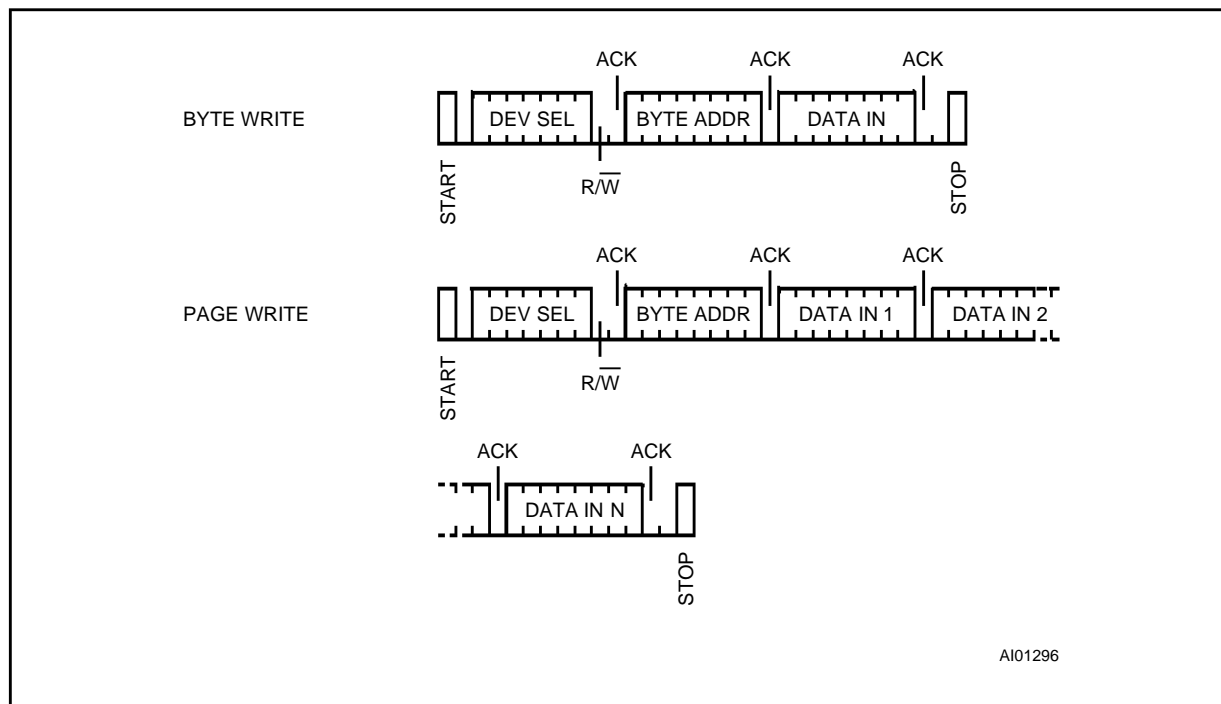


Figure 8. Write Modes Sequence



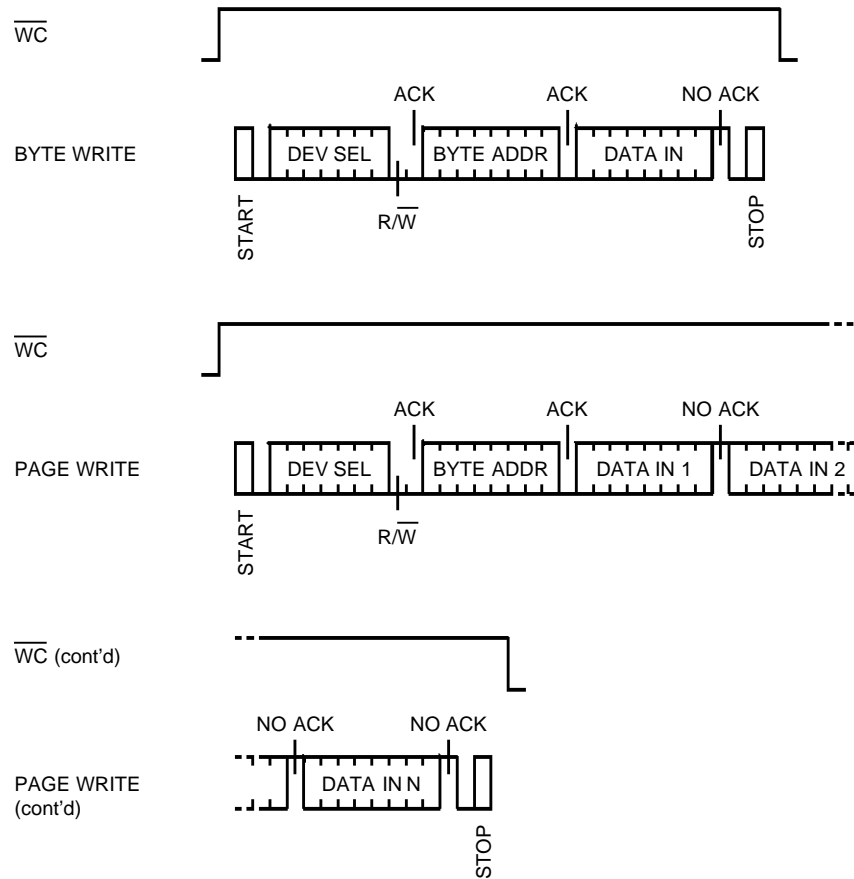
Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence.

To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

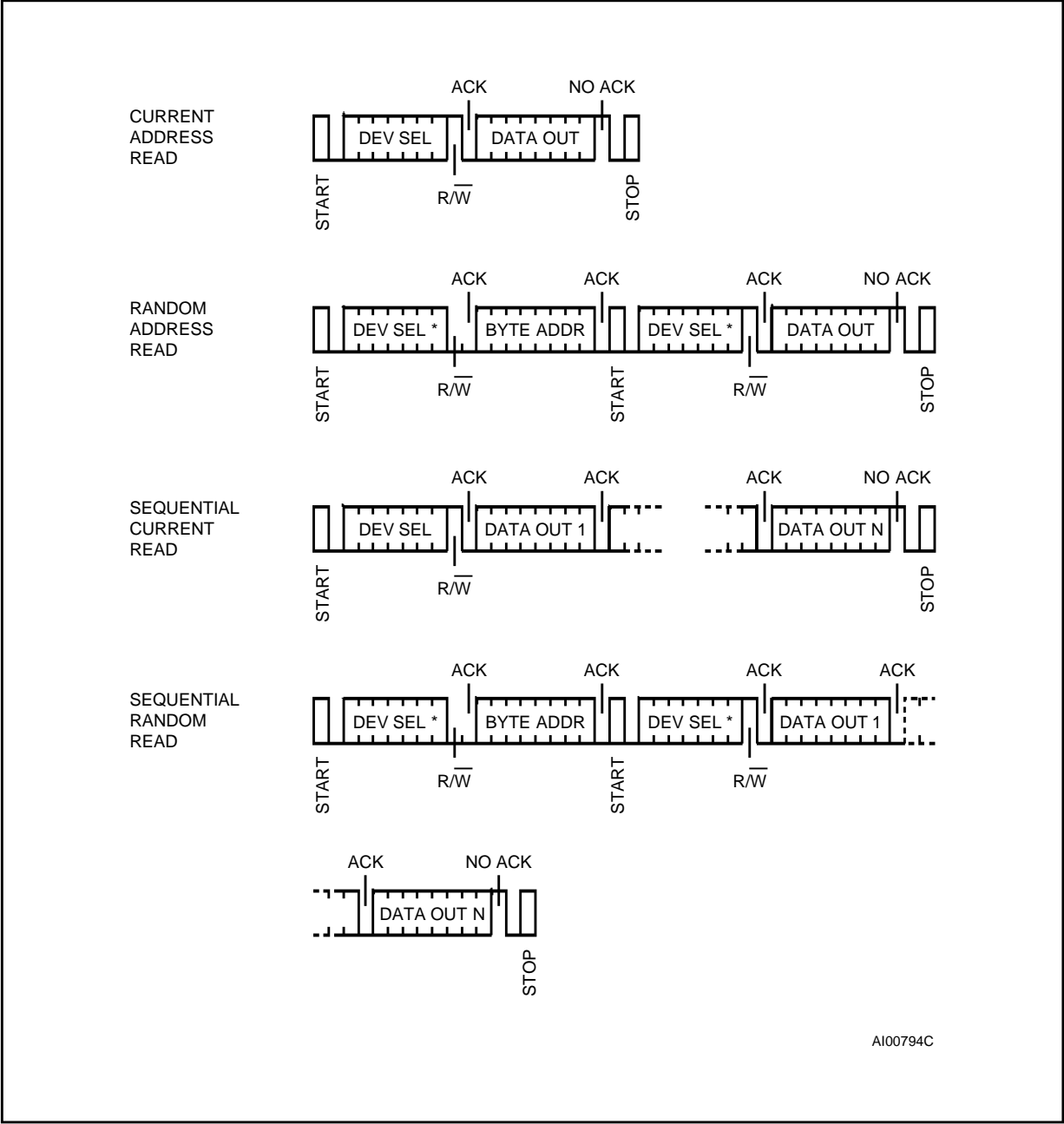
Acknowledge in Read Mode. In all read modes the ST24/25164 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25164 terminates the data transfer and switches to a standby state.

Figure 9. Write Modes Sequence with Write Control = 1



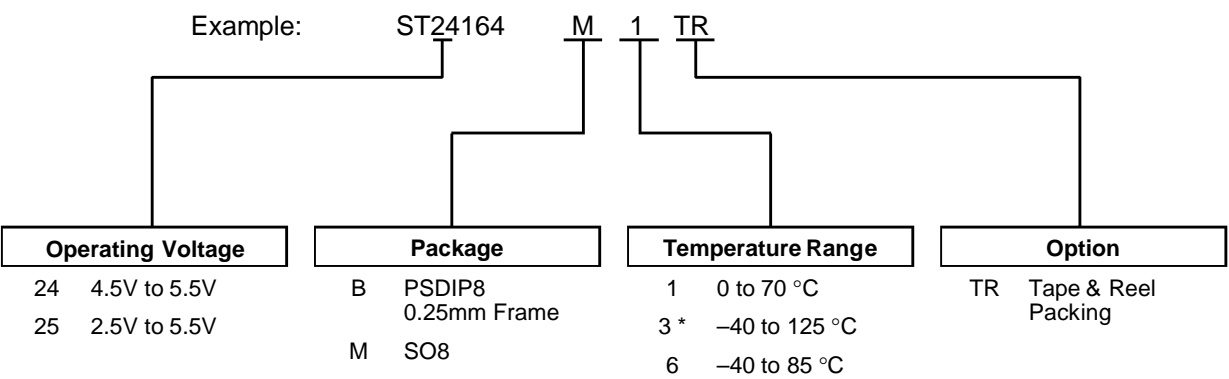
AI01161B

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



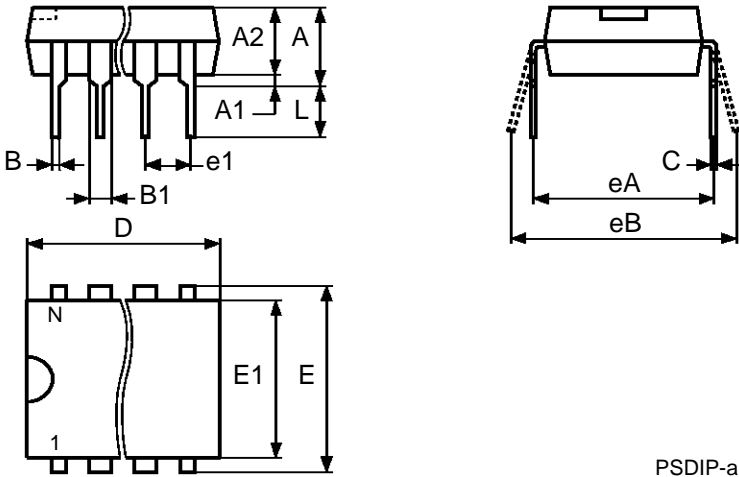
Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	

PSDIP8

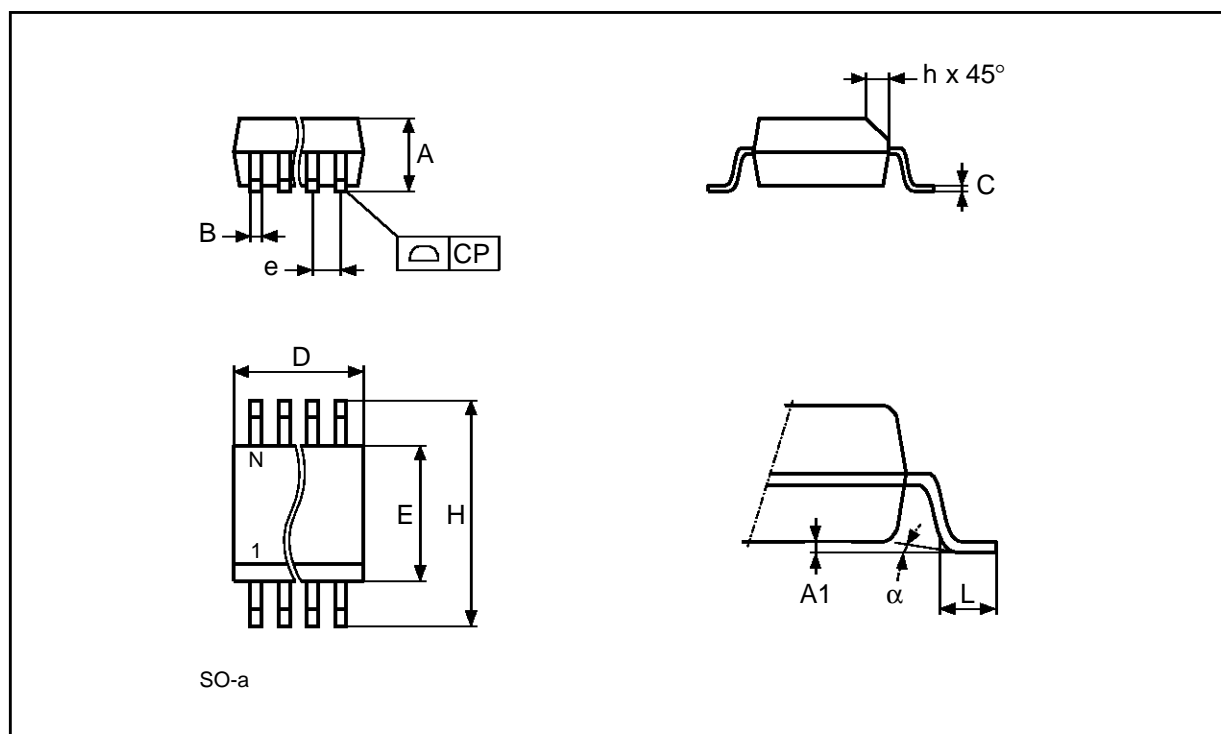


Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	—	—	0.050	—	—
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



Drawing is not to scale

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1995 SGS-THOMSON Microelectronics - All Rights Reserved

Purchase of I²C Components by SGS-THOMSON Microelectronics, conveys a license under the Philips I²C Patent. Rights to use these components in an I²C system, is granted provided that the system conforms to the I²C Standard Specifications as defined by Philips.

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.