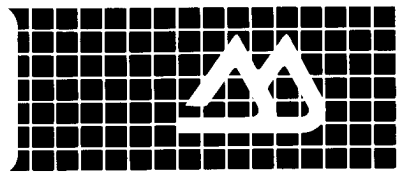


S-130  
T1577

001577

Oug  
sms



# HIGH SPEED 16K BIT CMOS STATIC RAM

SRM2268C<sub>45</sub> • SRM2268C<sub>55</sub> • SRM2268C<sub>70</sub>

test  
04/01/85  
07/21/89

# SRM2268

12/1/85  
Japan  
-

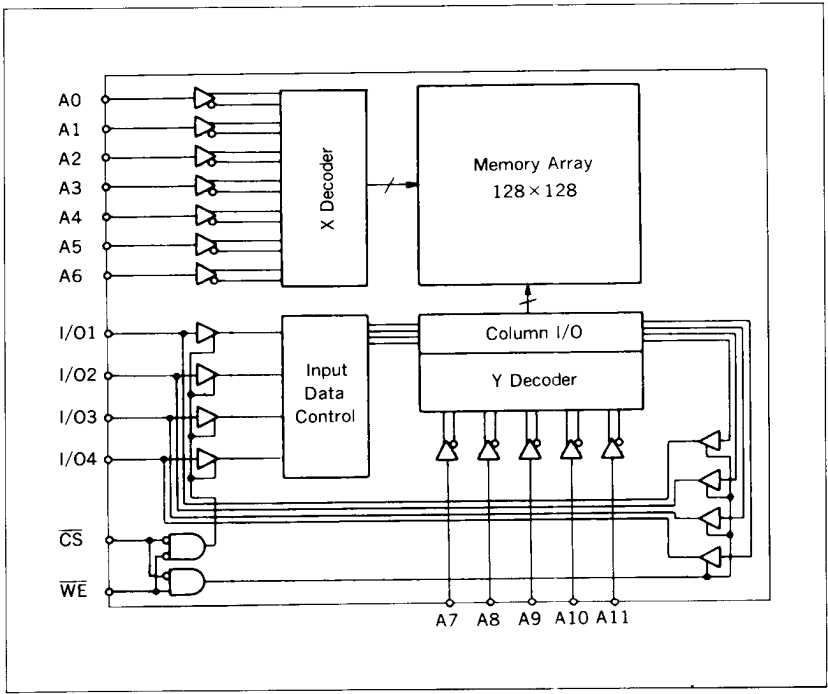
## DESCRIPTION

The SRM2268C<sub>45/55/70</sub> is a 4,096 words × 4 bits asynchronous, static, random access memory on a monolithic CMOS chip. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

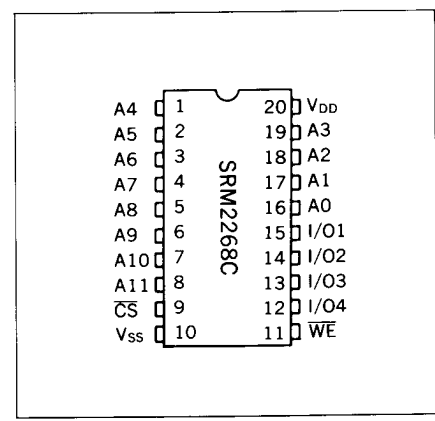
## FEATURES

- Fast access time ..... SRM2268C<sub>45</sub> 45ns (Max)  
SRM2268C<sub>55</sub> 55ns (Max)  
SRM2268C<sub>70</sub> 70ns (Max)
- Low supply current ..... Standby : 20μA (Typ)  
Operation : 40mA (Typ)
- Completely static
- Single power supply ..... 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Package ..... 20-pin DIP (plastic)

## BLOCK DIAGRAM



## PIN CONFIGURATION



## PIN DESCRIPTION

|              |                   |
|--------------|-------------------|
| A0 to A11    | Address Input     |
| WE           | Write Enable      |
| CS           | Chip Select       |
| I/O1 to I/O4 | Data Input/Output |
| VDD          | Power Supply (5V) |
| VSS          | Power Supply (0V) |

## ■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

| Parameter              | Symbol            | Ratings     | Unit |
|------------------------|-------------------|-------------|------|
| Supply voltage         | V <sub>DD</sub>   | -3.5 to 7.0 | V    |
| Input voltage*         | V <sub>I</sub>    | -3.5 to 7.0 | V    |
| Output voltage*        | V <sub>O</sub>    | -3.5 to 7.0 | V    |
| Power dissipation      | P <sub>D</sub>    | 1.0         | W    |
| Operating temperature  | T <sub>opr</sub>  | 0 to 70     | °C   |
| Storage temperature    | T <sub>stg</sub>  | -55 to 125  | °C   |
| Temperature under bias | T <sub>bias</sub> | -10 to 85   | °C   |

\*Pulse Width 20ns, DC = -0.5V

## ■ DC RECOMMENDED OPERATING CONDITIONS

(T<sub>a</sub> = 0 to 70°C)

| Parameter      | Symbol          | Conditions | Min   | Typ | Max | Unit |
|----------------|-----------------|------------|-------|-----|-----|------|
| Supply voltage | V <sub>DD</sub> | —          | 4.5   | 5.0 | 5.5 | V    |
|                | V <sub>SS</sub> | —          | —     | 0   | —   | V    |
| Input voltage  | V <sub>IH</sub> | —          | 2.2   | —   | 6.0 | V    |
|                | V <sub>IL</sub> | —          | -3.0* | —   | 0.8 | V    |

\*Pulse width 20ns, DC: V<sub>IL</sub> (Min) = -0.5V

## ■ ELECTRICAL CHARACTERISTICS

### ● DC Electrical Characteristics

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

| Parameter                 | Symbol            | Conditions   | Min  | Typ*1 | Max | Unit |
|---------------------------|-------------------|--|------|-------|-----|------|
| Input leakage current     | I <sub>LI</sub>   | V <sub>DD</sub> = 5.5V, V <sub>I</sub> = V <sub>SS</sub> to V <sub>DD</sub>                              | -2.0 | —     | 2.0 | μA   |
| Standby supply current    | I <sub>DDS</sub>  | $\overline{CS} = V_{IH}$   | —    | 15    | 25  | mA   |
|                           | I <sub>DDS1</sub> | $\overline{CS} \geq V_{DD} - 0.2V$ ,<br>V <sub>I</sub> ≤ 0.2V or V <sub>I</sub> ≥ V <sub>DD</sub> - 0.2V | —    | 0.02  | 2.0 | mA   |
| Operating supply current  | I <sub>DDO</sub>  | $\overline{CS} = V_{IL}$ , I <sub>I/O</sub> = 0mA  | —    | 40    | 90  | mA   |
| Output leakage current    | I <sub>LO</sub>   | $\overline{CS} = V_{IH}$ , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>DD</sub>                         | -2.0 | —     | 2.0 | μA   |
| High level output voltage | V <sub>OH</sub>   | I <sub>OH</sub> = -4.0mA   | 2.4  | —     | —   | V    |
| Low level output voltage  | V <sub>OL</sub>   | I <sub>OL</sub> = 8.0mA  | —    | —     | 0.4 | V    |

\*1 Typical values are for T<sub>a</sub> = 25°C and V<sub>DD</sub> = 5.0V

### ● Terminal Capacitance \*2

(f = 1.0MHz, T<sub>a</sub> = 25°C)

| Parameter          | Symbol         | Conditions          | Min | Typ | Max | Unit |
|--------------------|----------------|---------------------|-----|-----|-----|------|
| Input capacitance  | C <sub>I</sub> | V <sub>I</sub> = 0V | —   | —   | 6   | pF   |
| Output capacitance | C <sub>O</sub> | V <sub>O</sub> = 0V | —   | —   | 8   | pF   |

\*2 This parameter is sampled and not 100% tested.

### ● AC Electrical Characteristics

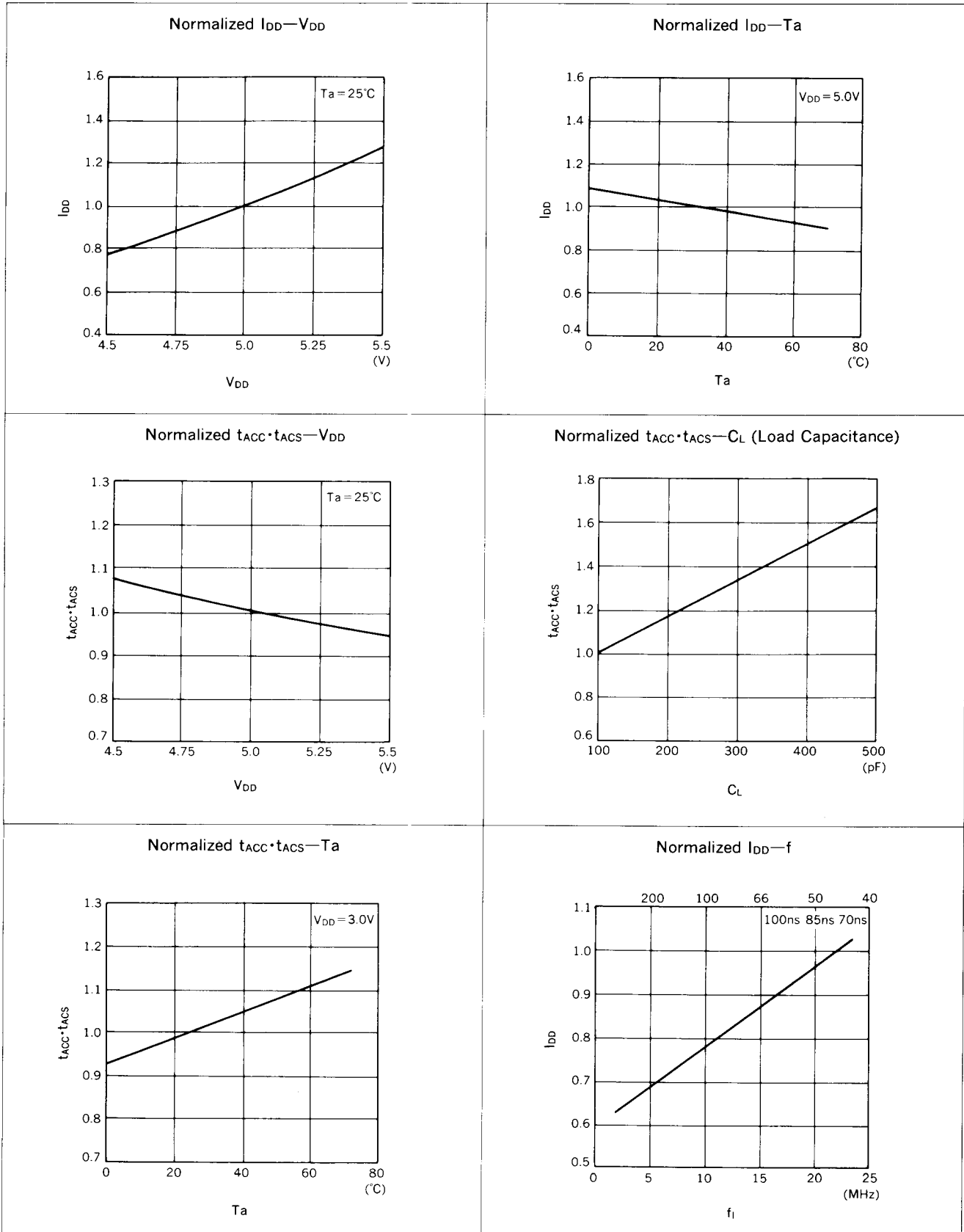
#### ○ Read Cycle

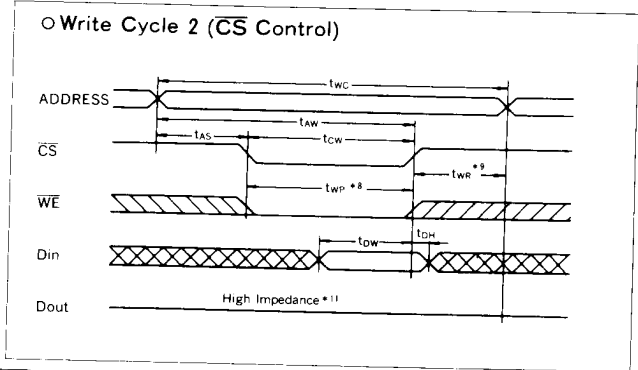
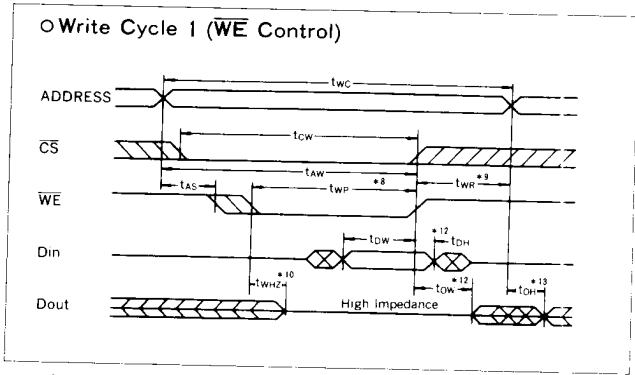
(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

| Parameter                         | Symbol           | SRM2268C <sub>45</sub> |     | SRM2268C <sub>55</sub> |     | SRM2268C <sub>70</sub> |     | Unit |
|-----------------------------------|------------------|------------------------|-----|------------------------|-----|------------------------|-----|------|
|                                   |                  | Min                    | Max | Min                    | Max | Min                    | Max |      |
| Read cycle time                   | t <sub>RC</sub>  | 45                     | —   | 55                     | —   | 70                     | —   | ns   |
| Address access time               | t <sub>ACC</sub> | —                      | 45  | —                      | 55  | —                      | 70  | ns   |
| $\overline{CS}$ access time       | t <sub>ACS</sub> | —                      | 45  | —                      | 55  | —                      | 70  | ns   |
| $\overline{CS}$ output set time*3 | t <sub>CLZ</sub> | 20                     | —   | 20                     | —   | 20                     | —   | ns   |
| $\overline{CS}$ output floating*3 | t <sub>CHZ</sub> | 0                      | 20  | 0                      | 20  | 0                      | 20  | ns   |
| $\overline{CS}$ power up time     | t <sub>PU</sub>  | 0                      | —   | 0                      | —   | 0                      | —   | ns   |
| $\overline{CS}$ power down time   | t <sub>PD</sub>  | —                      | 30  | —                      | 30  | —                      | 30  | ns   |
| Output hold time                  | t <sub>OH</sub>  | 5                      | —   | 5                      | —   | 5                      | —   | ns   |

\*3 Transition is measured ±500mV for high impedance voltage with Load B.  
This parameter is sampled and not 100% tested.

## CHARACTERISTICS CURVES





- \*8 A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ , ( $t_{WP}$ )
- \*9  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
- \*10 During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- \*11 If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output buffer buffers remain in a high impedance state.
- \*12 If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
- \*13 Dout is the same phase of Write data of this write cycle.

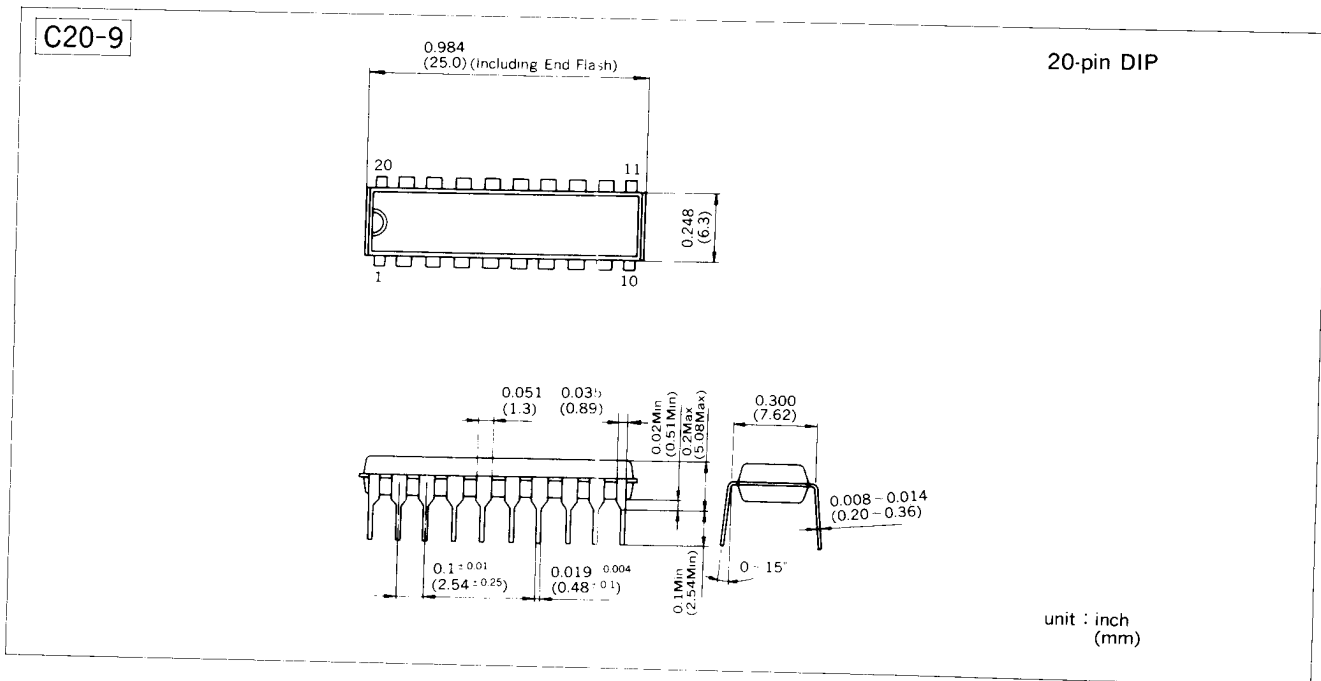
## FUNCTIONS

### Truth Table

| $\overline{CS}$ | $\overline{WE}$ | A0 to A11 | Data I/O    | Mode       | $I_{DD}$            |
|-----------------|-----------------|-----------|-------------|------------|---------------------|
| H               | X               | —         | Hi-Z        | Unselected | $I_{DDS}, I_{DDS1}$ |
| L               | H               | Stable    | Output data | Read       | $I_{DDO}$           |
| L               | L               | Stable    | Input data  | Write      | $I_{DDO}$           |

X: "H" or "L", —: "H", "L" or "Hi-Z"

## PACKAGE DIMENSIONS



○ Write Cycle

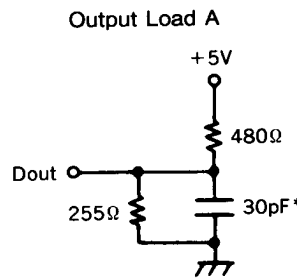
( $V_{DD}=5V \pm 10\%$ ,  $V_{SS}=0V$ ,  $T_a=0$  to  $70^\circ C$ )

| Parameter                                       | Symbol    | SRM2268C <sub>45</sub> |     | SRM2268C <sub>55</sub> |     | SRM2268C <sub>70</sub> |     | Unit |
|---|-----------|------------------------|-----|------------------------|-----|------------------------|-----|------|
|   |           | Min                    | Max | Min                    | Max | Min                    | Max |      |
| Write cycle time                                | $t_{WC}$  | 45                     | —   | 55                     | —   | 70                     | —   | ns   |
| Chip select time ( $\overline{CS}$ )            | $t_{CW}$  | 40                     | —   | 50                     | —   | 60                     | —   | ns   |
| Address enable time                             | $t_{AW}$  | 40                     | —   | 50                     | —   | 60                     | —   | ns   |
| Address setup time                              | $t_{AS}$  | 0                      | —   | 0                      | —   | 0                      | —   | ns   |
| Write pulse width                               | $t_{WP}$  | 35                     | —   | 45                     | —   | 55                     | —   | ns   |
| Address hold time                               | $t_{WR}$  | 0                      | —   | 0                      | —   | 0                      | —   | ns   |
| Input data setup time                           | $t_{DW}$  | 20                     | —   | 25                     | —   | 30                     | —   | ns   |
| Input data hold time                            | $t_{DH}$  | 0                      | —   | 0                      | —   | 0                      | —   | ns   |
| $\overline{WE}$ output floating* <sup>4</sup>   | $t_{WHZ}$ | 0                      | 15  | 0                      | 20  | 0                      | 25  | ns   |
| $\overline{WE}$ output setup time* <sup>4</sup> | $t_{OW}$  | 0                      | —   | 0                      | —   | 0                      | —   | ns   |

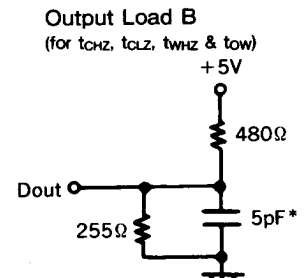
\*4 Transition is measured  $\pm 500mV$  from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

○ Test Conditions

1. Input pulse levels :  $V_{SS}$  to 3.0V
2. Input rise and fall times : 5 ns
3. Input timing reference levels : 1.5V
4. Output reference levels : 1.5V
5. Output load : see figure

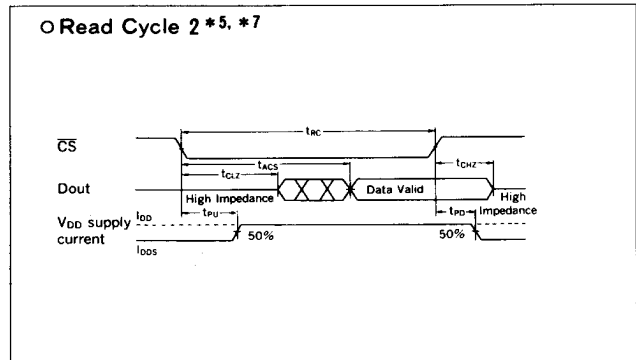
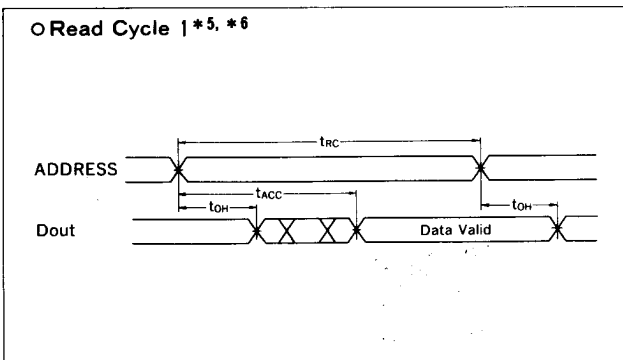


\* Including scope and jig.



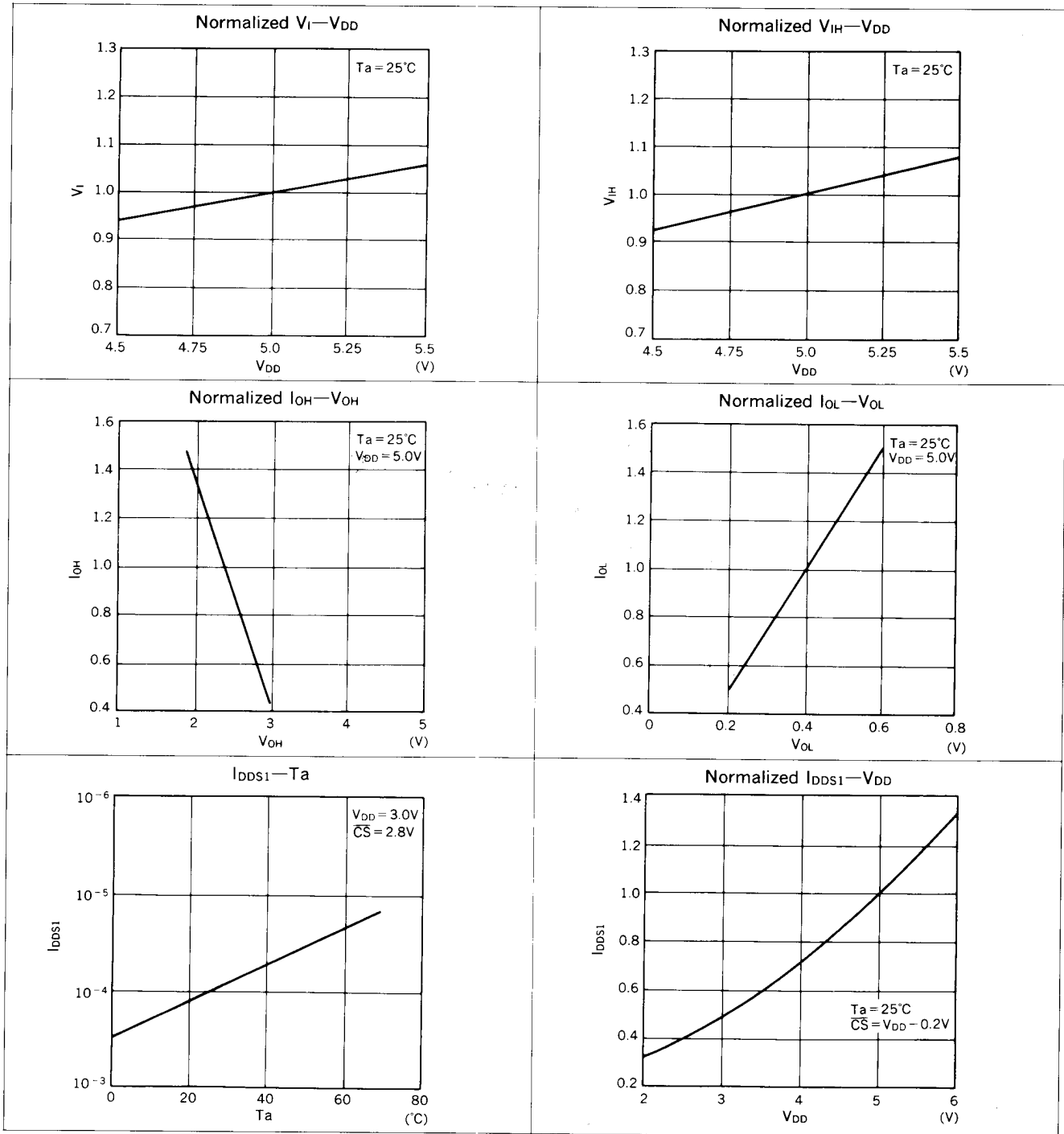
\* Including scope and jig.

● Timing Chart



- \*5  $\overline{WE}$  is High for Read Cycle.
- \*6 Device is continuously selected,  $\overline{CS}=V_{IL}$ .
- \*7 Addresses valid prior to or coincident with  $\overline{CS}$  transition low.

## CHARACTERISTICS CURVES (Continued)



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