

# SN54LS651 THRU SN54LS653 SN74LS651 THRU SN74LS653 OCTAL BUS TRANSCIEVERS AND REGISTERS

SDLS191A – JANUARY 1981 – REVISED DECEMBER 2000

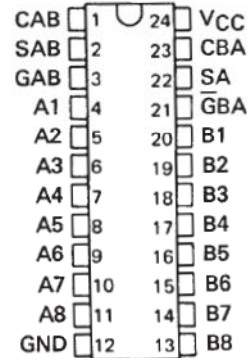
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Dependable Texas Instruments Quality and Reliability

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'LS651	3-State	3-State	Inverting
'LS652	3-State	3-State	True
'LS653	Open-collector	3-State	Inverting

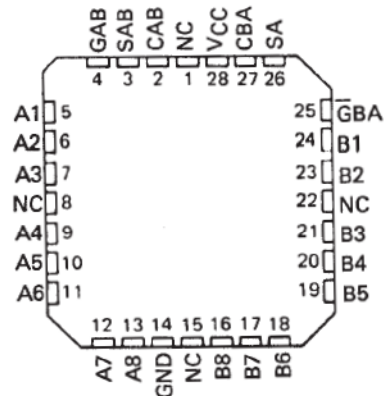
## description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and  $\bar{G}BA$  are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether realtime or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS651, 'LS652, and 'LS653.

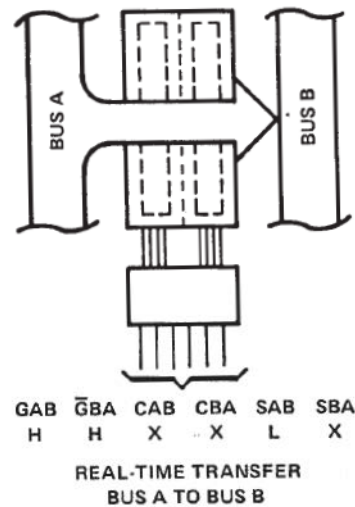
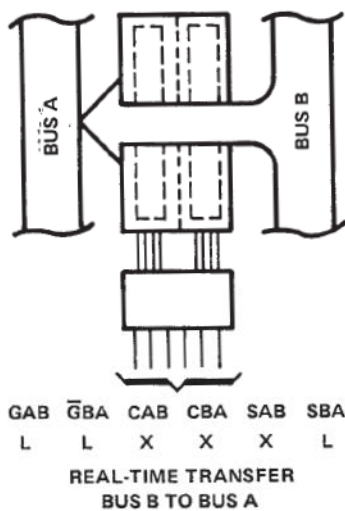
SN54LS' . . . JT PACKAGE  
SN74LS' . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54LS' . . . FK PACKAGE  
(TOP VIEW)



NC — No internal connection



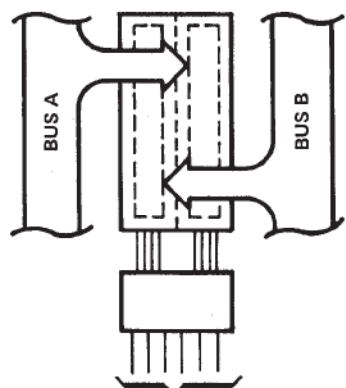
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

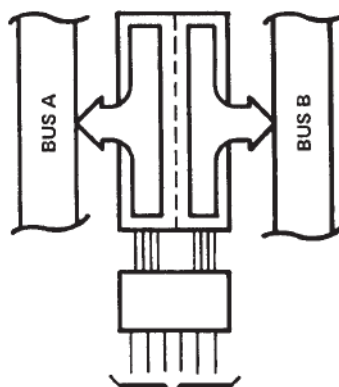
Copyright © 2000, Texas Instruments Incorporated

**SN54LS651 THRU SN54LS653**  
**SN74LS651 THRU SN74LS653**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS**  
 SDLS191A – JANUARY 1981 – REVISED DECEMBER 2000



GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM  
A AND/OR B



GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER  
STORED DATA  
TO A AND/OR B

Data on the A or B data bus, or both, can be stored in the internal D flip-flop by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB or SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and  $\overline{\text{GBA}}$ . In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54LS651 through SN54LS653 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS651 through SN74LS653 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

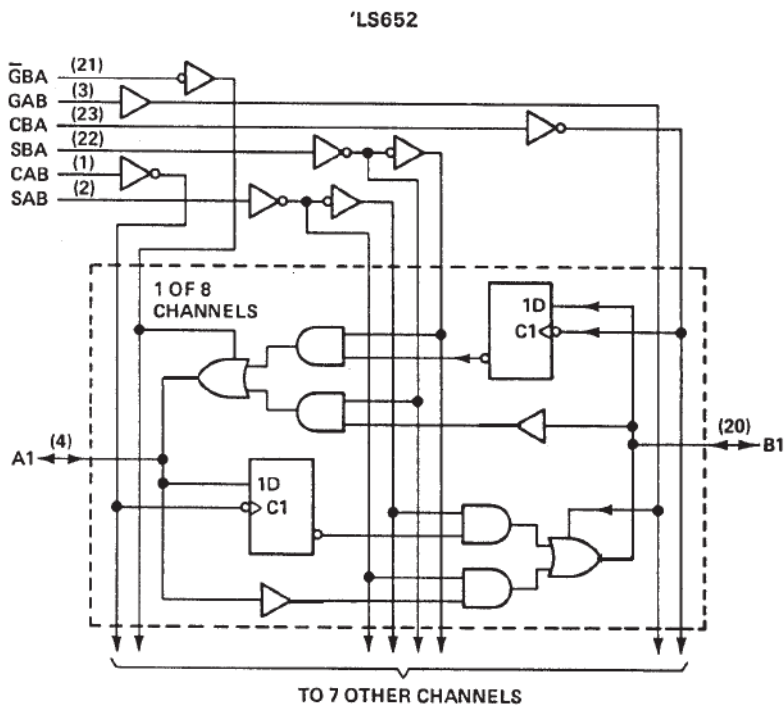
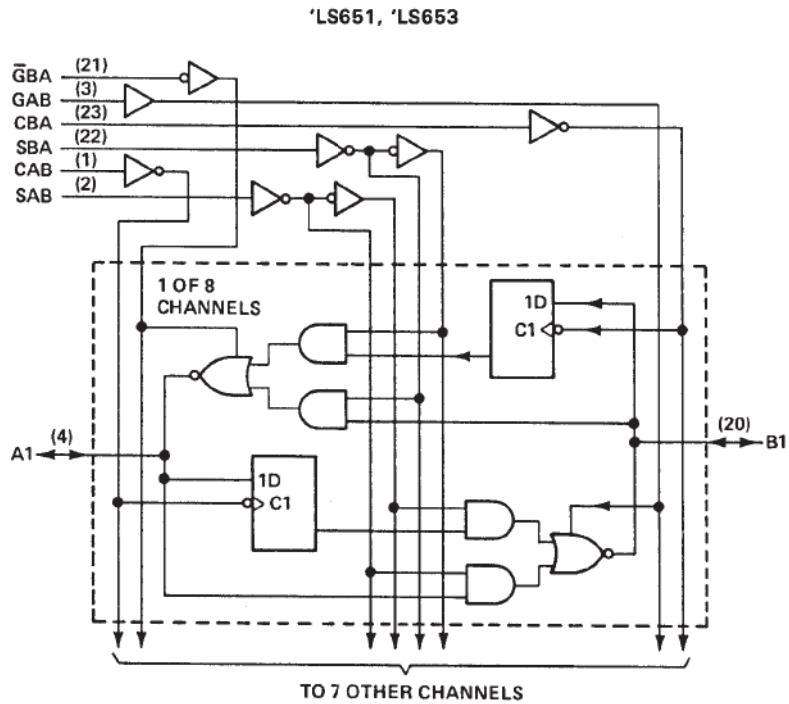
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS651, 'LS653	'LS652, 'LS654
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{\text{B}}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{\text{B}}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{\text{A}}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{\text{A}}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{\text{A}}$ Data to B Bus and Stored $\overline{\text{B}}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

\* The data output functions may be enabled or disabled by various signals at the GAB and  $\overline{\text{GBA}}$  inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

**SN54LS651 THRU SN54LS653**  
**SN74LS651 THRU SN74LS653**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS**  
SDLS191A – JANUARY 1981 – REVISED DECEMBER 2000

logic diagrams (positive logic)

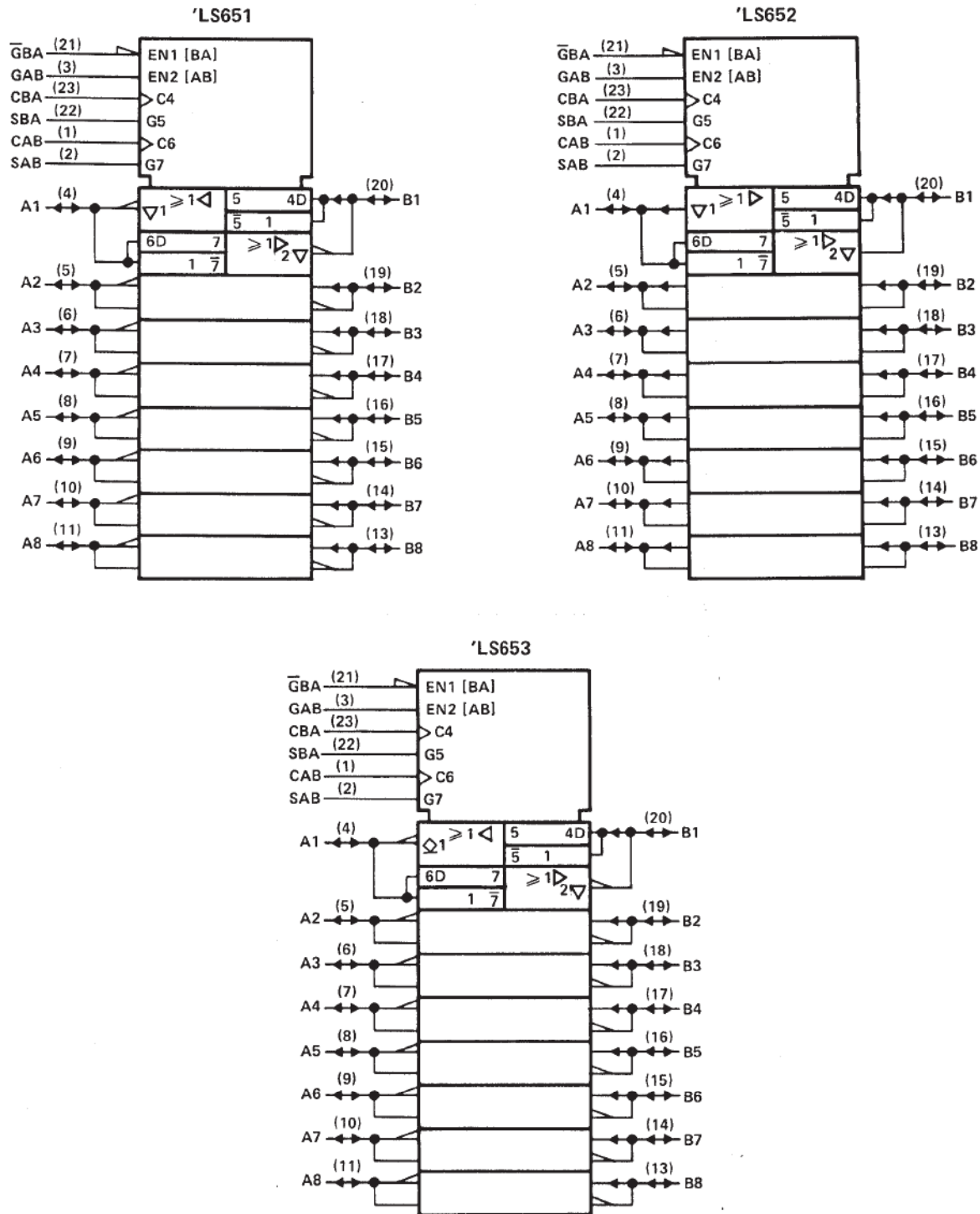


Pin numbers shown are for DW, JT or NT packages.

**SN54LS651 THRU SN54LS653**  
**SN74LS651 THRU SN74LS653**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS**

SDLS191A – JANUARY 1981 – REVISED DECEMBER 2000

logic symbols†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, or NT packages.

# SN54LS651, SN54LS652, SN74LS651, SN74LS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS191 – JANUARY 1981 – REVISED MARCH 1988

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ .....	7 V
Input voltage: Control inputs .....	7 V
I/O ports .....	5.5 V
Operating free-air temperature range: SN54LS651, SN54LS652 .....	– 55°C to 125°C
SN74LS651, SN74LS652 .....	0°C to 70°C
Storage temperature range .....	– 65°C to 150°C

## recommended operating conditions

		SN54LS651 SN54LS652			SN74LS651 SN74LS652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage				0.7			V
$I_{OH}$	High-level output current				– 12			mA
$I_{OL}$	Low-level output current				12			mA
$t_w$	Pulse duration	CBA or CAB high		15	15		ns	
		CBA or CAB low		15	15			
		Data high or low		15	15			
$t_{su}$	Setup time before CAB ↑ or CBA ↑	A or B		15	15		ns	
$t_h$	Hold time after CAB ↑ or CBA ↑	A or B		0	0		ns	
$T_A$	Operating free-air temperature	– 55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS651 SN54LS652		SN74LS651 SN74LS652		UNIT
				MIN	TYP‡	MAX	MIN	
$V_{IK}$		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		– 1.5		– 1.5		V
$V_{OH}$		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OH} = -3 \text{ mA}$	2.4	3.4	2.4	3.4	V
			$I_{OH} = -12 \text{ mA}$	2				
			$I_{OH} = -15 \text{ mA}$			2		
$V_{OL}$		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4	V
			$I_{OL} = 24 \text{ mA}$			0.35 0.5		
$I_I$	Control inputs	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$	0.1		0.1		mA	
	A or B ports	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	0.1		0.1			
$I_{IH}$	Control inputs	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20		20		µA	
	A or B ports†		20		20			
$I_{IL}$	Control inputs	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	– 0.4		– 0.4		mA	
	A or B ports†		– 0.4		– 0.4			
$I_{OS}§$		$V_{CC} = \text{MAX}, V_O = 0 \text{ V}$	– 40	– 225	– 40	– 225	mA	
$I_{CC}$	LS651	$V_{CC} = \text{MAX}$	Outputs high	95	145	95	145	mA
			Outputs low	103	165	103	165	
			Outputs disabled	103	165	103	165	
	LS652		Outputs high	95	145	95	145	
			Outputs low	103	165	103	165	
			Outputs disabled	120	180	120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

† For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.



# SN54LS651, SN54LS652, SN74LS651, SN74LS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS191 – JANUARY 1981 – REVISED MARCH 1988

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS651			'LS652			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$	Clock	Bus	$R_L = 667\ \Omega$ , $C_L = 45\ \text{pF}$ , See Note 2	14	24		15	25	ns	
$t_{PHL}$				23	35		24	36	ns	
$t_{PLH}$	Bus	Bus		9	18		12	18	ns	
$t_{PHL}$				20	30		13	20	ns	
$t_{PLH}$	Select, with bus input high†	Bus		31	47		23	35	ns	
$t_{PHL}$				22	33		21	32	ns	
$t_{PLH}$	Select, with bus input low†	Bus		23	35		33	50	ns	
$t_{PHL}$				19	30		15	23	ns	
$t_{PZH}$	$\overline{\text{G}}\text{BA}$	A Bus		29	44		30	45	ns	
$t_{PZL}$				40	60		36	54	ns	
$t_{PZH}$	GAB	B Bus		19	29		20	30	ns	
$t_{PZL}$				26	40		25	38	ns	
$t_{PHZ}$	$\overline{\text{G}}\text{BA}$	A Bus	25	38		25	38	ns		
$t_{PLZ}$			19	30		19	30	ns		
$t_{PHZ}$	GAB	B Bus	25	38		25	38	ns		
$t_{PLZ}$			19	30		19	30	ns		

$t_{PLH}$  = propagation delay time, low-to-high-level output.

$t_{PHL}$  = propagation delay time, high-to-low-level output

$t_{PZH}$  = output enable time to high level

$t_{PZL}$  = output enable time to low level

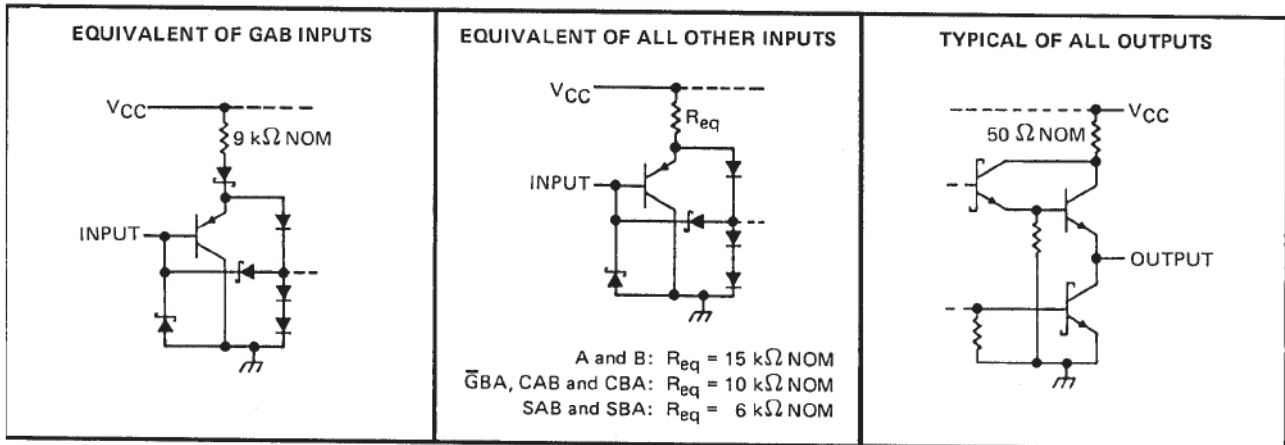
$t_{PHZ}$  = output disable time from high level

$t_{PLZ}$  = output disable time from low level

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## schematics of inputs and outputs



# SN54LS653, SN74LS653 OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS191 – JANUARY 1981 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ .....	7 V
Input voltage: All inputs and A I/O ports .....	7 V
B I/O ports .....	5.5 V
Operating free-air temperature range: SN54LS653 .....	–55 °C to 125 °C
SN74LS653 .....	0 °C to 70 °C
Storage temperature range .....	–65 °C to 150 °C

**recommended operating conditions**

		SN54LS653			SN74LS653			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
$V_{IH}$	High-level input voltage	2			2			V		
$V_{IL}$	Low-level input voltage				0.8			V		
$V_{OH}$	High-level output voltage	A ports			5.5			V		
$I_{OH}$	High-level output current	B ports			–12			mA		
$I_{OL}$	Low-level output current				12			mA		
$t_w$	Pulse duration	CBA or CAB high			15			ns		
		CBA or CAB low			30					
		Data high or low			30					
$t_{su}$	Setup time before CAB $\uparrow$ or CBA $\uparrow$	A or B			15			ns		
$t_h$	Hold time after CAB $\uparrow$ or CBA $\uparrow$	A or B			0			ns		
$T_A$	Operating free-air temperature	–55			125			0	70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS <sup>†</sup>		SN54LS653		SN74LS653		UNIT	
				MIN	TYP <sup>‡</sup>	MAX	MIN		TYP <sup>‡</sup>
$V_{IK}$		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		–1.5		–1.5		V	
$V_{OH}$	B ports	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$		$I_{OH} = -3 \text{ mA}$	2.4	3.4	2.4	3.4	V
				$I_{OH} = -12 \text{ mA}$	2				
				$I_{OH} = -15 \text{ mA}$			2		
$I_{OH}$	A ports	$V_{CC} = \text{MIN}, V_{OH} = 5.5 \text{ V}$		0.1		0.1		mA	
$V_{OL}$		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$		$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4	V
				$I_{OL} = 24 \text{ mA}$			0.35		
$I_I$	Control inputs	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1		0.1		mA	
	A or B ports <sup>¶</sup>	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		0.1		0.1			
$I_{IH}$	Control inputs	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20		20		$\mu\text{A}$	
	A or B ports <sup>¶</sup>			20		20			
$I_{IL}$	Control inputs	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		–0.4		–0.4		mA	
	A or B ports <sup>¶</sup>			–0.4		–0.4			
$I_{OS}$ <sup>§</sup>	B ports	$V_{CC} = \text{MAX}, V_O = 0 \text{ V}$		–40	–225	–40	–225	mA	
$I_{CC}$	LS653	$V_{CC} = \text{MAX}$		Outputs high	95	145	95	145	mA
				Outputs low	103	165	103	165	
				Outputs disabled	103	165	103	165	
				Outputs high	95	145	95	145	
				Outputs low	105	170	105	170	
				Outputs disabled	120	180	120	180	
	LS654								

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

<sup>¶</sup> For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.



# SN54LS653, SN74LS653 OCTAL BUS TRANSCEIVERS AND REGISTERS

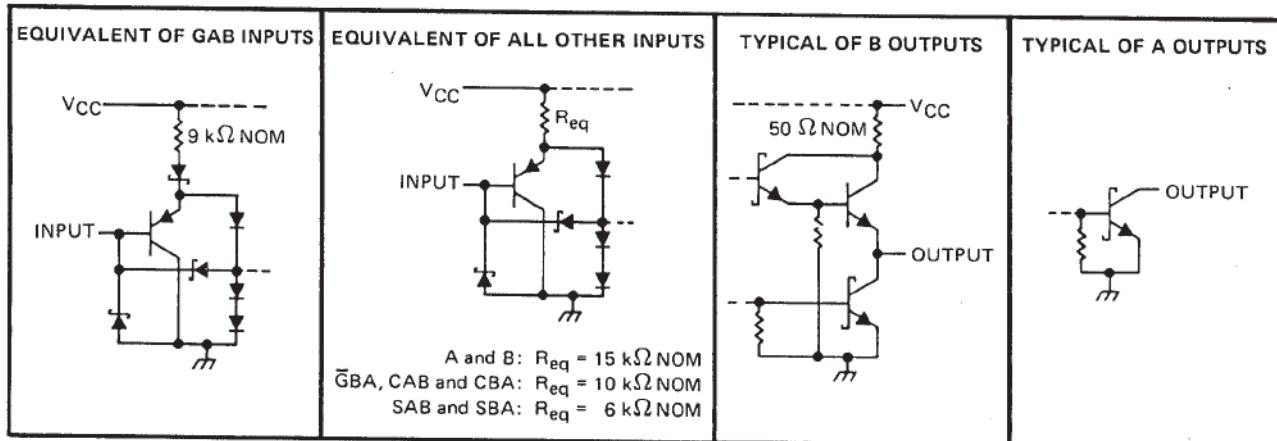
SDLS191 – JANUARY 1981 – REVISED MARCH 1988

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	CBA	A Bus	$R_L = 667\ \Omega$ , $C_L = 45\ \text{pF}$ , See Note 2		25	38	ns
$t_{PHL}$				26	39		
$t_{PLH}$	CAB	B Bus			15	23	ns
$t_{PHL}$				24	36		
$t_{PLH}$	A Bus	B Bus			10	18	ns
$t_{PHL}$				20	30		
$t_{PLH}$	B Bus	A Bus			21	32	ns
$t_{PHL}$				16	24		
$t_{PLH}$	SBA <sup>†</sup> (with B high)	A Bus			38	57	ns
$t_{PHL}$				26	39		
$t_{PLH}$	SBA <sup>†</sup> (with B low)	A Bus			34	51	ns
$t_{PHL}$				23	35		
$t_{PLH}$	SAB <sup>†</sup> (with A high)	B Bus			32	48	ns
$t_{PHL}$				22	33		
$t_{PLH}$	SAB <sup>†</sup> (with A low)	B Bus			24	36	ns
$t_{PHL}$				20	30		
$t_{PLH}$	$\overline{\text{G}}\text{BA}$	A Bus		23	35	ns	
$t_{PHL}$			37	55			
$t_{PZH}$	GAB	B Bus	$R_L = 667\ \Omega$ , $C_L = 5\ \text{pF}$ , See Note 2	19	29	ns	
$t_{PZL}$				25	38		
$t_{PHZ}$	GAB	B Bus		26	39	ns	
$t_{PLZ}$				19	29		

<sup>†</sup>These parameters are measured with the internal output state of the storage register opposite to that of the bus input.  
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## schematics of inputs and outputs



## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.