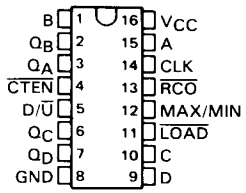
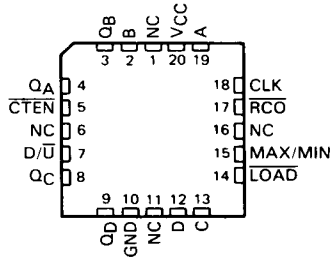
D2684, DECEMBER 1982 – REVISED JUNE 1989

- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable with Load Control**
- **Package Options: Plastic and Ceramic DIPs, Plastic Small-Outline Packages, and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC190, SN54HC191 . . . J PACKAGE
SN74HC190, SN74HC191 . . . D† OR N PACKAGE
(TOP VIEW)



SN54HC190, SN54HC191 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

†Contact the factory for D availability.

description

The 'HC190 and 'HC191 are synchronous, reversible up/down counters. The 'HC190 is a 4-bit decade counter, and the 'HC191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up ($D/\overline{U}$) input. When $D/\overline{U}$ is low, the counter counts up, and when $D/\overline{U}$ is high, it counts down.

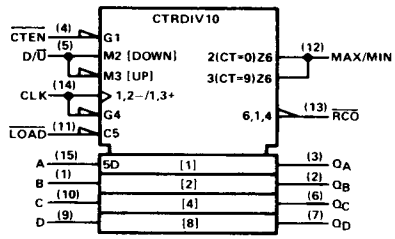
These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and $D/\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

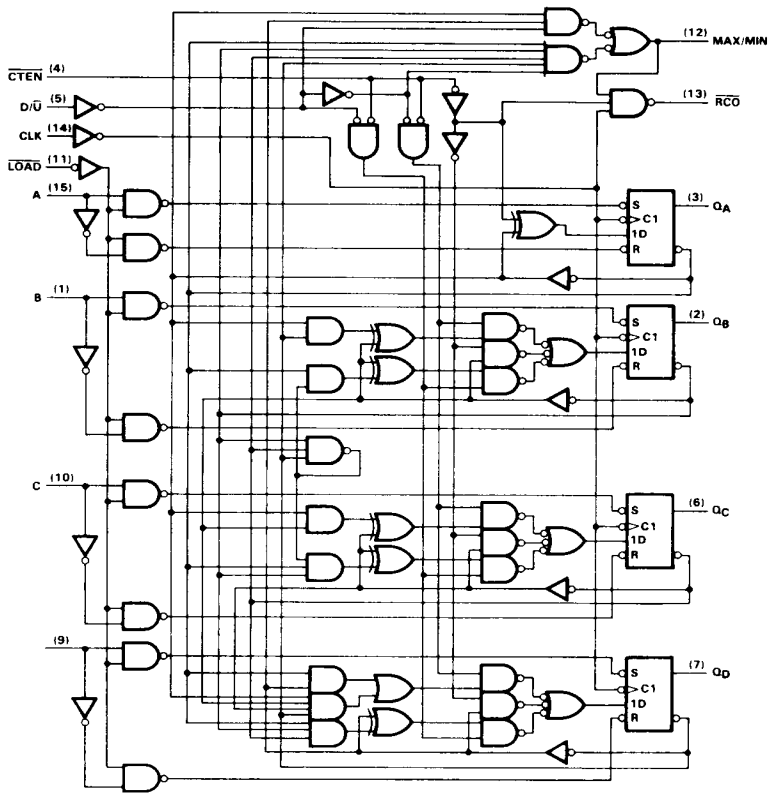
The SN54HC190 and SN54HC191 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC190 and SN74HC191 are characterized for operation from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers are for D, J, and N packages.

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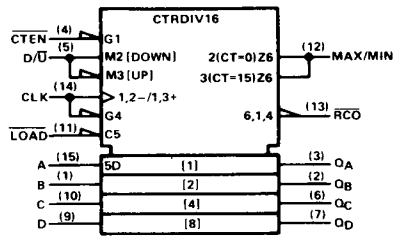
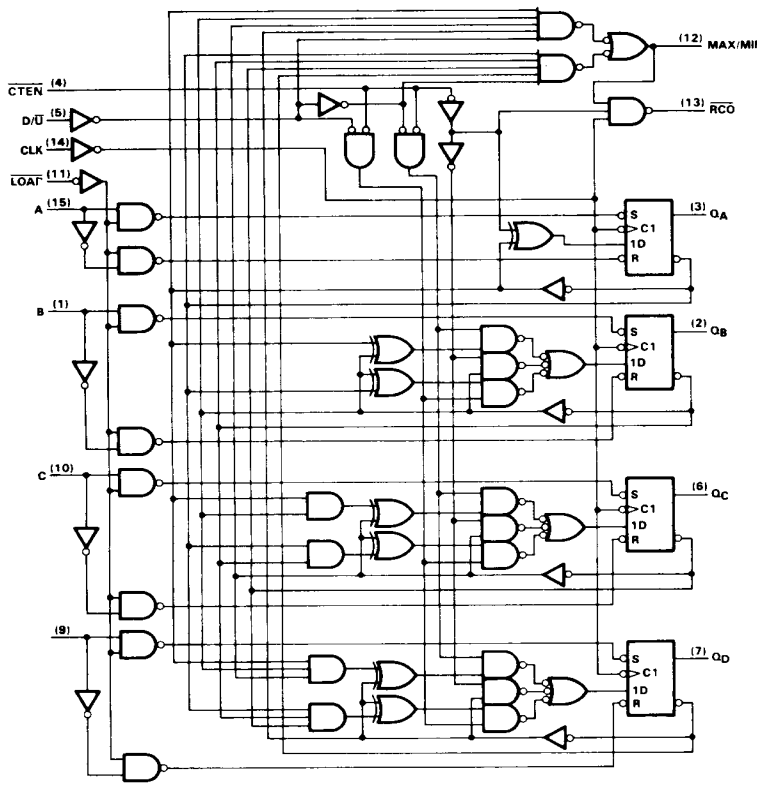
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

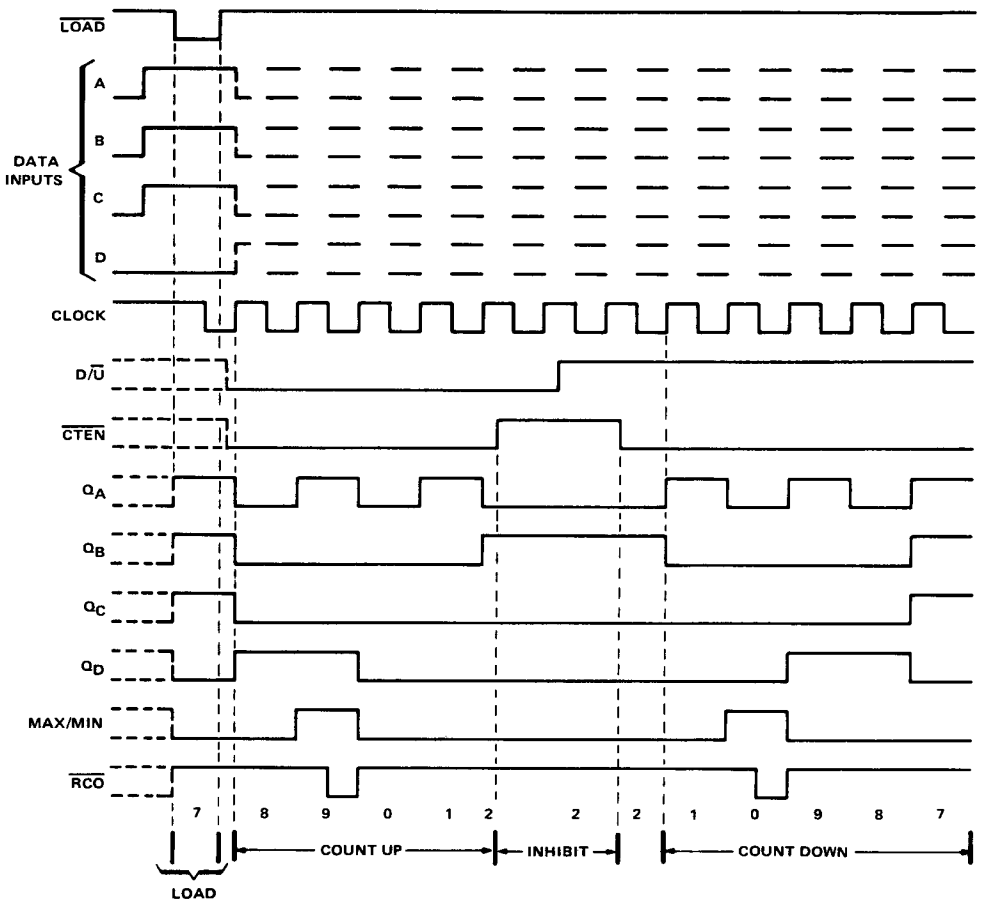


Pin numbers are for D, J, and N packages.

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven.



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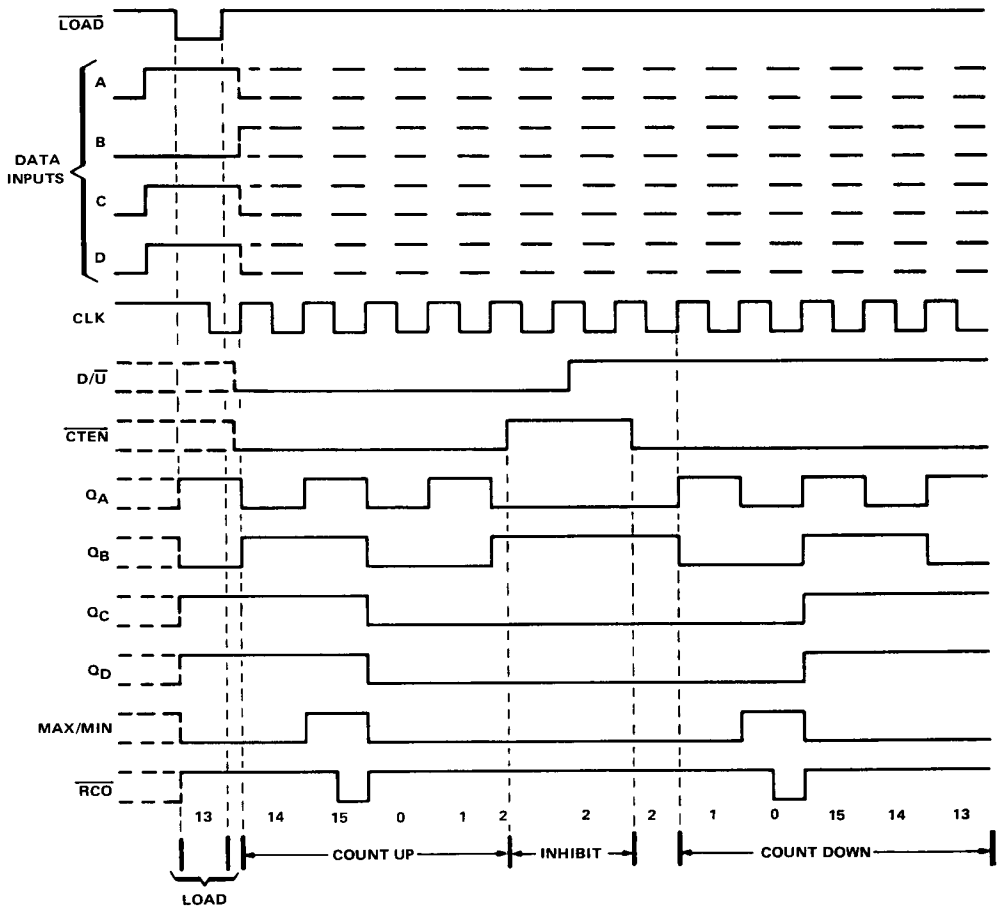
typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC190 SN54HC191			SN74HC190 SN74HC191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC190 SN54HC191		SN74HC190 SN74HC191		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC190 SN54HC191		SN74HC190 SN74HC191		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	4.2	0	2.8	0	3.3	MHz
			4.5 V	0	21	0	14	0	17	
			6 V	0	24	0	16	0	19	
t_w	Pulse duration	$\overline{LOAD}$ low	2 V	120		180		150		ns
			4.5 V	24		36		30		
			6 V	21		31		26		
		CLk high or low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
t_{su}	Setup time	Data before $\overline{LOAD}$↑	2 V	150		230		188		ns
			4.5 V	30		46		38		
			6 V	25		38		32		
		$\overline{CTEN}$ before CLK↑	2 V	205		306		255		
			4.5 V	41		61		51		
			6 V	35		53		44		
		D/$\overline{U}$ before CLK↑	2 V	205		306		255		
			4.5 V	41		61		51		
			6 V	35		53		44		
		$\overline{LOAD}$ inactive before CLK↑	2 V	150		225		190		
			4.5 V	30		45		38		
			6 V	25		38		32		
t_h	Hold time	Data after $\overline{LOAD}$↑	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		
		$\overline{CTEN}$ after CLK↑	2V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		
		D/$\overline{U}$ after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC190 SN54HC191		SN74HC190 SN74HC191		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	42		14		17		
			6 V	24	48		16		19		
t_{pd}	$\overline{LOAD}$	Any Q	2 V		130	264		396		330	ns
			4.5 V		40	53		79		66	
			6 V		33	45		67		56	
t_{pd}	A, B, C, or D	Q_A, Q_B Q_C, or Q_D	2 V		135	240		360		300	ns
			4.5 V		36	48		72		60	
			6 V		30	41		61		51	
t_{pd}	CLK	$\overline{RCO}$	2 V		58	120		180		150	ns
			4.5 V		17	24		36		30	
			6 V		14	21		31		26	
t_{pd}	CLK	Any Q	2 V		107	192		288		240	ns
			4.5 V		31	38		58		48	
			6 V		26	32		49		41	
t_{pd}	CLK	MAX/MIN	2 V		123	252		378		315	ns
			4.5 V		39	50		76		63	
			6 V		32	43		65		54	
t_{pd}	D/$\overline{U}$	$\overline{RCO}$	2 V		102	228		342		285	ns
			4.5 V		29	46		68		57	
			6 V		24	38		59		49	
t_{pd}	D/$\overline{U}$	MAX/MIN	2 V		86	192		288		240	ns
			4.5 V		24	38		58		48	
			6 V		20	32		49		41	
t_{pd}	$\overline{CTEN}$	$\overline{RCO}$	2 V		50	132		198		165	ns
			4.5 V		15	26		40		33	
			6 V		13	23		34		28	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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