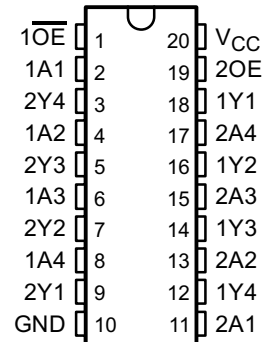


# SN54ABT241, SN74ABT241A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

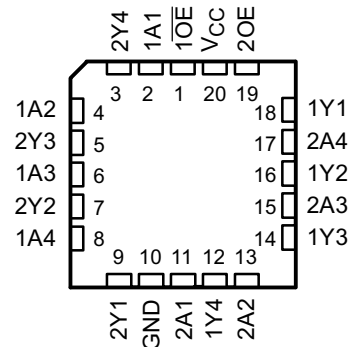
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- State-of-the-Art **EPIC-II<sup>TM</sup>** BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

SN54ABT241 . . . J OR W PACKAGE  
SN74ABT241A . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ABT241 . . . FK PACKAGE  
(TOP VIEW)



## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT240, SN74ABT240A, and 'ABT244A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ( $\overline{OE}$ ) inputs, and complementary OE and  $\overline{OE}$  inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT241 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT241A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-II<sup>B</sup> is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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## OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

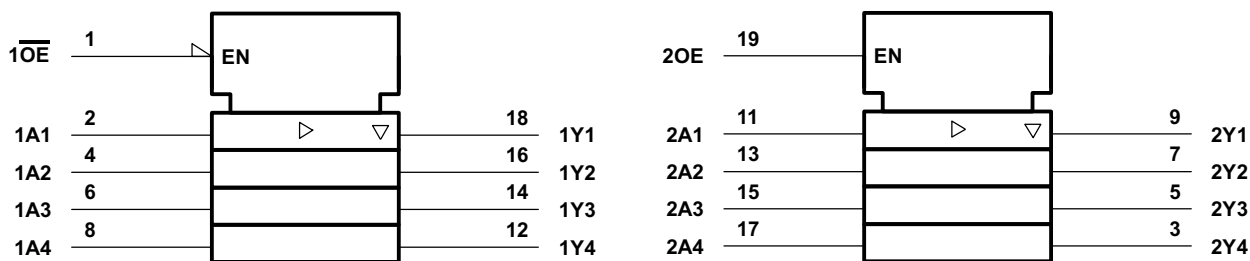
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## FUNCTION TABLES

INPUTS		OUTPUT 1Y
10E	1A	
L	H	H
L	L	L
H	X	Z

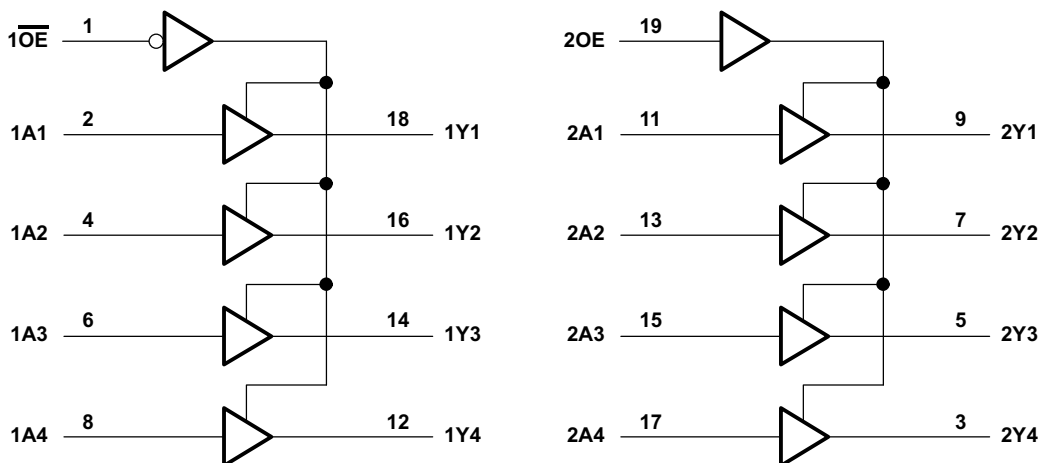
INPUTS		OUTPUT 2Y
2OE	2A	
H	H	H
H	L	L
L	X	Z

**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



# SN54ABT241, SN74ABT241A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT241	96 mA
SN74ABT241A	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

		SN54ABT241		SN74ABT241A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
	Outputs enabled					
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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# SN54ABT241, SN74ABT241A

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT241		SN74ABT241A		UNIT		
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA	–1.2			–1.2		–1.2		V		
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –3 mA	2.5			2.5		2.5		V		
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –3 mA	3			3		3				
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = –24 mA	2			2					
			I <sub>OH</sub> = –32 mA	2*					2			
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA	0.55			0.55		V			
			I <sub>OL</sub> = 64 mA	0.55*			0.55					
V <sub>hys</sub>			100							mV		
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	±1			±1		±1		μA		
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V	10			10		10		μA		
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V	–10			–10		–10		μA		
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V	±100					±100		μA		
I <sub>CEX</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50			50		μA	
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA		
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high			1		250		250		μA
			Outputs low			24		30		30		mA
			Outputs disabled			0.5		250		250		μA
ΔI <sub>CC</sub> §	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Outputs enabled			1.5		1.5		1.5		mA
			Outputs disabled			0.05		0.05		0.05		
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		1.5			1.5		1.5			
C <sub>i</sub>		V <sub>I</sub> = 2.5 V or 0.5 V		4							pF	
C <sub>o</sub>		V <sub>O</sub> = 2.5 V or 0.5 V		5.5							pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



# SN54ABT241, SN74ABT241A

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT241					UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	1	2.6	4.1	0.8	5.3	ns
t <sub>PHL</sub>			1	2.9	4.2	0.8	5	
t <sub>PZH</sub>	OE or OE	Y	1.1	4.8	6.3	1	7	ns
t <sub>PZL</sub>			1.3	4.3	5.8	1	7	
t <sub>PHZ</sub>	OE or OE	Y	1.1	4.6	6.1	0.8	7.9	ns
t <sub>PLZ</sub>			1	3.9	5.4	0.8	6.2	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

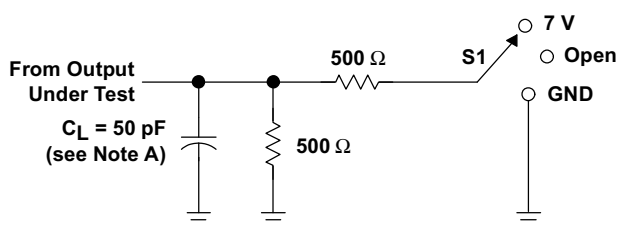
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT241A					UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	1	2.6	4.1	1	4.6	ns
t <sub>PHL</sub>			1	2.9	4.4	1	4.6	
t <sub>PZH</sub>	OE or OE	Y	1.1	4.8	6.3	1.1	6.8	ns
t <sub>PZL</sub>			1.3	4.3	5.8	1.3	6.8	
t <sub>PHZ</sub>	OE or OE	Y	1.6	4.6	6.1	1.6	7.1	ns
t <sub>PLZ</sub>			1	3.9	5.4	1	5.9	



# SN54ABT241, SN74ABT241A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

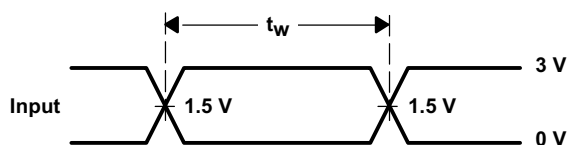
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## PARAMETER MEASUREMENT INFORMATION

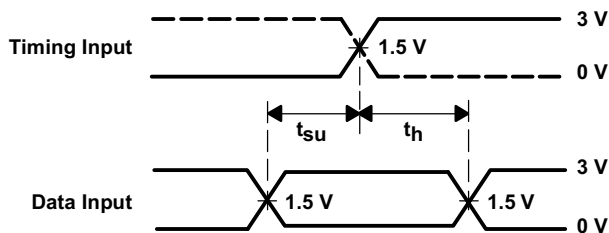


LOAD CIRCUIT

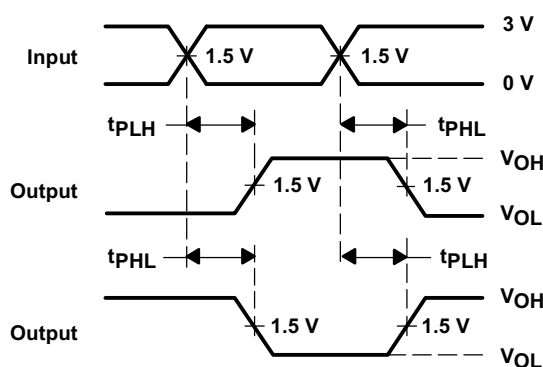
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



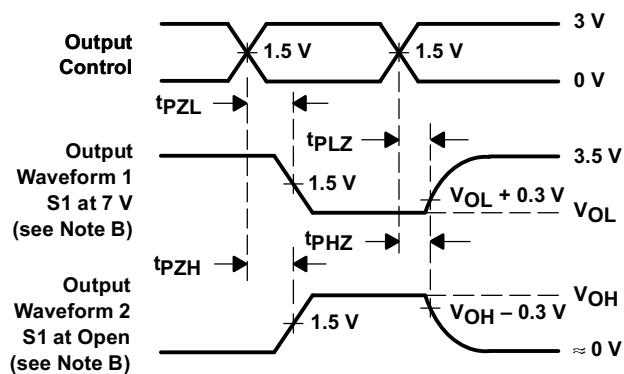
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9322701Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9322701QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9322701QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN74ABT241ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74ABT241ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT241ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT241APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74ABT241APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT241APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT241FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ABT241J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SNJ54ABT241W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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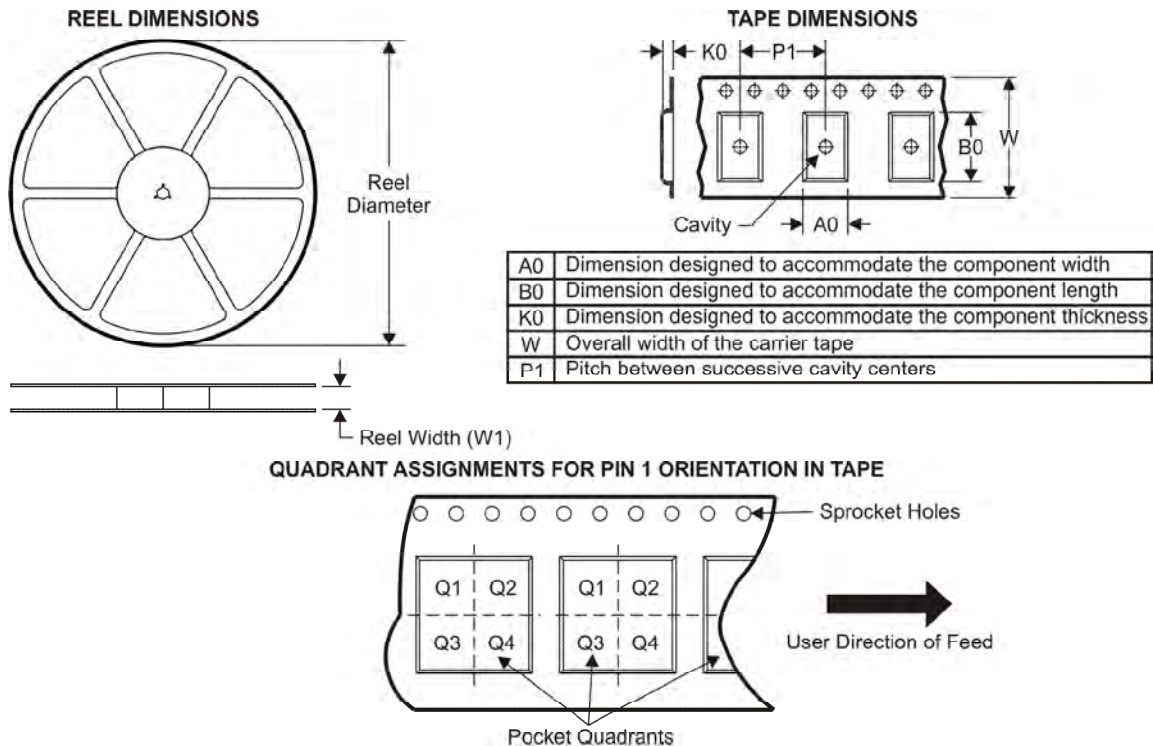
**OTHER QUALIFIED VERSIONS OF SN54ABT241 :**

- Catalog: [SN74ABT241](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

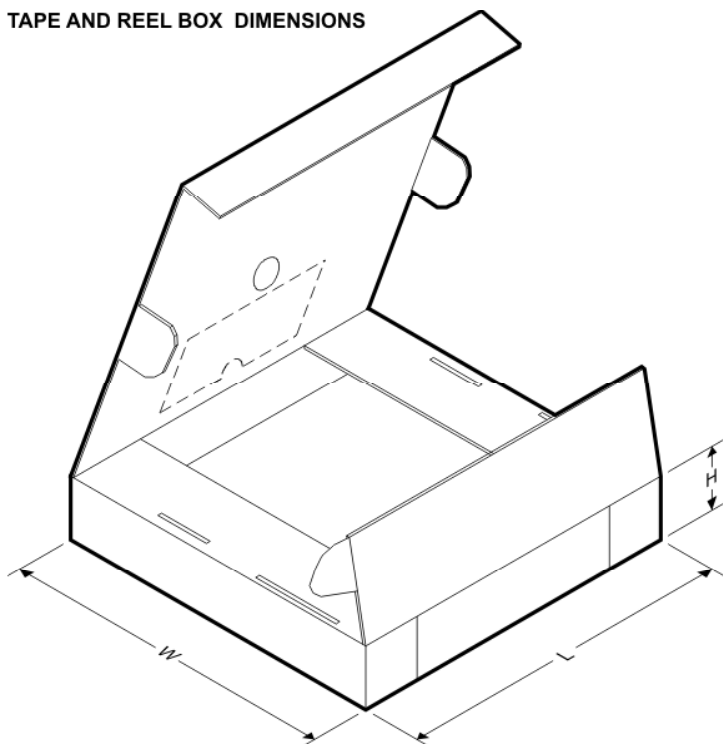
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT241ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT241ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ABT241APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



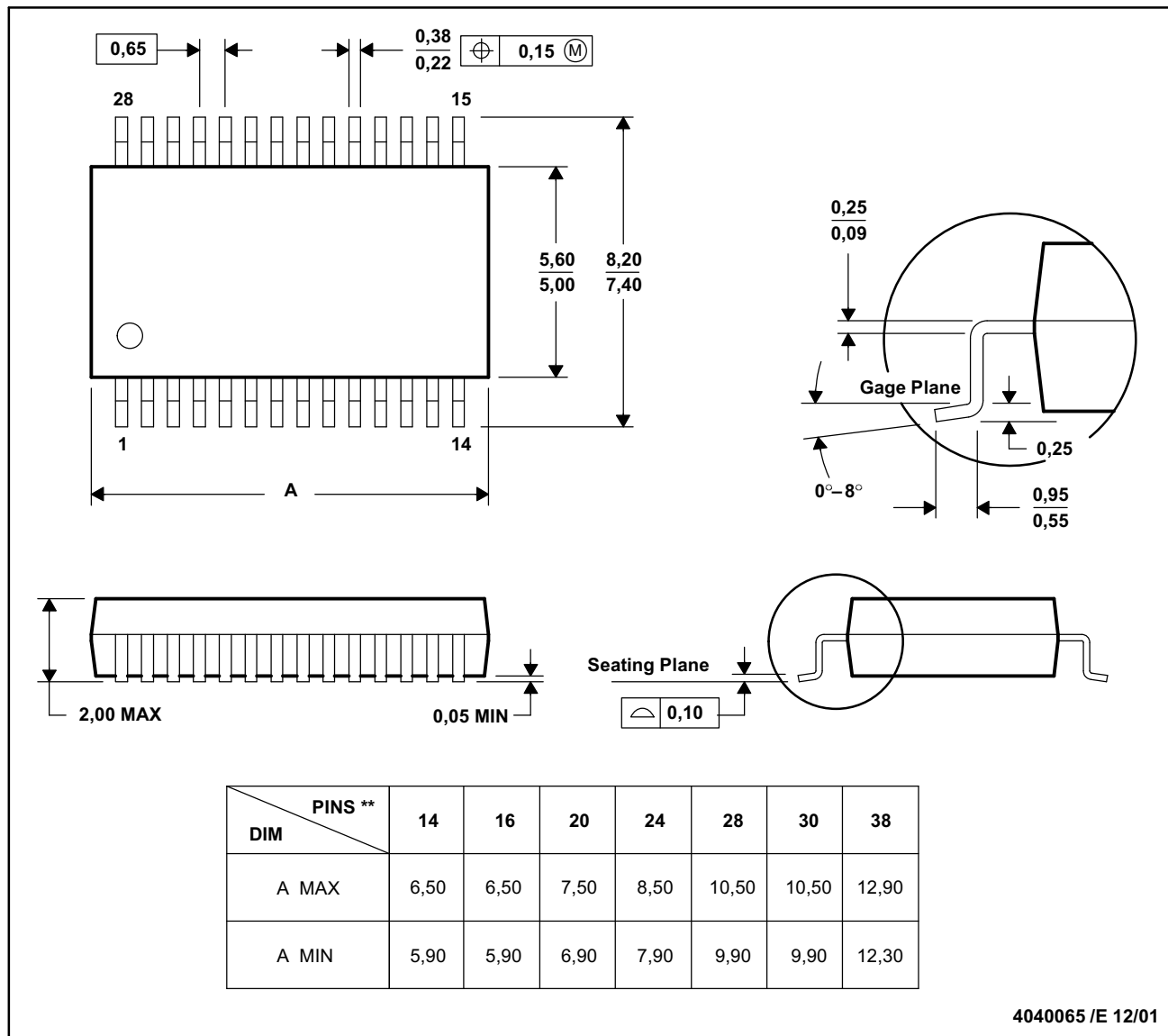
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT241ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74ABT241ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ABT241APWR	TSSOP	PW	20	2000	346.0	346.0	33.0

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

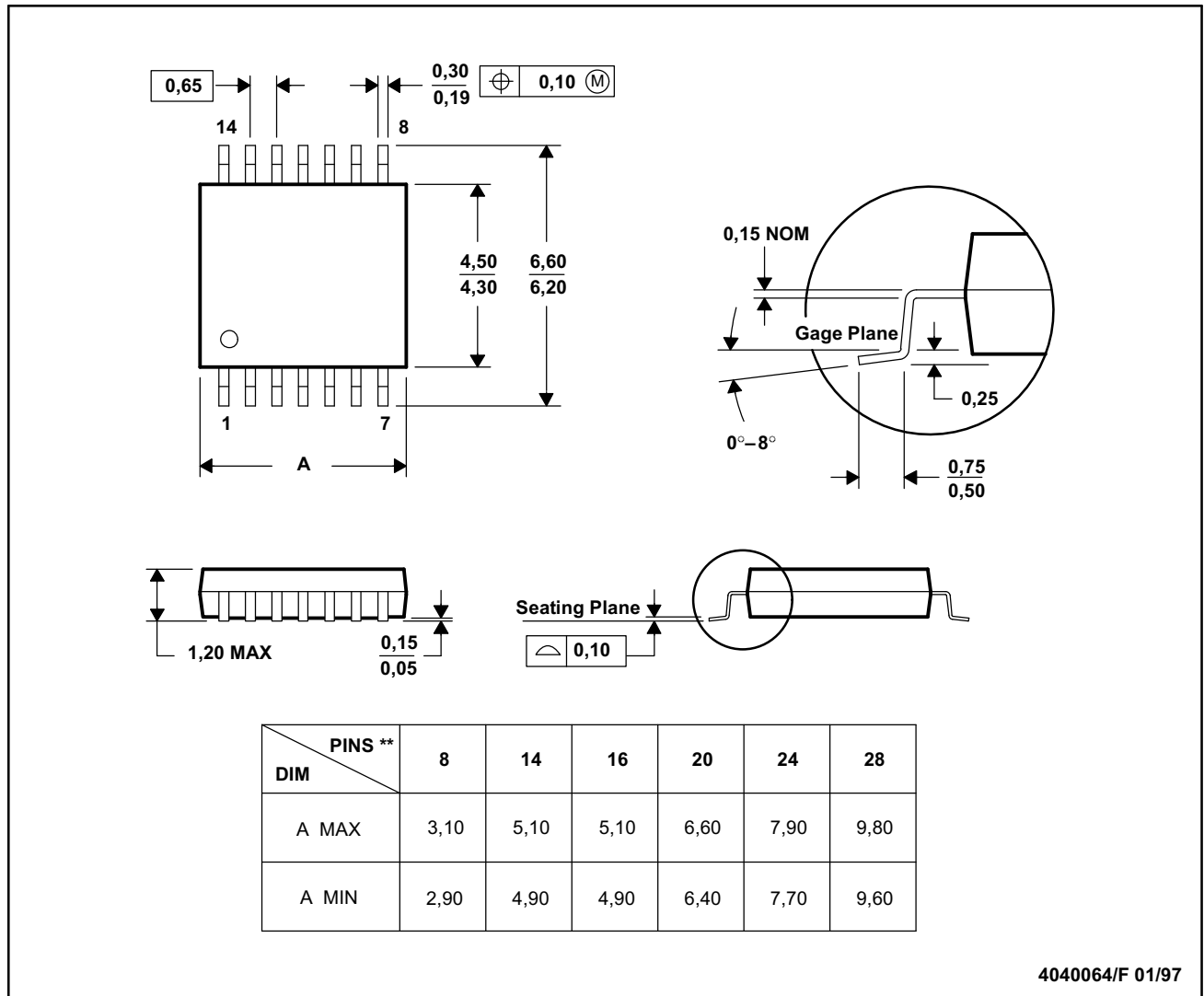
# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

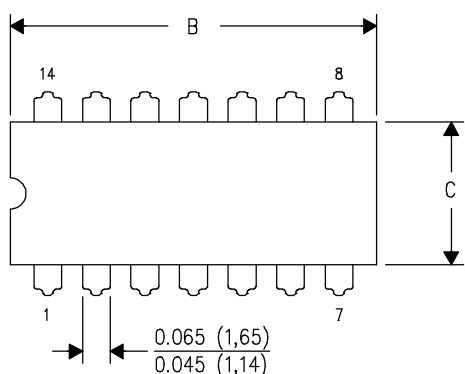
14 PINS SHOWN



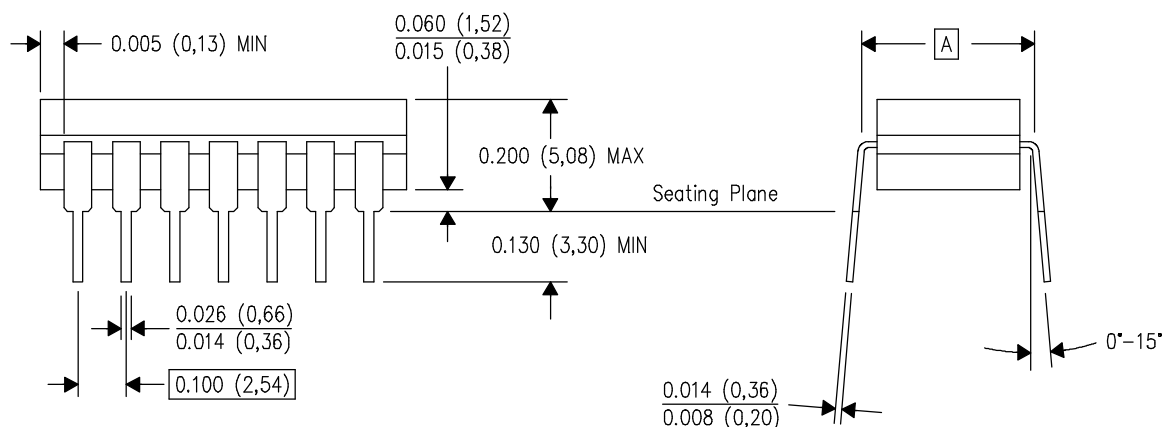
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

J (R-GDIP-T\*\*) 14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

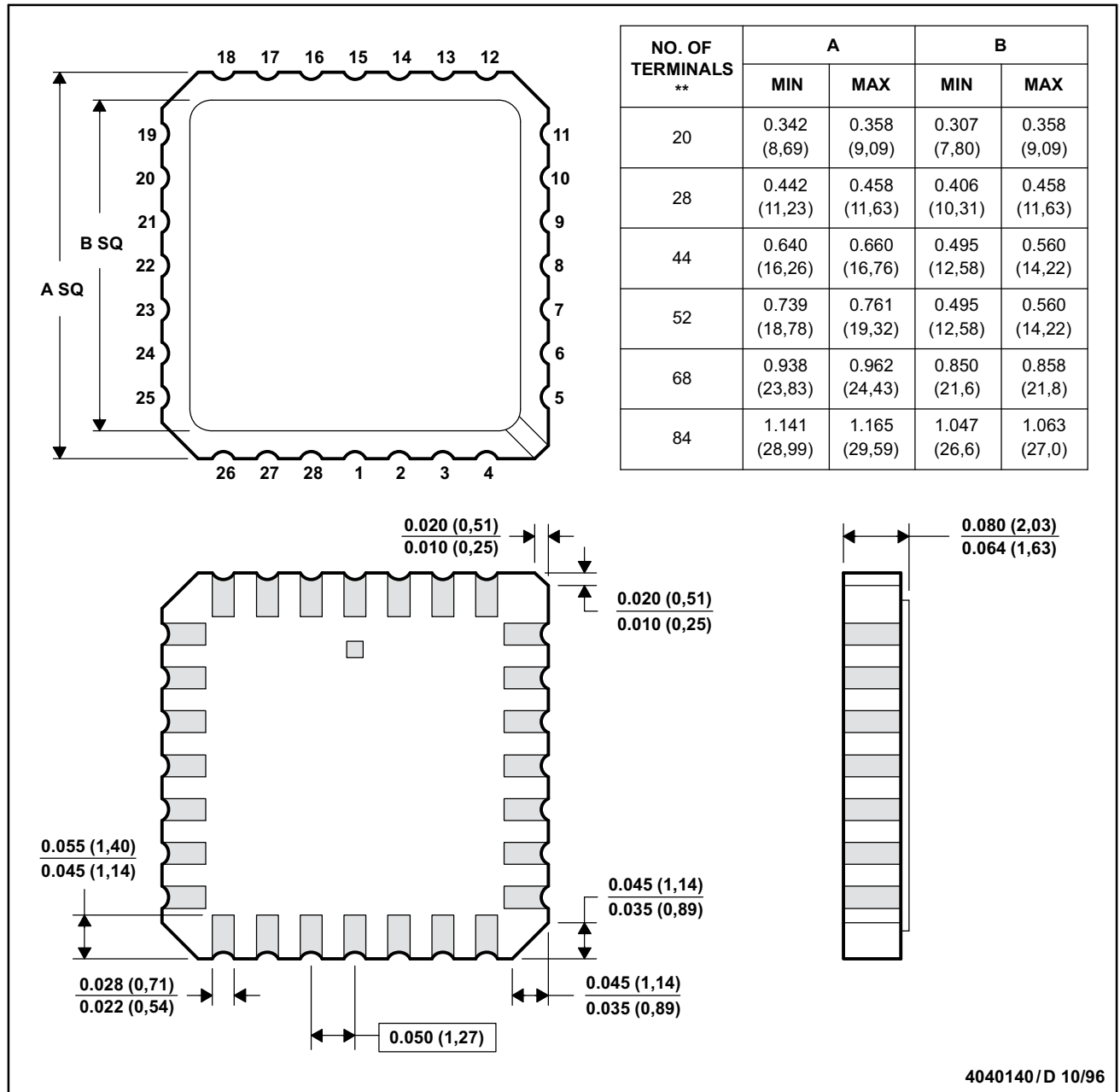
# MECHANICAL DATA

MLCC006B – OCTOBER 1996

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a metal lid.  
 D. The terminals are gold plated.  
 E. Falls within JEDEC MS-004

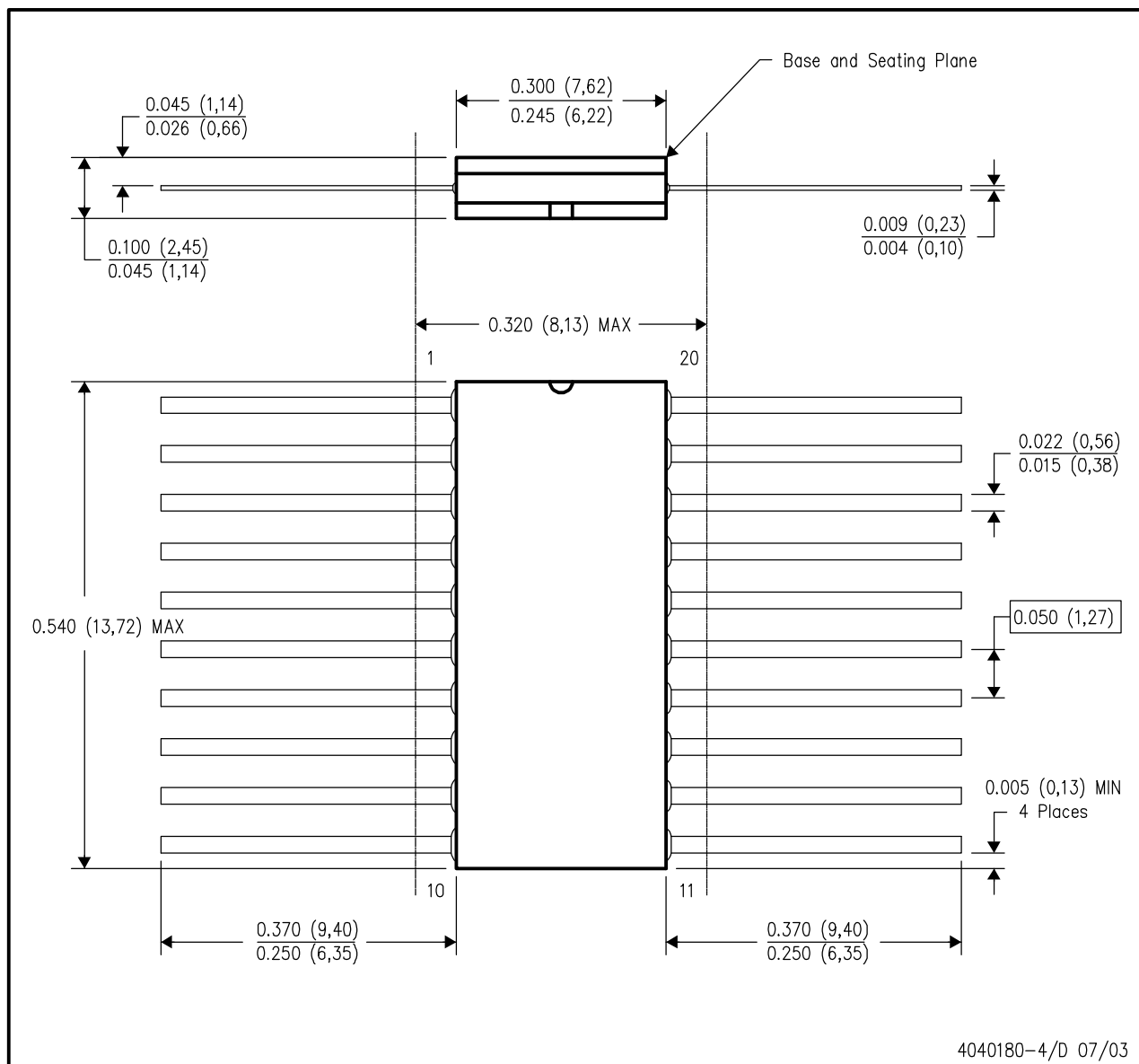
**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## MECHANICAL DATA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

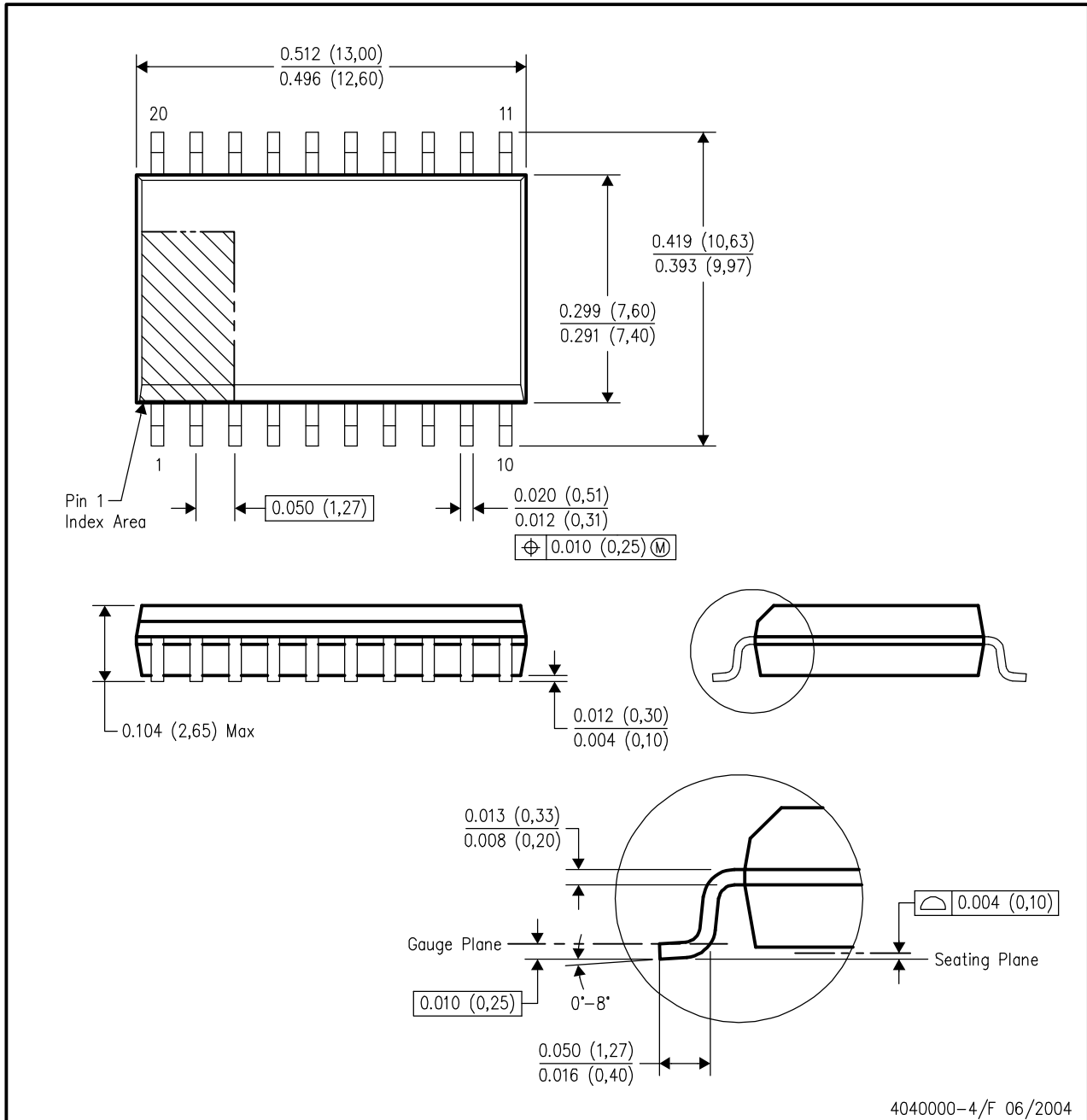


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within Mil-Std 1835 GDFP2-F20

# MECHANICAL DATA

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



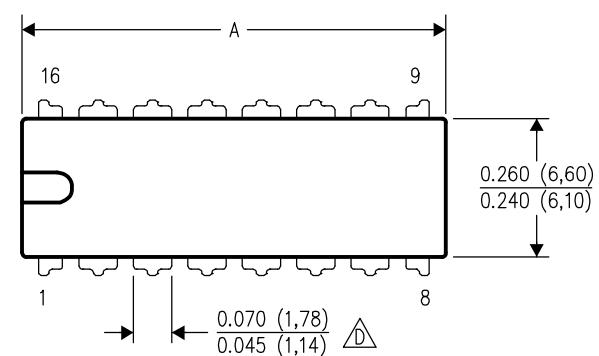
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

## MECHANICAL DATA

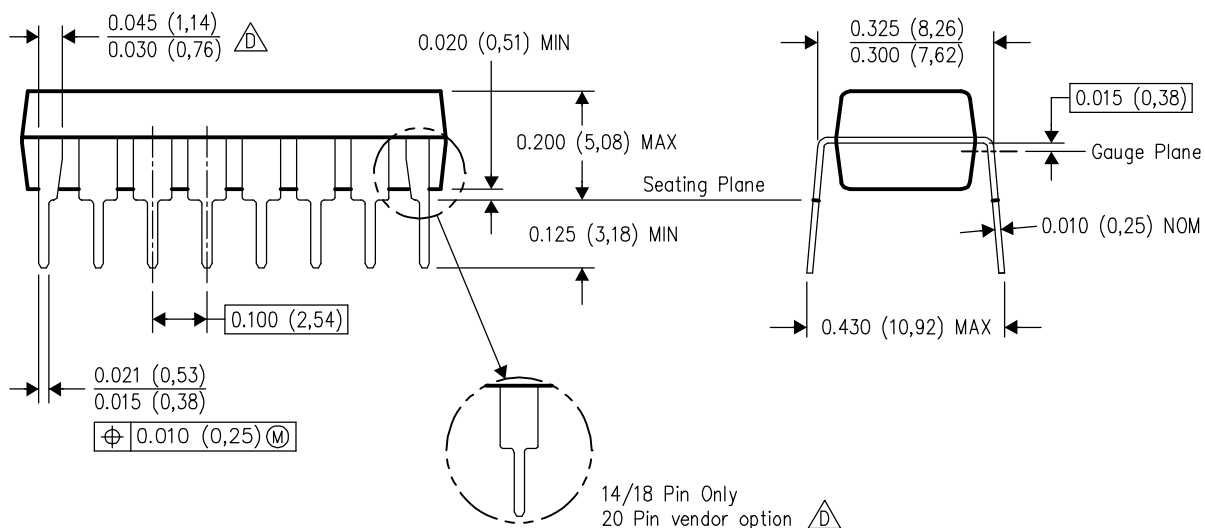
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
-  C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
-  D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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