

Vishay Siliconix

N-Channel 60-V (D-S) MOSFET

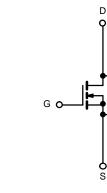
PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	
60	0.024 at V _{GS} = 10 V	7.5	
	0.03 at V _{GS} = 6.0 V	6.5	

FEATURES

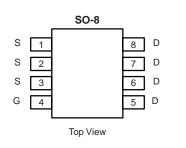
- Halogen-free According to IEC 61249-2-21
 Available
- TrenchFET[®] Power MOSFET



HALOGEN FREE Available



N-Channel MOSFET





ABSOLUTE MAXIMUM RATINGS	$T_A = 25$ °C, unles	ss otherwise not	eu		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V _{GS}	± 20	V	
	T _A = 25 °C	1	7.5		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C	I _D	5.5	•	
Pulsed Drain Current		I _{DM}	50	— A	
Continuous Source Current (Diode Conduction) ^a		۱ _S	2.1		
	T _A = 25 °C	D_	2.5	10/	
Maximum Power Dissipation ^a	T _A = 70 °C	P _D	1.6	W	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	50	°C/W	

Notes:

a. Surface Mounted on FR4 board, t \leq 10 s.

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm

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SPECIFICATIONS $T_J = 25 \text{ °C}$, unless otherwise noted							
Parameter	Symbol Test Conditions		Min.	Typ. ^a	Max.	Unit	
Static				•			
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 20 V$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			1	- μΑ	
		$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 \text{ °C}$			20		
On-State Drain Current ^b	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 10 V$	20			А	
Drain-Source On-State Resistance ^b	R _{DS(on)}	V_{GS} = 10 V, I _D = 7.5 A		0.020	0.024	0	
		$V_{GS} = 6.0 \text{ V}, I_D = 6.5 \text{ A}$		0.025	0.03	Ω	
Forward Transconductance ^b	9 _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 7.5 \text{ A}$		18.5		S	
Diode Forward Voltage ^b	V _{SD}	$I_{S} = 2.1 \text{ A}, V_{GS} = 0 \text{ V}$		0.75	1.2	V	
Dynamic				•			
Total Gate Charge	Qg			31	50	nC	
Gate-Source Charge	Q _{gs}	$V_{DS} = 30$ V, $V_{GS} = 10$ V, $I_{D} = 7.5$ A		7.7			
Gate-Drain Charge	Q _{gd}			8.3			
Gate Resistance	Rg		1		5.8	Ω	
Turn-On Delay Time	t _{d(on)}			16	30		
Rise Time	t _r	$\label{eq:VDD} \begin{array}{l} V_{DD} = 30 \ V, \ R_{L} = 30 \ \Omega \\ I_{D} \cong 1 \ A, \ V_{GEN} = 10 \ V, \ R_{g} = 6 \ \Omega \end{array}$		11	20	ns	
Turn-Off Delay Time	t _{d(off)}			41	80		
Fall Time	t _f			21	40		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.1 A, dI/dt = 100 A/µs		46	80		

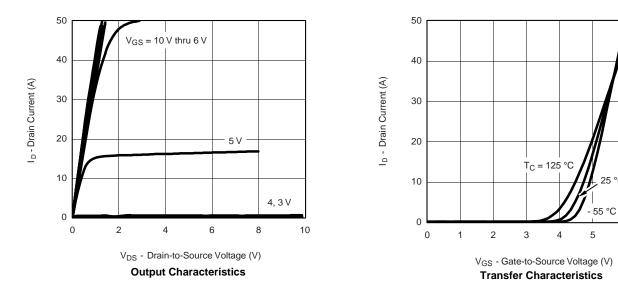
Notes:

a. For design aid only; not subject to production testing.

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



25

°C

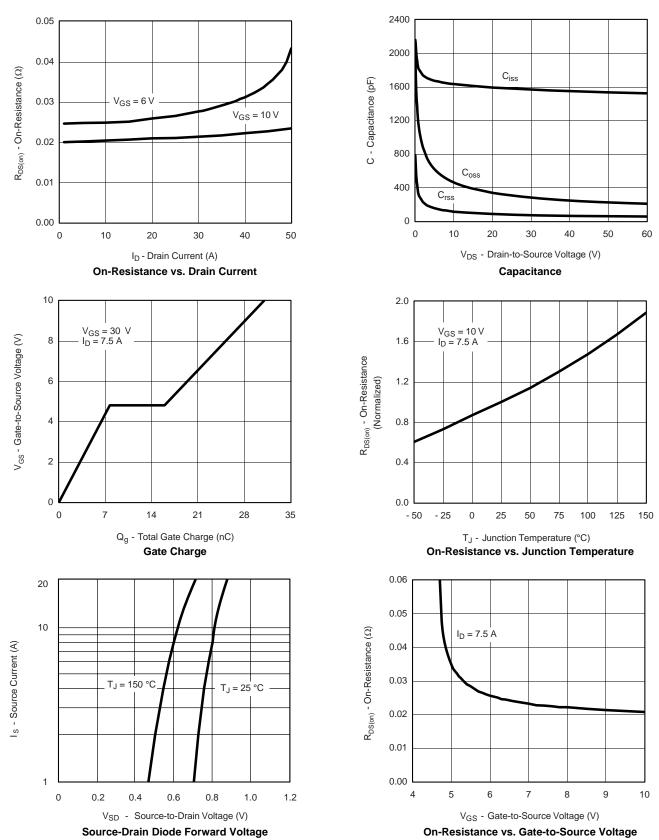
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Si4450DY Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

VISHAY

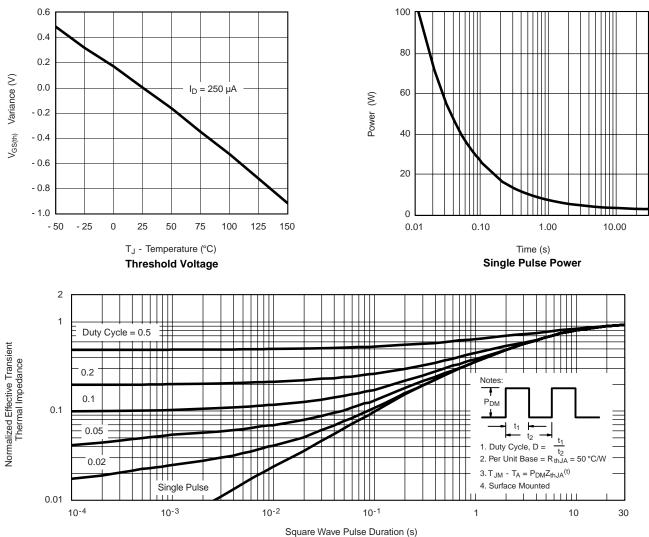


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Si4450DY

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70144.





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