32 768 BIT STATIC READ ONLY MEMORY

The SBB2632 is a 32 768 bit MOS N-channel static Read Only Memory. It is organised as 4096 eight-bit words.
This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

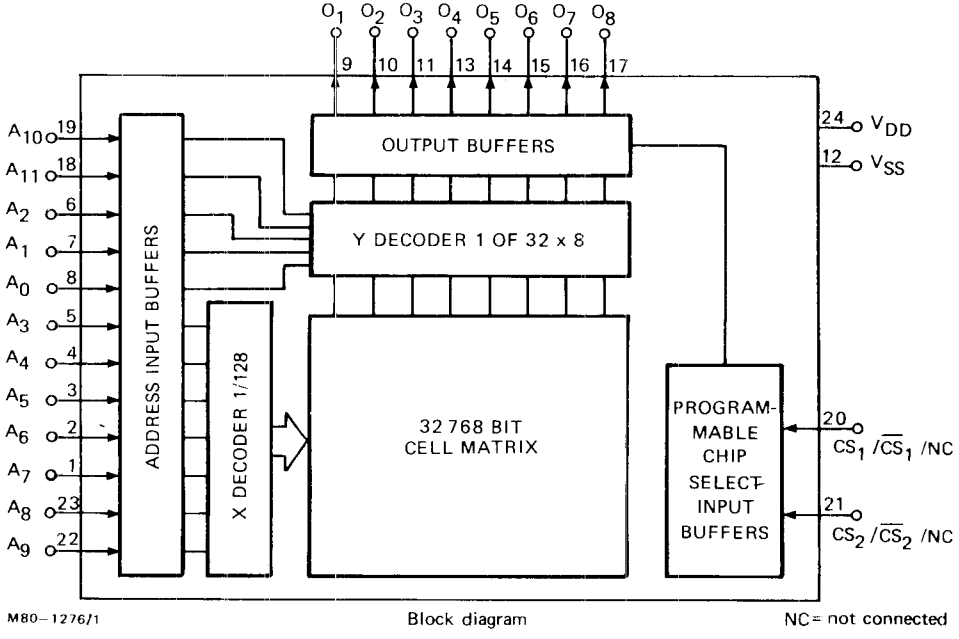
QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	max.	80	mA
Operating ambient temperature	T_{amb}		0 to 70	°C

PACKAGE OUTLINE

24-lead dual in line — Plastic (SOT–101): SBB2632P, Cerdip (SOT–94): SBB2632D
Cerdil (SOT–86): SBB2632E

BLOCK DIAGRAM



Block diagram

NC = not connected

Fig.1

32 768-BIT STATIC READ ONLY MEMORY

The SBB2632 is a 32 768 bit MOS N-channel static ROM organised as 4096 eight-bit words. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design considerations.

Features

- 450 ns access time; 2 TTL loads
- Two programmable chip select inputs
- Fully decoded
- All inputs and outputs directly TTL compatible
- Three-state outputs; OR-tied capability
- Single +5 V ± 10% power supply
- Protected inputs

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	max	80	mA
Operating ambient temperature range	T_{amb}		0 to +70	°C

purple binder, tab 5

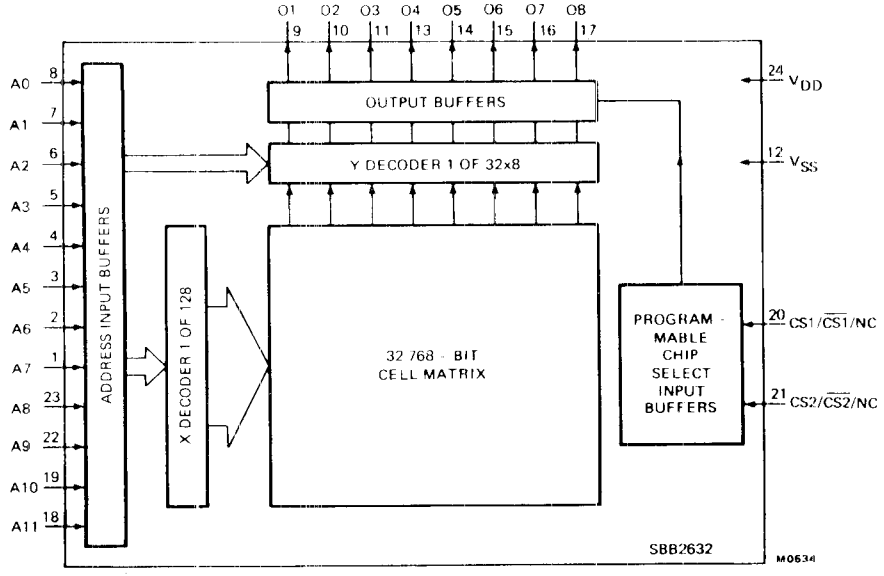


Fig. 1 Block diagram

PACKAGE OUTLINES

SBB2632P: 24-lead DIL; plastic (SOT-101A)
SBB2632D: 24-lead DIL; ceramic (SOT-94)
SBB2632E: 24-lead DIL; metal-ceramic (SOT-86B)

PINNING

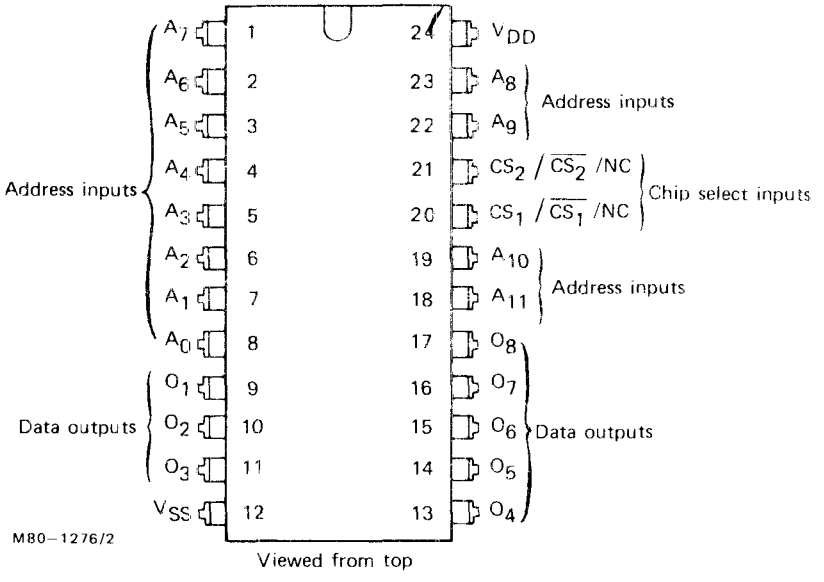


Fig.2

DESCRIPTION

The SBB2632 is a mask-programmable ROM and is manufactured to contain customer-defined data. The two chip select inputs are also programmable and any combination of active high or low or not connected chip select inputs can be defined by the customer. This combined with the 3-state data outputs allows the circuits to be 'OR TIED' for direct memory expansion.
The circuit requires a 5 V power supply and all inputs and outputs are directly TTL compatible.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (See MOS Handling Notes).

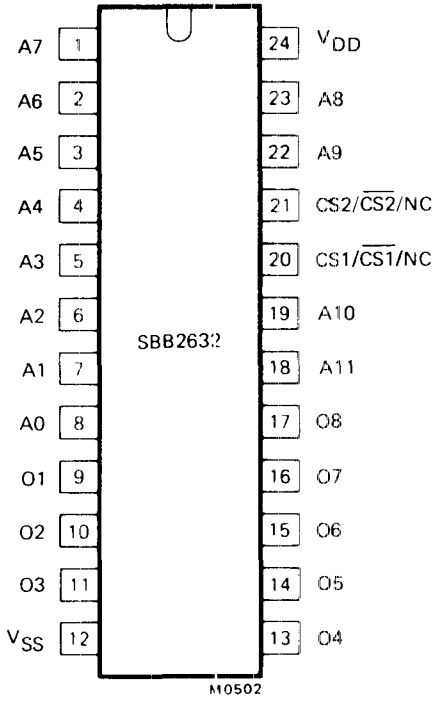


Fig.2 Pinning diagram.

PINNING

no.	type.	designation	function
1	I	A7	address inputs
2	I	A6	
3	I	A5	
4	I	A4	
5	I	A3	
6	I	A2	
7	I	A1	
8	I	A0	
9	O	O1	3-state data outputs
10	O	O2	
11	O	O3	
12		V_{SS}	ground
13	O	O4	3-state data outputs
14	O	O5	
15	O	O6	
16	O	O7	
17	O	O8	
18	I	A11	address input
19	I	A10	address input
20	I	CS1/$\overline{CS1}$/NC	chip select 1
21	I	CS2/CS2/NC	chip select 2
22	I	A9	address input
23	I	A8	address input
24		V_{DD}	positive supply (+5 V)

GENERAL DESCRIPTION

The SBB2632 is a mask-programmable ROM and is manufactured to contain customer-defined data. The two chip select inputs are also programmable, and any combination of active HIGH or LOW level or not connected chip select inputs can be defined by the customer. This, combined with the 3-state data outputs, allows the circuits to be 'OR TIED' for direct memory expansion. The circuit requires a single +5 V power supply, and all inputs and outputs are directly TTL compatible.

HANDLING

Inputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (See 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum System

Voltages (with respect to pin 12)

		min.	max.	
Supply voltage (pin 24)	V_{DD}	−0.5	7.0	V
Input voltage – All inputs (pins 1 to 8 and 18 to 23)		−0.5	7.0	V
Output voltage – All outputs (pins 9 to 11 and 13 to 17)		−0.5	7.0	V

Temperatures

Storage temperature	T_{stg}	−65 to 150	°C
Operating temperature	T_{amb}	0 to 70	°C

CHARACTERISTICS

Supply voltage		min.	typ.	max.	
V_{DD} (pin 24)		4.75	5.0	5.25	V

The following characteristics apply at T_{amb} = 0 to 70 °C and V_{DD} = 5.0 V ± 5% unless otherwise stated.

Supply current

I_{DD} (T_{amb} = 25 °C, outputs unloaded, V_{in} = V_{DD})		–	–	80	mA
All Inputs (pins 1 to 8 and 18 to 23)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input load current (V_{in} = 0 to 5.25 V)	I_{IN}	–	–	10	μA
Input capacitance (T_{amb} = 25 °C, f = 1.0 MHz)		–	–	7	pF
All outputs (pins 9 to 11 and 13 to 17)					
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{CC}	V
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output current in high impedance state (chip de-selected V_{out} = 0.4 V to V_{DD})		–	–	10	μA
Output capacitance (T_{amb} = 25 °C, f = 1.0 MHz		–	–	10	pF

DEVELOPMENT SAMPLE DATA

RATINGS (V_{SS} = 0 V)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	max.	7	V
Input voltage	V_I	max.	7	V
Output voltage	V_O	max.	7	V
Total power dissipation per package	P_{tot}	max.	1	W
Operating ambient temperature range	T_{amb}		0 to +70	°C
Storage temperature range	T_{stg}		−65 to +150	°C

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to +70 °C; unless otherwise stated.

parameter	symbol	min.	typ.	max.	conditions
Supply voltage	V_{DD}	4.5	5.0	5.5 V	
Supply current	I_{DD}	–	–	80 mA	chip deselected V_{DD} = 5.5 V $V_I = V_{DD}$
Inputs					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD} V	
Input voltage, LOW	V_{IL}	0	–	0.8 V	
Input load current	I_I	–	–	10 μA	V_I = 0 to 5.5 V V_{DD} = 5.5 V
Input capacitance	C_I	–	–	7 pF	f = 1 MHz; T_{amb} = 25 °C
Outputs					
Output voltage; HIGH	V_{OH}	2.4	–	V_{DD} V	$-I_{OH}$ = 200 μA
Output voltage; LOW	V_{OL}	–	–	0.4 V	I_{OL} = 3.2 mA, V_{DD} = 4.5 V
Output current in high-impedance state	I_O	–	–	10 μA	chip deselected V_O = 0.4 V to V_{DD}
Output capacitance	C_O	–	–	10 pF	f = 1 MHz; T_{amb} = 25 °C

DEVELOPMENT SAMPLE DATA

A.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 5 V ± 10%; T_{amb} = 0 to +70 °C unless otherwise specified.
Input transition time = 20 ns

	symbol	min.	typ.	max.	conditions
Timings (note 1; Fig.3)					
Address access time	t_{ACC}	–	–	450 ns	Output load is 2 TTL loads and 100 pF
Chip select delay (note 2)	t_{CO}	–	–	150 ns	
Chip de-select delay (note 3)	t_{DF}	–	–	100ns	
Previous data valid after address change delay	t_{OH}	20	–	– ns	

Notes

1. Timing reference levels: inputs = 1.5 V.
   outputs = 0.6 V and 2.2 V.
2. This maximum value of t_{CO} applies providing the valid address leads the chip select by $(t_{ACC} - t_{CO})$ns or more.
3. Measured at V_{OL} = 0.8 V on the LOW to 3-state transition.

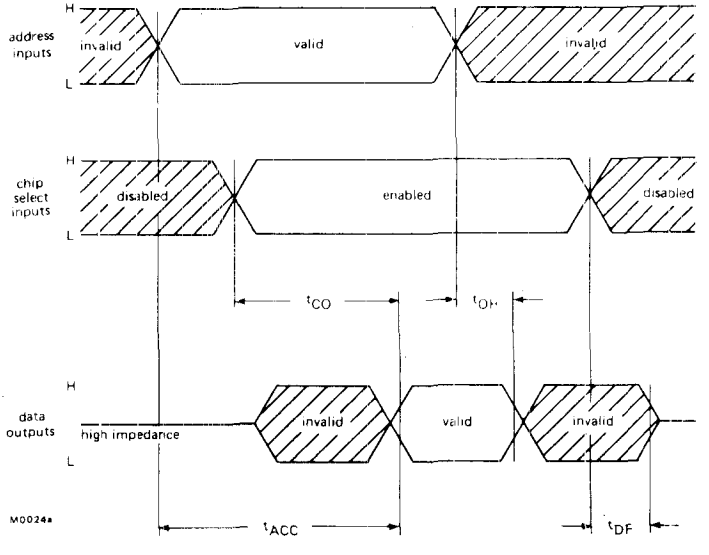


Fig.3 Timing diagram

Timings		min.	typ.	max.	
Address access time	t_{ACC}	–	–	450	ns
Chip select delay	t_{CO}	–	–	200	ns
Chip de-select delay	t_{DF}	–	–	200	ns
Previous data valid after address change delay	t_{OH}	20	–	–	ns

TIMING DIAGRAM

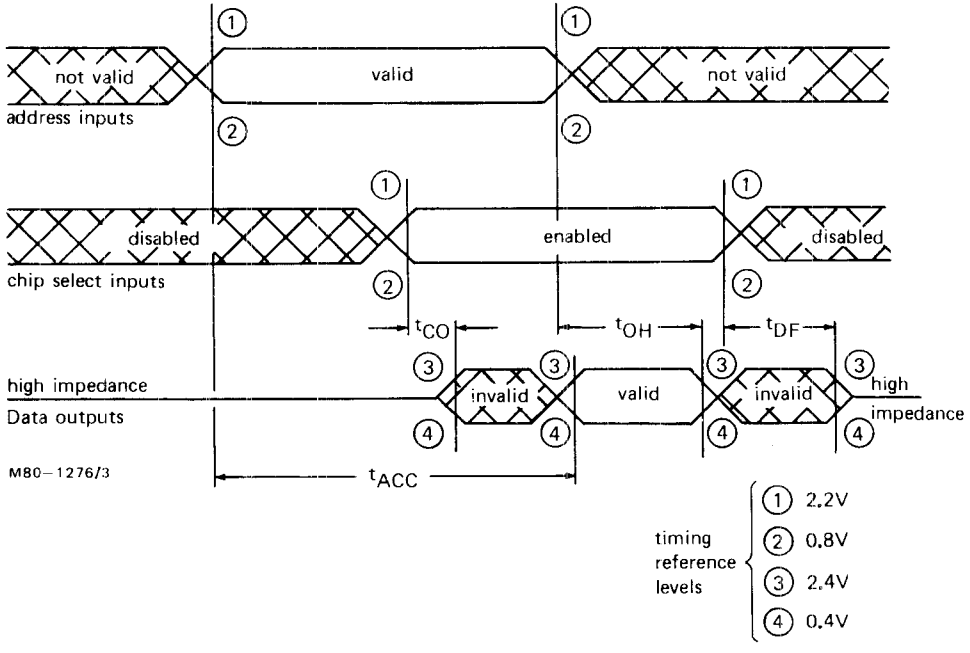
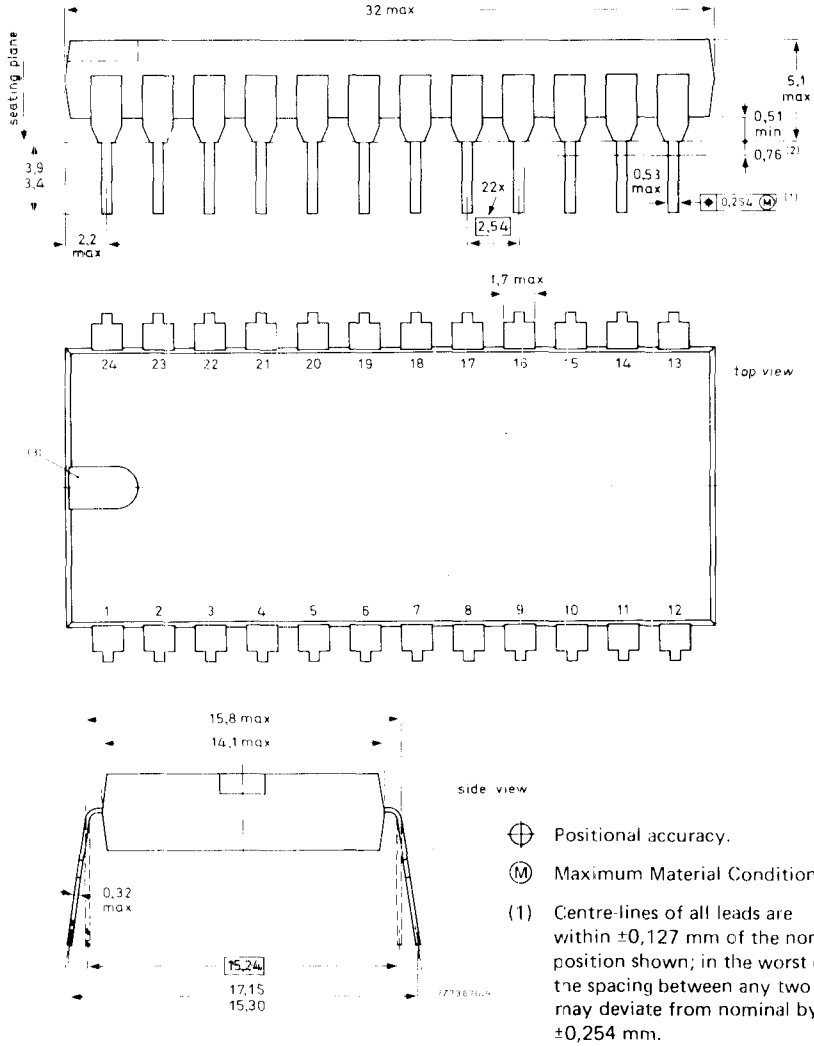


Fig.3

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

SOLDERING

See next page

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

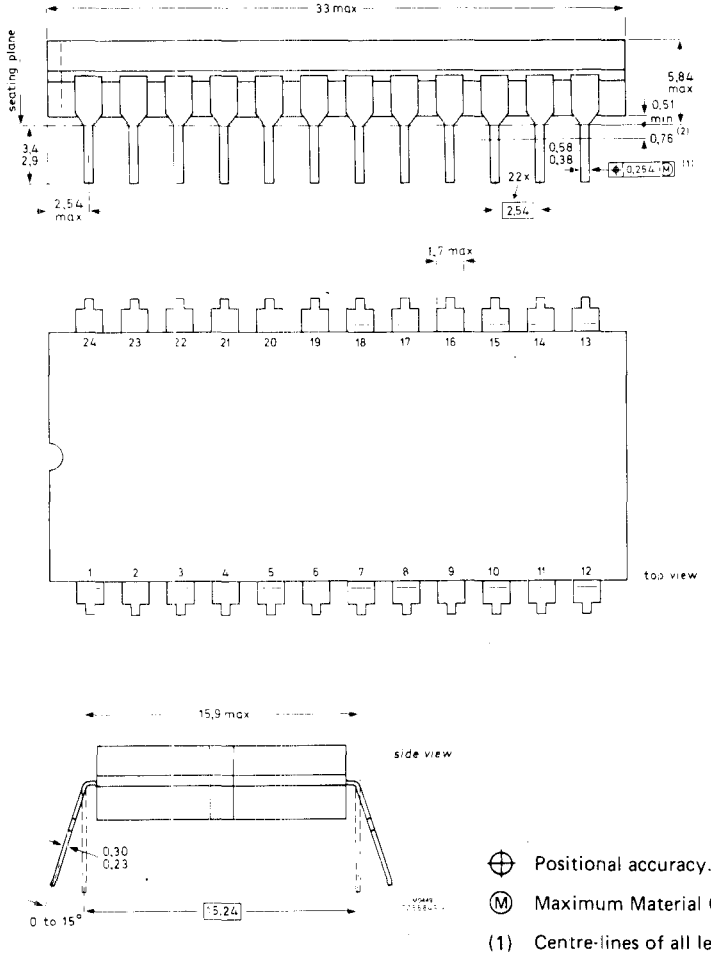
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; CERAMIC (SOT-94)



1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

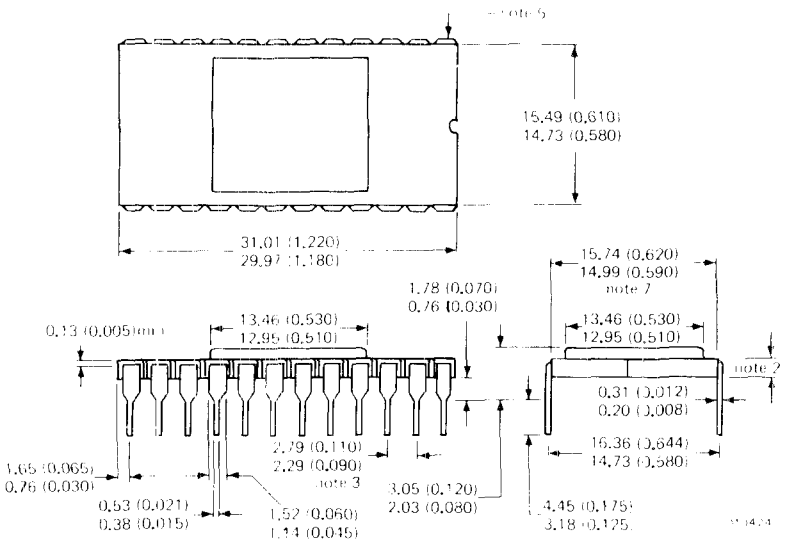
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

24-LEAD DUAL IN-LINE; METAL CERAMIC (SOT-86B)



Dimensions in mm (note 1)

Notes

1. Dimensions shown in parentheses are in inches.
2. Lead spacing shall be measured within this zone.
   Shoulder and lead tip dimensions are to the centre line of leads.
3. Tolerances are non-cumulative.
4. Lead material: ASTM alloy F-15 (KOVAR) or equivalent – tin plated.
5. Body material: ceramic ASTM alloy F-15 or equivalent.
6. Lead number 1 denoted by Signetics symbol, angle cut, or lead tab.
7. Dimension also applies to seating plane.