5 V Precision Voltage Reference/Temperature Transducer

REF02

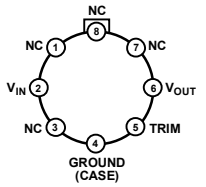
FEATURES

5 V output: ±0.3% maximum
Temperature voltage output: 1.96 mV/°C
Adjustment range: ±3% minimum
Excellent temperature stability: 8.5 ppm/°C maximum
Low noise: 15 µV p-p maximum
Low supply current: 1.4 mA maximum
Wide input voltage range: 7 V to 40 V
High load-driving capability: 10 mA
No external components
Short-circuit proof

GENERAL DESCRIPTION

The REF02 precision voltage reference provides a stable 5 V output that can be adjusted over a ±6% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 7 V to 40 V, low current drain of 1 mA, and excellent temperature stability are achieved with an improved band gap design. Low cost, low noise, and low power make the REF02 an excellent choice whenever a stable voltage reference is required. Applications include DACs and ADCs, portable instrumentation, and digital voltmeters. The versatility of the REF02 is enhanced by its use as a monolithic temperature transducer. For new designs, refer to the ADR02.

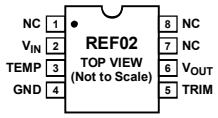
PIN CONFIGURATIONS



NC = NO CONNECT. DO NOT CONNECT ANYTHING ON THESE PINS. SOME OF THEM ARE RESERVED FOR FACTORY TESTING PURPOSES.

00375-F-001

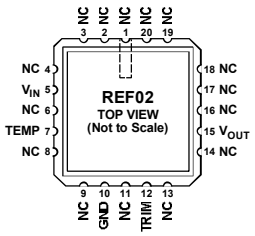
Figure 1. 8-Lead TO-99 (J-Suffix)



NC = NO CONNECT. DO NOT CONNECT ANYTHING ON THESE PINS. SOME OF THEM ARE RESERVED FOR FACTORY TESTING PURPOSES.

00375-F-002

Figure 2. 8-Lead PDIP (P-Suffix), 8-Lead CERDIP (Z-Suffix) and 8-Lead SOIC (S-Suffix)



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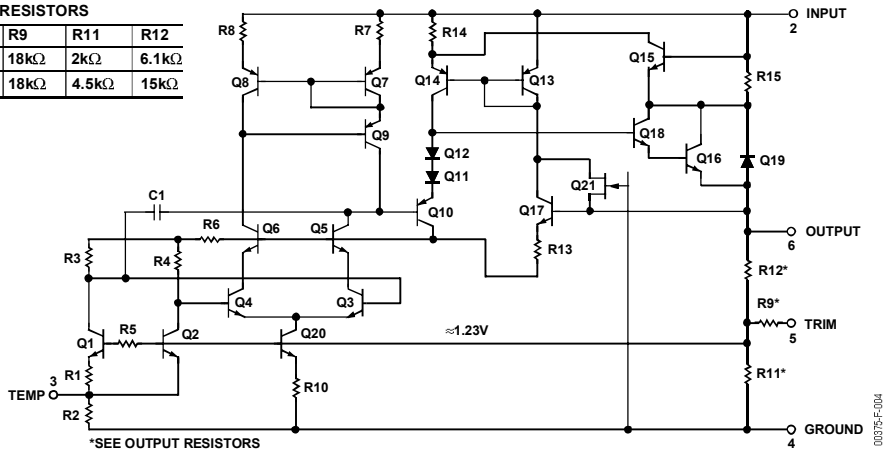
00375-F-003

Figure 3. 20-Terminal LCC (RC-Suffix)

OUTPUT RESISTORS

REF02 OPTION	R9	R11	R12
883C PRODUCT	18kΩ	2kΩ	6.1kΩ
P, S, J, Z PACKAGES	18kΩ	4.5kΩ	15kΩ



00375-F-004

Figure 4. Simplified Schematic

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

@ V_{IN} = 15 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	REF02A/REF02E Min	REF02A/REF02E Typ	REF02A/REF02E Max	REF02/REF02H Min	REF02/REF02H Typ	REF02/REF02H Max	Unit
Output Voltage	V_O	I_L = 0 mA	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{TRIM}	R_P = 10 kΩ	±3	±6		±3	±6		%
Output Voltage Noise[1]	e_n p-p	0.1 Hz to 10 Hz							
P, Z, and S Packages				15			15		µV p-p
J Package				20			20		µV p-p
883 Parts				10	15		10	15	µV p-p
Line Regulation[2]		V_{IN} = 8 V to 40 V		0.006	0.010		0.006	0.010	%/V
Load Regulation[2]		I_L = 0 mA to 10 mA		0.005	0.010		0.006	0.010	%/mA
Turn-On Settling Time[1]	t_{ON}	To ±0.1% of final value		5			5		µs
Quiescent Supply Current	I_{SY}	No load		1.0	1.4		1.0	1.4	mA
Load Current	I_L		10			10			mA
Sink Current[3]	I_S		−0.3	−0.5		−0.3	−0.5		mA
Short-Circuit Current	I_{SC}	V_O = 0		30			30		mA
Temperature Voltage Output[4]									
883C Product	V_T			630			630		mV
P, S, J, and Z Packages	V_T			550			550		mV

[1] Guaranteed by design.
[2] Line and load regulation specifications include the effect of self-heating.
[3] During sink current test, the device meets the output voltage specified.
[4] Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.

@ V_{IN} = 15 V, −55°C ≤ T_A ≤ +125°C for REF02A and REF02; 0°C ≤ T_A ≤ 70°C for REF02E and REF02H; I_L = 0 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	REF02A/REF02E Min	REF02A/REF02E Typ	REF02A/REF02E Max	REF02/REF02H Min	REF02/REF02H Typ	REF02/REF02H Max	Unit
Output Voltage Change with Temperature[1, 2]	ΔV_{OT}	0°C ≤ T_A ≤ 70°C		0.02	0.06		0.07	0.17	%
		−55°C ≤ T_A ≤ +125°C		0.06	0.15		0.18	0.45	%
Output Voltage Temperature Coefficient[3]	TCV_O			3	8.5		10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_P = 10 kΩ		0.7			0.7		ppm/%
Line Regulation V_{IN} = 8 V to 40 V[4]		0°C ≤ T_A ≤ 70°C		0.007	0.012		0.007	0.012	%/V
		−55°C ≤ T_A ≤ +125°C		0.009	0.015		0.009	0.015	%/V
Load Regulation I_L = 0 mA to 8 mA[4]		0°C ≤ T_A ≤ 70°C		0.006	0.010		0.007	0.012	%/mA
		−55°C ≤ T_A ≤ +125°C		0.007	0.012		0.009	0.015	%/mA
Temperature Voltage Output Temperature Coefficient[5]	TCV_T								
883C Product				2.10			2.10		mV/°C
P, S, J, and Z Packages				1.96			1.96		mV/°C

[1] ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5 V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5\ \text{V}} \right| \times 100$$

[2] ΔV_{OT} specification applies trimmed to 5,000 V or untrimmed.

[3] TCV_O is defined as ΔV_{OT} divided by the temperature range.

$$TCV_O = \frac{\Delta V_{OT}}{70°\text{C}}$$

[4] Line and load regulation specifications include the effect of self-heating.

[5] Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.

@ V_{IN} = 15 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	REF02C Min	REF02C Typ	REF02C Max	REF02D Min	REF02D Typ	REF02D Max	Unit
Output Voltage	V_O	I_L = 0 mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{TRIM}	R_P = 10 kΩ	±2.7	±6.0		±2.0	±6.0		%
Output Voltage Noise[1]	e_n p-p	0.1 Hz to 10 Hz							
P, Z, and S Packages				15					µV p-p
J Package				20			15		µV p-p
883 Parts				12	18		20		µV p-p
Line Regulation[2]		V_{IN} = 8 V to 40 V		0.009	0.015		0.010	0.04	%/V
Load Regulation[2]		I_L = 0 mA to 8 mA		0.006	0.015				%/mA
		I_L = 0 mA to 4 mA					0.015	0.04	%/mA
Turn-On Settling Time[1]	t_{ON}	To ±0.1% of final value		5			5		µs
Quiescent Supply Current	I_{SY}	No load		1.0	1.6		1.0	2.0	mA
Load Current	I_L		8			8			mA
Sink Current[3]	I_S		−0.3	−0.5		−0.3	−0.5		mA
Short-Circuit Current	I_{SC}	V_O = 0		30			30		mA
Temperature Voltage Output[4]									
883C Product	V_T			630			630		mV
P, S, J, and Z Packages	V_T			550			550		mV

[1] Guaranteed by design.
[2] Line and load regulation specifications include the effect of self-heating.
[3] During sink current test, the device meets the output voltage specified.
[4] Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.

@ V_{IN} = 15 V, I_L = 0 mA, 0°C ≤ T_A ≤ 70°C for REF02CJ, REF02CZ, and REF02DP; and −40°C ≤ T_A ≤ +85°C for REF02CP and REF02CS, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	REF02C Min	REF02C Typ	REF02C Max	REF02D Min	REF02D Typ	REF02D Max	Unit
Output Voltage Change with Temperature[1, 2]	ΔV_{OT}			0.14	0.45		0.49	1.7	%
Output Voltage Temperature Coefficient[3]	TCV_O			20	65		70	250	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_P = 10 kΩ		0.7			0.7		ppm/%
Line Regulation[4]		V_{IN} = 8 V to 40 V		0.011	0.018		0.012	0.05	%/V
Load Regulation[4]		I_L = 0 mA to 5 mA		0.008	0.018		0.016	0.05	%/mA
Temperature Voltage Output Temperature Coefficient[5]	TCV_T								
883C Product				2.10			2.10		mV/°C
P, S, J, and Z Packages				1.96			1.96		mV/°C

[1] ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5 V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5\ \text{V}} \right| \times 100$$

[2] ΔV_{OT} specification applies trimmed to 5,000 V or untrimmed.

[3] TCV_O is defined as ΔV_{OT} divided by the temperature range.

$$TCV_O = \frac{\Delta V_{OT}}{70°\text{C}}$$

[4] Line and load regulation specifications include the effect of self-heating.

[5] Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating[1]
Input Voltage	40 V
Output Short-Circuit Duration to Ground or V_{IN}	Indefinite
Storage Temperature Range	
J, RC, and Z Packages	−65°C to +150°C
P Package	−65°C to +125°C
Operating Temperature Range	
REF02A, REF02J, REF02RC	−55°C to +125°C
REF02CJ, REF02CZ	0°C to 70°C
REF02CP, REF02CS, REF02E, and REF02H	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] Absolute maximum ratings apply to both DICE packaged parts, unless otherwise noted.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

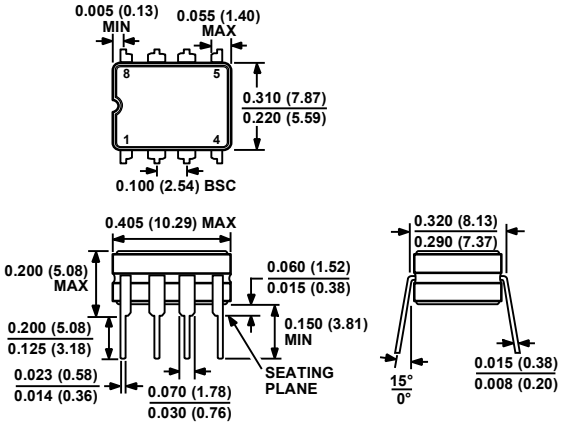
Package Type	θ_{JA}[1]	θ_{JC}	Unit
TO-99 (J)	170	24	°C/W
8-Lead CERDIP (Z)	162	26	°C/W
8-Lead PDIP (P)	110	50	°C/W
20-Terminal Ceramic LCC (RC)	120	40	°C/W
8-Lead SOIC (S)	160	44	°C/W

[1] θ_{JA} is specified for worst-case mounting conditions; device in socket for TO, CERDIP, PDIP, and LCC packages; and device soldered to printed circuit board for SOIC package.

ESD CAUTION

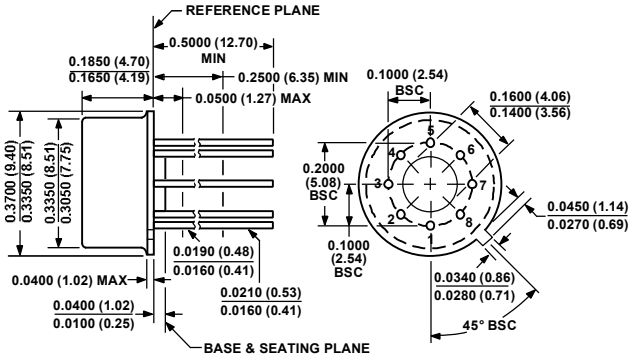
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS



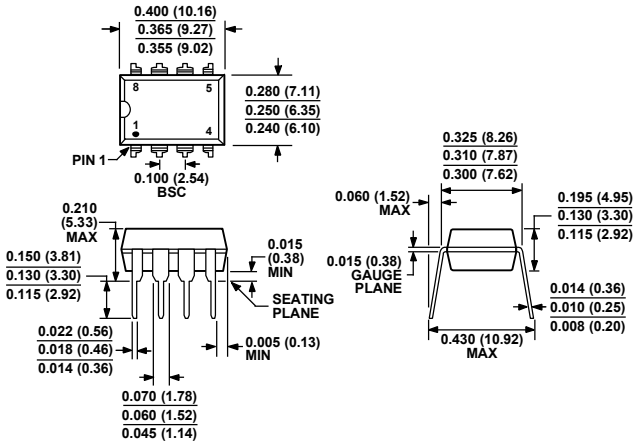
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 27. 8-Lead Ceramic Dual In-Line Package [CERDIP]
Z-Suffix
(Q-8)
Dimensions shown in inches and (millimeters)



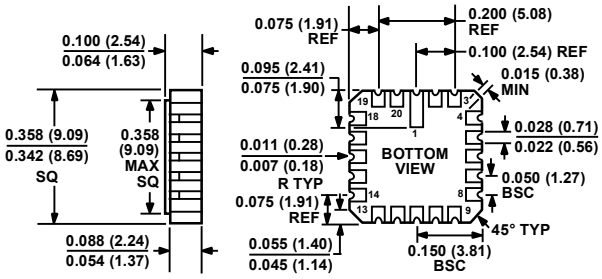
COMPLIANT TO JEDEC STANDARDS MO-002-AK
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 29. 8-Lead Metal Header Package [TO-99]
J-Suffix
(H-08)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001-BA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 28. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
P-Suffix
(N-8)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 30. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
RC-Suffix
(E-20A)
Dimensions shown in inches and (millimeters)

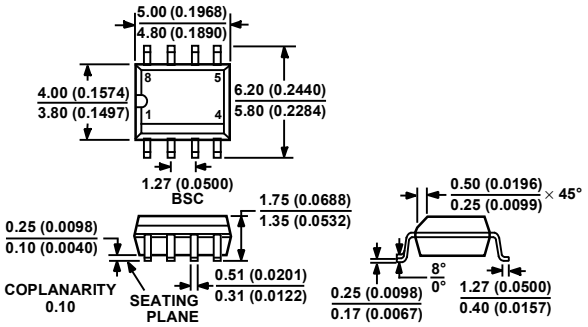


Figure 31. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body
S-Suffix
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	T_A = 25°C ΔV_{OS} Max (mV)	Temperature Range	Package Description	Package Option
REF02AJ/883C[1]	±15	−55°C to +125°C	8-Lead TO-99	J-Suffix (H-08)
REF02AZ	±15	−55°C to +125°C	8-Lead CERDIP	Z-Suffix (Q-8)
REF02AZ/883C[1]	±15	−55°C to +125°C	8-Lead CERDIP	Z-Suffix (Q-8)
REF02CJ	±50	0°C to 70°C	8-Lead TO-99	J-Suffix (H-08)
REF02CP	±50	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
REF02CPZ[2]	±50	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
REF02CS	±50	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CS-REEL	±50	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CS-REEL7	±50	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CSZ[2]	±50	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CSZ-REEL[2]	±50	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CSZ-REEL7[2]	±50	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CZ	±50	0°C to 70°C	8-Lead CERDIP	Z-Suffix (Q-8)
REF02DP	±100	0°C to 70°C	8-Lead PDIP	P-Suffix (N-8)
REF02DPZ[2]	±100	0°C to 70°C	8-Lead PDIP	P-Suffix (N-8)
REF02EJ	±15	−40°C to +85°C	8-Lead TO-99	J-Suffix (H-08)
REF02EZ	±15	−40°C to +85°C	8-Lead CERDIP	Z-Suffix (Q-8)
REF02J	±25	−55°C to +125°C	8-Lead TO-99	J-Suffix (H-08)
REF02HJ	±25	−40°C to +85°C	8-Lead TO-99	J-Suffix (H-08)
REF02HZ	±25	−40°C to +85°C	8-Lead CERDIP	Z-Suffix (Q-8)
REF02HP	±25	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
REF02HPZ[2]	±25	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
REF02HS	±25	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02HSZ[2]	±25	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02RC/883[1]	±25	−55°C to +125°C	20-Lead LCC	RC-Suffix (E-20A)
REF02Z	±25	−55°C to +125°C	8-Lead CERDIP	Z-Suffix (Q-8)

[1] Consult sales for 883 data sheet.
[2] Z = Pb-free part.