Rockwell

PCMCIA Interface Control Adapter (PICA)

INTRODUCTION

The Rockwell PCMCIA Interface Control Adapter (PICA), packaged in a single industry-standard 100-pin ultra-thin quad flat package (TQFP), provides all of the functions necessary to interface Rockwell modem device sets to a PCMCIA PC Card Standard (Release 2.0) compatible bus connector (socket) interface. The PICA is specifically designed to interface PCMCIA and ExCA™ compatible host socket interfaces to Rockwell RC224ATF, and RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL family modems.

The PICA provides the required configuration registers and address decoding to support a full-featured implementation of a PCMCIA PC Card modem. The addressing decode supports four built-in communication ports (commonly referred to as COM1 through COM4), or optionally allows for host-supported port decoding.

Additional circuits are required to provide for the PCMCIA Card Information Structure (CIS) memory and digital audio generation (optional). The recommended CIS memory size is 256 bytes. This CIS should contain the PCMCIA tuple definitions necessary to define the functionality of the PC Card modem implementation, including support for the modem extension tuple. Refer to the PCMCIA PC Card Standard (Release 2.0) for further guidance.

Ring indication handling support is provided by two different methods. The recommended method implements the optional I/O Event Indication Register for statusing I/O Card events. In this approach, Ring indications are registered and the PCMCIA status change process is initiated. The secondary method follows the ExCA implementation approach whereby the Ring indication is directly routed to the status change signal pin.

Rockwell PCMCIA AccelerATor™ kits are available for modems in the above named families. AccelerATor™ kits speed time to market by providing an evaluation and development board in the form of a completed PCMCIA card design, along with design notes, schematics, and printed circuit board layouts.

The Rockwell PICA device manufacturing number is R8290.

FEATURES

- Four PCMCIA Card Configuration Registers
  - Configuration Option Register (full support)
  - Card Configuration and Status Register (full support)
  - Pin Replacement Register (RRdy/Bsy and CRdy/Bsy functions)
  - I/O Event Indication Register (RIEnab and RIEvt functions)
- Decodes PCMCIA PC Card addresses
  - Provides chip selects for the modem and CIS memory
  - Supports the decoding for 4 standard COM ports in Overlapping I/O Address Mode
  - Supports Independent I/O Address Mode
- Supports unrestricted CIS Table Access
- Performs power-down mode control support for the following Rockwell modem families:
  - RC224ATF
  - C39 controller-based RC96V24AC/ RC14V24AC
  - C39 controller-based RC96ACL/ RC144ACL
- Selectable pass through of PCMCIA audio data
- Supports two ring handling methods
  - I/O Event Indication Register
  - Ring Indicate pass-through to Status Change
- 100-pin 1.5 mm height ultra-thin quad flat package (TQFP)
- Low power +5 volt operation: 35 mW (typical)

ExCA is a trademark of the Intel Corporation.
AccelerATor is a trademark of Rockwell International.

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TECHNICAL SPECIFICATIONS

FUNCTIONAL INTERFACES

The PICA has the following functional interfaces: the PCMCIA socket, CIS memory, modem, DAA (i.e., Data Access Arrangement), and digital audio signal.

The PICA additionally provides Power Management support via the Card Configuration and Status Register (CCSR) in attribute memory.

The PICA Interconnect Block Diagram is given in Figure 1.

PCMCIA Card Connector Interface

The PCMCIA 68-pin Card Connector (Socket) provides the interface between the host and PC card, with 60 signal and 8 power pins. The signal pins provide data and address lines, output and address enables, I/O read and write signals, a digital audio signal, an interrupt, a reset, and supporting status signals.

Attribute Memory Interface. The host interfaces with the PICA to control and receive status information from the modem. This is accomplished by way four PCMCIA card configuration registers contained in attribute memory, with access supported by the address decode logic. The Card Information Structure (CIS) also resides in attribute memory, and contains information about the PC-card and its features.

Address Decode Logic. The address decode logic controls access to the Card Configuration Registers in attribute memory, decodes valid accesses to the CIS and to the modem, and provides chip selects and an input acknowledge signal (-INPACK).

Card Information Structure (CIS). The CIS table resides in a customer-provided programmable memory device such as ROM or EEPROM that has a minimum capacity of 256 bytes. The CIS table provides the host with PC Card specific information including card type, address range decoding capability, and control requirements to complete host link establishment with the PC card.

Card Configuration Registers. Four single-byte PICA card configuration registers provide the PC with the capability to configure, control, and receive status from the PICA, and as a consequence, the modem. The functionality of these four registers and their individual bit settings is described in Section 3.

Modem Interface

The PICA provides host control and status of the modem across the PICA/modem interface. This interface includes modem select, read, power down, and reset signals as well as a Ring indicate signal, and modem ready and service request interrupt modem status signals.

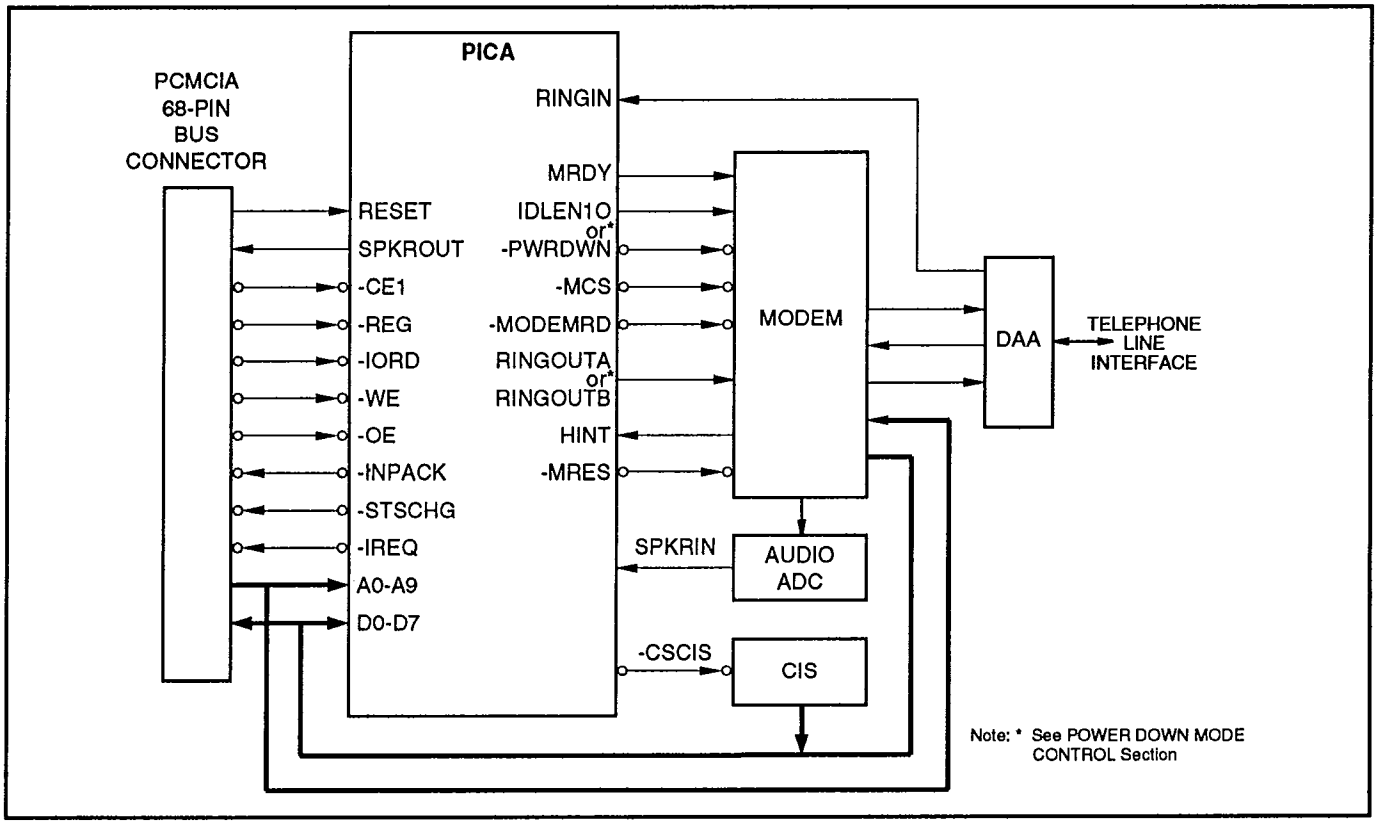


Figure 1. PICA Interconnect Block Diagram

The PCMCIA Card Connector directly connects to the modem address and data bus providing the modem digital data transfer path.

DAA interface

The PICA receives the Ring indicate signal from the DAA, that may be host-selectably passed to the modem to initiate modem call reception.

Digital Audio Signal interface

The PICA supports the throughput of a digital audio signal that is host-selectably passed to the host without signal conditioning to drive a speaker.

Power Management

The PICA supports host power management of the PC Card. This is accomplished by a host write into the PwrDwn bit of the Card Configuration and Status Register resulting in the PC Card being placed in power down mode.

CARD INFORMATION STRUCTURE (CIS) DESIGN INFORMATION

The modem's Card Information Structure (CIS) must be located in attribute memory beginning at address zero, with each byte residing at an even address location. To implement the CIS on the PCMCIA modem card, a small programmable memory device should be used with the host address lines offset to the device's address lines by one bit. The memory device can then be loaded with the CIS data at each of the device's memory locations. This results in consecutive bytes of data in the device being located at consecutive even address locations in attribute memory. The Rockwell PICA provides a chip select (-CSCIS) which should be tied to the memory device's chip select pin. The -CSCIS signal is asserted by the PICA for valid EVEN address accesses to attribute memory in the range 000h-1FFh, allowing access to up to 256 bytes of CIS data.

The memory device used for the CIS can be either a ROM device or a re-programmable device such as an EEPROM. By using a re-programmable device and connecting the PCMCIA socket's -WE signal to the CIS write enable pin, the CIS parameters can be modified during product development. However, in production designs, the -WE signal should be disabled or a ROM device should be used so that the CIS table cannot be inadvertently overwritten during operation.

POWER DOWN MODE CONTROL

Power Down Mode control is provided to support the operation of the lowest-power mode, stop mode, in Rockwell's RC224ATF and C39 controller-based RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL complete modem solutions. Note that C29 controller-based modem solutions do not support stop mode, and the Power Down Mode control cannot be used with these modems.

General Description

The following describes the operation and modem interaction of the PICA when the PwrDwn bit in the Card Configuration and Status Register (CCSR) is set by the host to make a power down request.

Several PICA signals control modem entry into low power Sleep Mode and Stop Mode. Sleep Mode is the normal power down mode entered automatically during periods of inactivity (as defined by the value of the modem's S24 register), while Stop Mode is the power down mode selected when the PwrDwn bit is set in the CCSR.

The IDLEN1O and -PWRDWN signals direct the modem to enter power down mode, while RINGOUTA and RINGOUTB provide Ring indication signals to the modem, depending on modem type. IDLEN1O and RINGOUTA are used exclusively with RC224ATF modem family cards, while -PWRDWN and RINGOUTB are used with C39 controller-based RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL modem family cards. The different signal pairs are used with the two modem groups due to differing Sleep/Stop Mode control signal level requirements.

Specifically, with the RC224ATF modem family, IDLEN1O connects to the modem's IDLEN1 pin. Enabling Sleep Mode requires that IDLEN1 be LOW, while Stop Mode entry requires that IDLEN1 be HIGH. Additionally, Sleep Mode entry requires that the modem -RING pin be HIGH, while Stop Mode entry requires that this pin be LOW.

On the other hand, with C39 controller-based RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL family modems, -PWRDWN connects to the modem controller's -STPMODE pin. A LOW level directs the modem to enter Stop Mode. Furthermore, the modem controller's -RING pin must be LOW for the modem to enter either Sleep or Stop Modes.

Powering Down

When the host sets the PwrDwn bit in the CCSR, several events occur. First, the modem is provided with the power down request via either IDLEN1O (RC224ATF modem family) or -PWRDWN (C39 controller-based RC96V24AC/ RC14V24AC and RC96ACL/RC144ACL modem families). When the PwrDwn bit is set, IDLEN1O is HIGH and -PWRDWN is LOW.

If the modem is already in the Sleep Mode when the power down request is made, it is first awakened to accept the power down request signal. In order to wake-up the modem, an event is required on the modem's Ring input, accomplished as given below.

RC224ATF Modem Family. The PICA RINGOUTA pin is normally HIGH in the absence of telephone line ringing thus enabling modem Sleep Mode. When the PwrDwn bit is set in the CCSR, the PICA resets RINGOUTA LOW regardless of the state of MRDY. If in Sleep Mode, the falling edge of RINGOUTA causes the modem to wake-up. RINGOUTA remains LOW as long as the PwrDwn bit is set, because the modem requires this to be able to enter Stop Mode.

C39 Controller-based RC96V24AC/ RC14V24AC and RC96ACL/RC144ACL Modem Families. The PICA RINGOUTB pin is normally LOW in the absence of telephone line ringing. When the PwrDwn bit is set in the CCSR, the PICA monitors MRDY. If MRDY is LOW indicating that the modem is in Sleep Mode, RINGOUTB is set HIGH and the positive edge of this signal wakes-up the modem. Once awake, the modem controller sets MRDY HIGH and upon PICA recognition of this, RINGOUTB is reset LOW once more. (Note that the modem controller cannot place itself in Stop Mode if the Ring input is HIGH.)

If the MRDY signal is already HIGH when the PwrDwn bit is set in the CCSR, no action is taken on the RINGOUTB pin because the modem is already awake. The -PWRDWN pin is simply reset LOW to indicate the power down request to the modem.

Ready/-Busy Indication at Power Down. The host must not change the state of the PwrDwn bit while the RRdy/-Bsy bit in the Pin Replacement Register (PRR) is a zero a) when the PwrDwn bit is set, the RRdy/-Bsy bit is immediately reset to a zero to indicate that the modem is busy processing the power down request, or b) once the modem has entered its Stop Mode (as indicated by a HIGH-to-LOW transition on MRDY), the RRdy/-Bsy bit is set to a one.

Modem Chip Select and RINGIN Pass Through. When the PwrDwn bit is set in the CCSR, all accesses to the modem UART interface are blocked. Additionally, the modem will not be awakened by telephone line ringing because pass through of Ring signals on the RINGIN pin is blocked (i.e., RINGOUTA and RINGOUTB remain LOW regardless of the state of the RINGIN input).

Wake-Up From Power Down Mode

When the host requests that the modem resume normal operation by resetting the PwrDwn bit in the CCSR, the modem must be awakened from Stop Mode. This is accomplished by an event on the modem's Ring pin and, as with power down request signals, the method used differs between RC224ATF family modems and C39 controller-based RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL family modems.

RC224ATF Modem Family. When the host resets the PwrDwn bit in the CCSR, RINGOUTA is set HIGH. After a period of about 12 ms (RCIN RC time constant), RINGOUTA is reset LOW again to wake-up the modem. Once the modem is operating normally, the modem sets MRDY HIGH indicating this status. The PICA then sets RINGOUTA HIGH and allows pass through of the RINGIN signal to RINGOUTA.

Once the PwrDwn bit has been reset by the host, -MCS is once again enabled and is asserted for any valid host accesses within the previously configured I/O window. All PICA preserved register configurations established prior to the setting of the PwrDwn bit are reestablished and normal operation is resumed.

C39 Controller-based RC96V24AC/ RC14V24AC and RC96ACL/RC144ACL Modem Families. When the host resets the PwrDwn bit in the CCSR, RINGOUTB is set HIGH. The positive-going edge of this signal wakes-up the modem. Once the modem is operating normally, MRDY is set HIGH indicating this status. When the PICA observes MRDY HIGH, it resets RINGOUTB LOW (i.e., to it's normal operating level) and enables pass through of the signal from RINGIN to RINGOUTB.

When the host resets the PwrDwn bit in the CCSR, the RRdy/-Bsy bit in the PRR is immediately set indicating the busy state. Once the modem is operating normally, as indicated by a LOW-to-HIGH transition on MRDY, the RRdy/-Bsy bit is reset indicating that the modem is ready to receive commands.

The Power Down and Power Up Signal State diagrams for modems in the RC224ATF, and in the C39 controller-based RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL modem families, respectively, are provided in Figures 2 and 3.

Indication of Incoming Ringing During Power Down Mode

While the modem is in a power down mode, an incoming call indication can be passed to the host, in either of two ways, to provide the host with the option of waking-up the modem to answer the call. These mutually exclusive call indication pass through methods are a) using the I/O Event Indication Register (IOEIR), or b) enabling the RingEn bit in the CCSR.

I/O Event Indication Register. The RIEvt bit of the IOEIR is latched to a one upon detection of a RINGIN signal rising edge. The host can poll RIEvt at any time (even during power down mode) because the PICA CCSR interface remains active at all times. [Note that the RIEvt bit gets set to a one by every RINGIN positive edge at the frequency of the incoming Ring signal (i.e., 15 - 68 Hz)].

Furthermore, if the RIEnab bit of the IOEIR is set to a one by the host, the Changed bit in the CCSR is a one whenever the RIEvt bit is a one. If the SigChg bit in the CCSR has also been set to a one, thus enabling indication of state changes on the -STSCHG pin, -STSCHG will also be driven LOW. Once the host has polled the RIEvt bit, it may reset it to a zero by writing a one to it.

RingEn Bit in the CCSR. The Intel ExCA specification provides for host Ring indication using -STSCHG. (Note that while this use of -STSCHG is not recommended, the PICA provides this Ring indication method for those who desire it.)

The RingEn bit in the CCSR is used to enable the Intel ExCA Ring indication function. The RingEn default state of zero disables this function, while -STSCHG becomes a Ring indication signal when the RingEn bit is set to a one by the host.

When the RingEn bit is set to a one, an incoming Ring signal on RINGIN is integrated to smooth the 15 - 68 Hz Ring frequency. During the ringing ON period, -STSCHG is held LOW. During the ringing OFF period and when there is no incoming Ring signal, -STSCHG is held HIGH.

When the RingEn function is enabled, all other state change indications on -STSTCHG are disabled (i.e., the Changed bit in the CCSR will have no effect on the state of -STSCHG regardless of the state of the SigChg bit in the CCSR).

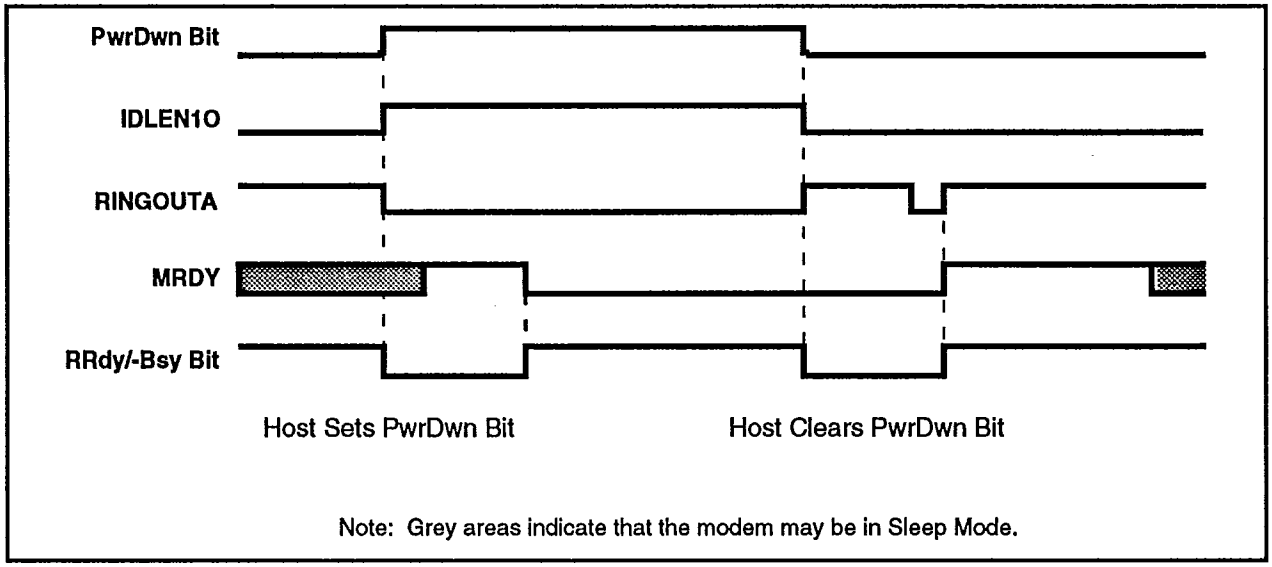


Figure 2. RC224ATF Modem Family Power Down /Up Signal State Diagram

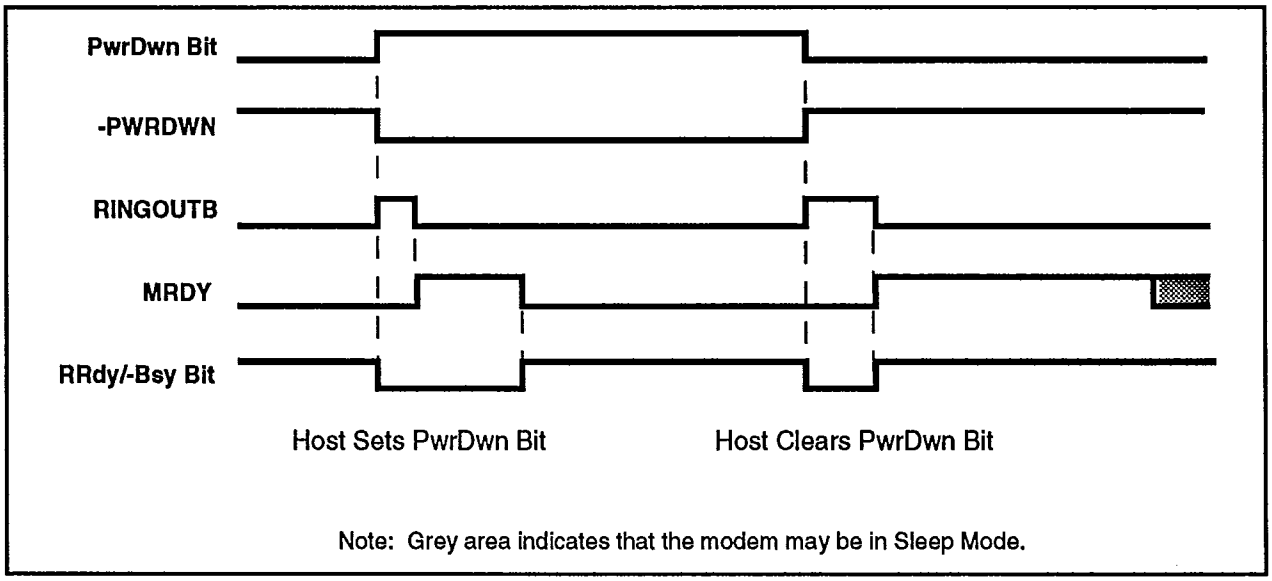


Figure 3. C39 Controller-based RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL Modem Families Power Down/Up Signal State Diagram

RESET LOGIC

The PICA provides a modem reset output signal, -MRES, which can be asserted by three separate methods.

1. **Power up.** When power is applied to the PC Card, -MRES is LOW for a period determined by the RCIN3 RC time constant (approximately 15 ms), at the end of which time, -MRES is HIGH. The PICA registers are in their default (i.e., unconfigured) states.
2. **Hard Reset.** The PCMCIA socket's RESET output is tied to the PICA RESET pin and can be asserted HIGH to reset the PC Card (and PICA). While RESET is HIGH, -MRES is LOW, and when RESET is LOW, -MRES is HIGH.

   Additionally, RESET HIGH resets the PICA and returns all of its registers to their default (i.e., unconfigured) states.
3. **Soft Reset.** SReset in the Configuration and Option Register (COR) provides a method of resetting the PC Card via software. When the host writes a one to SReset, -MRES is asserted LOW and the PICA is placed and held in the reset state. (This is equivalent to assertion of RESET except that the SReset bit is not cleared.) When the host resets SReset to a zero, -MRES is de-asserted HIGH, and the PICA returns to it's default (i.e., unconfigured) state.

Busy Indication During Reset. Following any of the three possible reset methods described above, the PC Card default state is Memory-Only Interface, and the PC Card uses the Memory-Only Interface mode until it is configured by the host as an I/O card.

While in the Memory-Only Interface mode, -IREQ is used as the RDY/BSY signal. After a reset, the modem must not be accessed by the host until it has completed its configuration and self-test routines and is ready to accept commands. The PICA indicates the busy state (corresponding to execution of the configuration, reset, and self-test routines) to the host by asserting pin 56 (-IREQ) LOW. Once the modem is operating normally and ready to accept commands, it sets MRDY HIGH, and the PICA sets pin 56 HIGH.

HARDWARE INTERFACE

Interface Signals

The PICA Block Diagram is provided in Figure 4. The PICA Pin-Out Diagram is provided in Figure 5, while the PICA Pin Signals are listed in Table 1 and described in detail in Table 2.

PICA Electrical Interface Characteristics are provided in Table 3, while Absolute Limits are provided in Table 4.

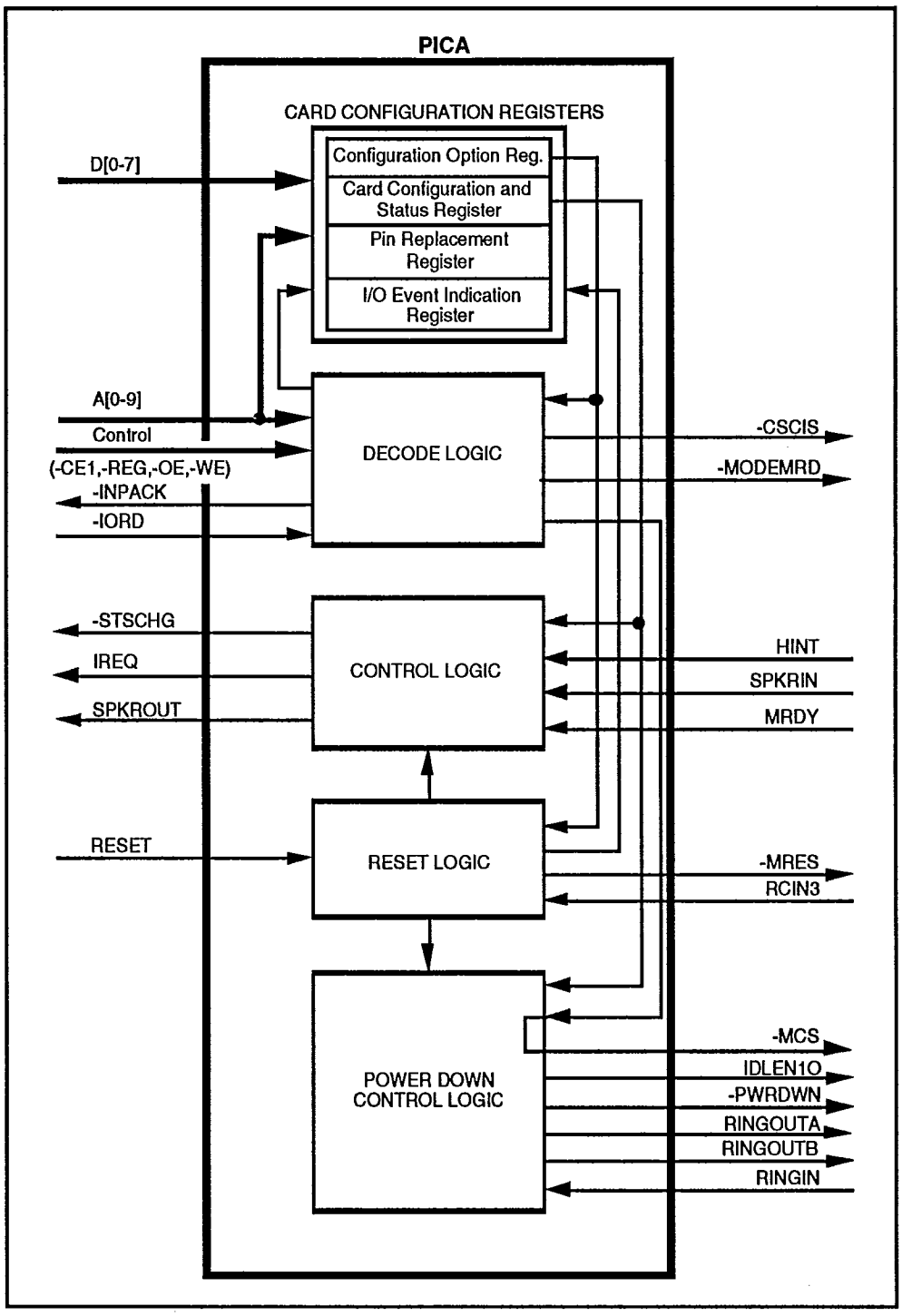


Figure 4. PICA Block Diagram

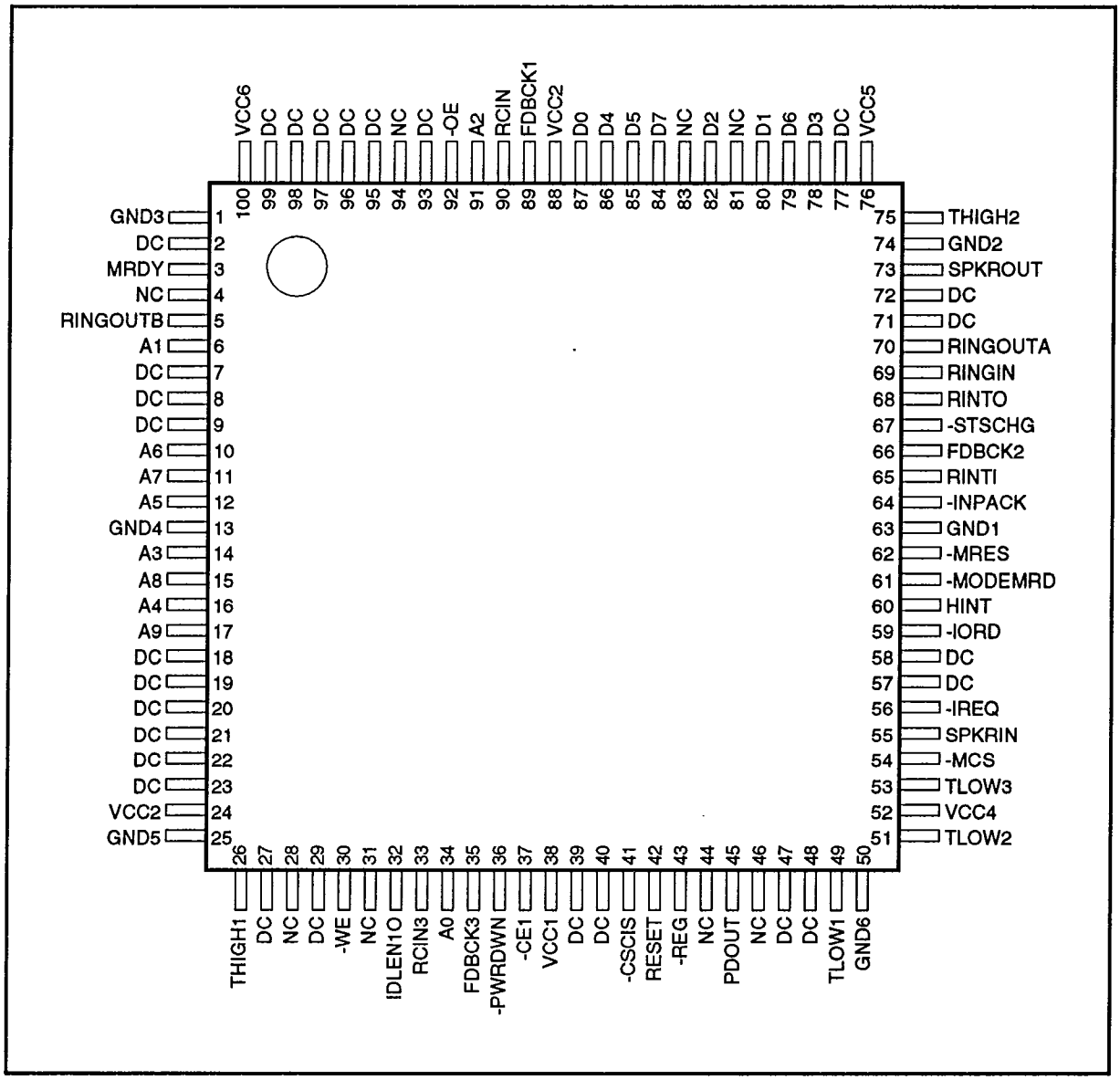


Figure 5. PICA Pin-Out Diagram

Table 1. PICA Pin Signals

Pin Number	Signal Name	I/O Type
1	GND3	GND
2	DC	Note 5
3	MRDY	I
4	NC	Note 6
5	RINGOUTB	O
6	A1	I
7	DC	Note 5
8	DC	Note 5
9	DC	Note 5
10	A6	I
11	A7	I
12	A5	I
13	GND4	GND
14	A3	I
15	A8	I
16	A4	I
17	A9	I
18	DC	Note 5
19	DC	Note 5
20	DC	Note 5
21	DC	Note 5
22	DC	Note 5
23	DC	Note 5
24	VCC3	PWR
25	GND5	GND
26	THIGH1	I (Tie to VCC)
27	DC	Note 5
28	NC	Note 6
29	DC	Note 5
30	-WE	I
31	NC	Note 6
32	IDLEN1O	O (Note 4)
33	RCIN3	I (Note 2)
34	A0	I
35	FDBCK3	O (Note 3)
36	-PWRDWN	O (Note 4)
37	-CE1	I
38	VCC1	PWR
39	DC	Note 5
40	DC	Note 5
41	-CSCIS	O
42	RESET	I
43	-REG	I
44	NC	Note 6
45	PDOUT	O (Tie to RCIN)
46	NC	Note 6
47	DC	Note 5
48	DC	Note 5
49	TLOW1	I (Tie to GND)
50	GND6	GND

Table 1. PICA Pin Signals (Continued)

Pin Number	Signal Name	I/O Type
51	TLOW2	I (Tie to GND)
52	VCC4	PWR
53	TLOW3	I (Tie to GND)
54	-MCS	O
55	SPKRIN	I
56	-IREQ	O
57	DC	Note 5
58	DC	Note 5
59	-IORD	I
60	HINT	I
61	-MODEMRD	O
62	-MRES	O
63	GND1	GND
64	-INPACK	O
65	RINTI	I (Note 1)
66	FDBCK2	O (Note 3)
67	-STSCHG	O
68	RINTO	O (Tie to RINTI)
69	RINGIN	I
70	RINGOUTA	O
71	DC	Note 5
72	DC	Note 5
73	SPKROUT	O
74	GND2	GND
75	THIGH2	I (Tie to VCC)
76	VCC5	PWR
77	DC	Note 5
78	D3	I/O
79	D6	I/O
80	D1	I/O
81	NC	Note 6
82	D2	I/O
83	NC	Note 6
84	D7	I/O
85	D5	I/O
86	D4	I/O
87	D0	I/O
88	VCC2	PWR
89	FDBCK1	O (Note 3)
90	RCIN	I (Note 1)
91	A2	I
92	-OE	I
93	DC	Note 5
94	NC	Note 6
95	DC	Note 5
96	DC	Note 5
97	DC	Note 5
98	DC	Note 5
99	DC	Note 5
100	VCC6	PWR

Notes:

1. Tie to an RC network (R = 1 MΩ and C = 0.1 µF). [See Figure 11.]
2. Tie to an RC network (R = 180 kΩ and C = 0.1 µF) to provide a -MRES signal power-on time constant. [See Figure 11.]
3. Place a 5.1 MΩ resistor between FDBCK1 and RCIN, FDBCK2 and RINTI, and FDBCK3 and RCIN3. [See Figure 11.]
4. Tie IDLEN1O to IDLEN1 in RC224ATF modem designs only, and tie -PWRDWN to -STPMODE in C39 controller-based RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL modem designs only. DON'T connect unused pins.
5. DON'T connect these pins to anything.
6. No Connect (NC). Leave these pins unconnected or tie to any state.

Table 2. Hardware Interface Signal Definitions

Label	I/O Type	Signal Definition
		POWER AND GROUND
VCC	PWR	**+5 VDC Digital Power Supply.** +5V ± 5% is required.
GND	GND	**Ground.**
		PCMCIA BUS CONNECTOR/SOCKET INTERFACE
A0-9	I	**Address lines.** Used for Configuration Register selection, I/O decoding, and Attribute Memory selection.
D0-7	I/O	**Data Bus lines.**
-CE1	I	**Card Enable.** Asserted by the host during an access to an even addressed byte in attribute memory or the configuration registers, and during I/O accesses.
-INPACK	O	**Input Acknowledge.** Asserted by the PICA in response to a valid I/O read access. For an I/O read access to be valid, the Card Configuration Option Register must be properly configured and an I/O read access to the configured address window must occur.
-IORD	I	**I/O Read.** Asserted by the host to read data from the PC-card's I/O space. The -REG and -CE1 signals must also be active for an I/O transfer to take place.
-IREQ	O	**Interrupt Request.** Asserted by the PICA to indicate an interrupt request by the modem's UART function. Additionally, after any of the three possible reset conditions (Power-on reset, soft reset through bit 7 of the Configuration Option Register, or hard reset via the RESET pin), this pin serves as the memory interface RDY/-BSY pin and is held LOW (busy state indication) until a positive edge occurs on the MRDY pin indicating that the modem is ready, at which time this pin is set HIGH (ready state indication).
-OE	I	**Output Enable.** Asserted by the host to enable data out of the Card Configuration Registers or CIS during a memory read.
-REG	I	**Register Select and I/O Enable.** Asserted by the host during an I/O access, attribute memory access, or an access to the configuration registers.
RESET	I	**Card Reset.** Asserted by the host to request a PC Card reset. When asserted, the Card Configuration Option Register is reset, the -MRES output to the modem is asserted, and the PICA is reset. The -MRES line remains asserted and the PICA remains in the reset state until the RESET input is de-asserted.
SPKROUT	O	**Digital Audio Output.** When the Audio bit in the Configuration and Status Register is set to a one, this pin reflects the signal at the SPKRIN input. When the Audio bit is a zero, this pin is three-stated. A 100 kΩ pull-up resistor should be added to this pin.
-STSCHG	O	**Status Changed.** Used to alert the host to changes in the -Rdy/Bsy bit in the Pin Replacement register and to the setting of the RIEvt bit in the I/O Event Indication Register. Optionally, if the RingEn bit in the Card Configuration and Status Register is set, this pin is used for Ring indication to the host as follows: while the input on the RINGIN pin is LOW (no ringing), the -STSCHG pin is held HIGH. While the input on the RINGIN pin is toggling (indicating an incoming ring), the -STSCHG output is low.
-WE	I	**Write Enable.** Asserted by the host to strobe write data during a write to attribute memory or the configuration registers.
		DAA INTERFACE
RINGIN	I	**Ring Input.** This signal is input from the DAA's Ring detect circuit, usually an opto isolator output. This input should be LOW while there is no ringing.
		CIS MEMORY INTERFACE
-CSCIS	O	**CIS Memory Chip Select.** This chip select output is used to enable access to the memory device holding the CIS information, and is active whenever the host generates an even address to attribute memory in the range 0-1FFh.

Table 2. Hardware Interface Signal Definitions (Continued)

Label	I/O Type	Signal Definition
		MODEM INTERFACE
HINT	I	**Host Interrupt Request.** This input signal from the modem is inverted and passed through to the PICA -IREQ output pin. When this input is set HIGH by the modem's 16450/16550A interface to indicate an interrupt request, the -IREQ signal is asserted LOW.
IDLEN1O	O	**IDLEN1 Out.** This signal reflects the state of the PwrDwn bit in the Card Configuration and Status Register. A HIGH state indicates that the PwrDwn bit has been set by the host and that the modem should enter the Stop Mode. **Note:** This pin is tied to the IDLEN1 pin in RC224ATF modem family designs, and is NOT used with C39 controller-based RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL family modems.
-MCS	O	**Modem Chip Select.** This decoded chip select output signal ties to the modem -HCS pin. This signal is asserted whenever a valid address is presented to the PICA (i.e., falling within the I/O window selected via the configuration index bits of the Configuration Option Register). If no valid index has been written to these bits, this signal remains HIGH. Also, if the PwrDwn bit has been set in the Configuration and Status Register, the modem chip select signal is invalid, and remains HIGH.
-MODEMRD	O	**Modem Read.** This signal is to be tied to the modem -HRD input and is the buffered -IORD input.
MRDY	I	**Modem Ready.** MRDY LOW indicates that the modem is busy initializing the modem after a reset (power-on, soft reset, or hard reset), is in the Sleep Mode, or is in Stop Mode. The modem sets MRDY HIGH after it has initialized the system following a reset or after it has powered up from one of the low power modes and is ready to accept commands over the host bus interface.
-MRES	O	**Modem Reset.** This signal ties to the reset pins of both the modem controller and data pump, and is asserted during one of three conditions: 1. At PC Card power on until the RC time constant on RCIN3 has timed out, 2. While the PC Card RESET signal is asserted, or 3. While the SReset bit in the Configuration Option Register is set to a one.
-PWRDWN	O	**Power Down.** This pin reflects the inverse state of the Card Configuration and Status Register PwrDwn bit. A LOW state indicates that the PwrDwn bit has been set by the host and that the modem should enter the Stop Mode. **Note:** This pin is tied to the modem -STPMODE pin in C39 controller-based RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL family modems, and is NOT used with RC224ATF family modems.
RINGOUTA	O	**Ring Output A.** This is the Ring output signal for the RC224ATF modem family, and ties to the RC224ATF -RING pin. When there is no ringing on the RINGIN pin and the PwrDwn bit in the Configuration and Status Register is a zero, this output signal is HIGH allowing the RC224ATF to enter the Sleep Mode during periods of inactivity. During ringing, this signal directly reflects the inverse of the input at the RINGIN pin. When the PwrDwn bit is set, Ring signal pass through is blocked and this signal is reset LOW to allow the RC224ATF to enter Stop Mode. (For additional information on the behavior of this pin see POWER DOWN MODE CONTROL in Section 1). **Note:** This pin is NOT used with RC96V24AC/ RC14V24AC and RC96ACL/ RC144ACL family modems.
RINGOUTB	O	**Ring Output B.** This is the Ring signal output for the RC96V24AC/ RC14V24AC and R96ACL/ RC144ACL modem families, used instead of RINGOUTA (RC224ATF). This signal ties to the Ring signal input pins of both the modem controller and data pump. As long as the PwrDwn bit in the Configuration and Status Register is a zero, this signal directly reflects the RINGIN signal. (For additional information on the behavior of this pin, see POWER DOWN MODE CONTROL in Section 1). **Note:** This pin is NOT used with RC224ATF family modems.
		AUDIO ADC INTERFACE
SPKRIN	I	**Digitized Speaker Input.** The input signal to this pin should be a digitized audio signal. This signal is passed through to the SPKROUT pin whenever the Audio bit in the Configuration and Status Register is set to a one. If not used, this signal should be tied HIGH.

Table 3. Electrical Interface Characteristics

Characteristic	Symbol	Min.	Max.	Units	Conditions
Supply Voltage	V_{CC}	+4.75	+5.25	V	0°C to 70°C
Input High Voltage	V_{IH}	$0.7V_{CC}$	$1.0V_{CC}$	V	
Input Low Voltage	V_{IL}	0	$0.2V_{CC}$	V	
Output High Voltage	V_{OH}	+3.86	-	V	I_{OH} = –4.0 ma
Output Low Voltage	V_{OL}	-	+0.32	V	I_{OL} = +4.0 ma
Input Leakage Current	I_I	–10	+10	µA	V_{IN} = 0 V to V_{CC}
Quiescent Power Supply Current	I_{CCO}	-	+5	mA	V_{CC} = V_{CC}–max.

Table 4. Absolute Limits

Characteristic	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-0.5	+7.0	V
Input Voltage	V_{IN}	-0.5	V_{CC}+0.5	V
Voltage applied to three-state output	V_{TS}	-0.5	V_{CC}+0.5	V
Storage temperature (ambient)	T_{STG}	-65	+150	°C
Maximum soldering temperature (10 sec @ 1/16 in.)	T_{SOL}	-	+260	°C
Junction temperature plastic	T_J	-	+125	°C

MEMORY SPACE INTERFACE

The PICA provides two of the memory space types specified for the PCMCIA Release 2.0 Socket; Attribute Memory and I/O Address Space (i.e., Common Memory Space is not used).

Attribute Memory Card Configuration Registers

The CIS table resides in the attribute memory range 000h-1FFh as shown in Table 5, while the four card configuration registers reside in the attribute memory range 200h-208h as shown in Table 6. Tables 7a - 7d describe the functionality of the individual register bits.

Attribute Memory Decode Logic. Attribute memory contains both the Card Information Structure (CIS) table and card configuration registers, and is directly addressable (even only) by the host via the PICA address decoding logic summarized in Table 8.

Configuration Option Register. The Configuration Option Register is used to configure the PICA. This register also provides the host with a soft reset capability.

Card Configuration and Status Register. The Card Configuration and Status Register provides PC Card status information, modem service requests, host control of PICA digital audio and DAA Ring indicate signal pass through, and PC Card power down mode.

Pin Replacement Register. The Pin Replacement Register provides PC card ready/busy indication status.

I/O Event Indication Register. The I/O Event Indication Register provides Ring indication status, and host control of Ring indication pass through to the changed bit in the CCSR.

I/O Address Space Decode Logic

When the host accesses the PC Card's I/O Address Space, the PICA decodes the address lines as shown in Table 9, and asserts the Modem Chip Select (-MCS) based on the Configuration Index which has been written to the Configuration and Option Register.

Table 5. Attribute Memory Map

Address (Hex)	Allocation
(TOP) • • 210	Unused Attribute Memory
208 • • 200	Card Configuration Registers
1FF • • 000	CIS

Table 6. PICA Registers Bit Map

Memory Function	Address (Hex)	Bit								Default Value
		7	6	5	4	3	2	1	0	
I/O Event Indication Register (IOEIR)	208	0	0	0	RIEvt	0	0	0	RIEnab	00h
(Unused)	206									
Pin Replacement Register (PRR)	204	0	0	CRdy/-Bsy	0	0	0	RRdy/-Bsy	0	00h
Card Configuration and Status[1] Register (CCSR)	202	Changed	SigChg	0	RingEn	Audio	PwrDwn	Intr	0	00h
Configuration Option[2] Register (COR)	200	SReset	0	Configuration Index						00h

Notes: 1. All bits can be read by the host, and bits 2-4 and 6 can be written by the host.
2. This register can be read and written by the host.

Table 7a. I/O Event Indication Register (IOEIR)

Mnemonic	Memory Location	Name/Description
RIEvt	208:4	This bit is latched to a one at the start of each ring frequency cycle to indicate the presence of telephone line ringing (i.e. Ring is HIGH). When both this bit and RIEnab are set to a one, the Changed Bit in the Card Configuration and Status Register (CCSR) is also set to a one. If, in addition, the SigChg bit in that register has also been set by the host, the -STSCHG pin will be LOW. Host writing of a one to this bit resets it, while host writing of a zero to this bit has no effect on it.
RIEnab	208:0	Setting this bit to a one enables the setting of the CCSR Changed bit when the RIEvt bit is set. When this bit is reset to a zero, this feature is disabled. The RIEvt bit is not affected by resetting this bit.

Table 7b. Pin Replacement Register (PRR)

Mnemonic	Memory Location	Name/Description
CRdy/-Bsy	204:5	This bit is set to a one when the bit RRdy/-Bsy changes state, and may also be written by the host if a one is simultaneously written to bit 1 of this register (i.e., the Pin Replacement Register).
RRdy/-Bsy	204:1	When read, this bit represents the internal state of the Ready/-Busy signal. When written, this bit acts as a mask for writing the CRdy/-Bsy bit on that write cycle (e.g., to write a one to bit 5, the host writes 22h to this register, and to reset bit 5 to a zero, the host writes 02h to this register).

Table 7c. Card Configuration and Status Register (CCSR)

Mnemonic	Memory Location	Name/Description
Changed	202:7	This bit is the logical OR of the Crdy/-Bsy and RIEvt bit states. When the SigChg bit is a one and the RingEn bit is a zero, the -STSCHG pin is LOW whenever the Changed bit is a one.
SigChg	202:6	This bit is set/reset by the host to enable/disable a state-changed signal from the status register. When this bit is set to a one and the RingEn bit is a zero, the Changed bit controls -STSCHG. If both the SigChg bit and the RingEn bit are reset to a zero, then -STSCHG is always held HIGH.
RingEn	202:4	This bit is set/reset by the host to enable/disable a Ring indication signal on -STSCHG. When this bit is a zero, the state of -STSCHG is controlled by the SigChg and Changed bits in the CCSR. When the RingEn bit is set to a one, -STSCHG is used solely to indicate the state of the integrated Ring signal. In this mode, -STSCHG is held LOW while there is ringing present at the RINGIN pin, and -STSCHG is held HIGH when no ringing is present.
Audio	202:3	This bit is set/reset by the host to enable/disable pass through of the digital audio signal from SPKRIN to SPKROUT. When this bit is a zero, SPKROUT is three-stated. When this bit is set to a one, the SPKRIN signal is passed through to the SPKROUT pin.
PwrDwn	202:2	This bit is set to a one by the host to request that the PC Card enter a power-down state, and corresponds to modem Stop Mode. When the PwrDwn bit is set, all I/O accesses to the modem are disabled by keeping the -MCS pin HIGH, and pass through of the RINGIN signal to the RINGOUTA and RINGOUTB pins is blocked. When the PwrDwn bit is reset by the host, the modem controller is awakened by a pulse on RINGOUTA or RINGOUTB as appropriate, I/O accesses are allowed, and the RINGIN signal is passed through to the RINGOUTA pin or RINGOUTB pin.
Intr	202:1	This bit is read only and is the inverted HINTIN signal coming from the modem's UART interface (i.e., HINT). This bit is set to a one to indicate an interrupt condition and remains set until the condition which caused the interrupt request has been serviced.

Table 7d. Configuration Option Register (COR)

Mnemonic	Memory Location	Name/Description
SReset	200:7	When this bit is set to a one, the PICA is placed in the reset state and -MRES is reset LOW (this is the same as if the RESET pin were asserted, except that this bit is not reset). Returning this bit to a zero leaves the PICA in the same unconfigured reset state as following a power-up or hardware reset, and deasserts -MRES. This bit is reset to a zero by power up and hardware reset.
Configuration Index	200:0-5	The value written to these bits determines the I/O address range for which -MCS is asserted. The address range is determined by decoding the host address lines A3-A9 as follows:

Index Value						Chip Select Address Range
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	x	x	x	x	x	Chip selects are disabled
1	0	x	x	0	0	3F8h to 3FFh
1	0	x	x	0	1	2F8h to 2FFh
1	0	x	x	1	0	3E8h to 3EFh
1	0	x	x	1	1	2E8h to 2EFh
1	1	x	x	x	x	-MCS is asserted for all I/O cycles (i.e. address lines A3 - A9 are not decoded)

Note: The index value with bit 4 set to a one corresponds to Independent I/O Address Window mode, in which the -MCS pin is asserted for any valid I/O cycle (i.e., -CE1 and -REG LOW), and the host is responsible for providing address decoding to prevent conflicts with other installed devices. If bit 5 is a zero, all I/O accesses are disabled and -MCS is always held HIGH.

Table 8. Attribute Memory Address Space Decoding

-CE1	-REG	-OE	-WE	A9 - A1	A0	Selected Register
H	X	X	X	X	X	Standby
L	H	X	X	X	X	Common memory access (Not supported by PICA)
L	L	X	X	X	H	Invalid access
L	L	L	H	0-1FFh	L	Card Information Structure read (-CSCIS asserted)
L	L	H	L	0-1FFh	L	Card Information Structure write (-CSCIS asserted)
L	L	L	H	200h		Configuration Option Register read
L	L	H	L	200h		Configuration Option Register write
L	L	L	H	202h		Card Configuration and Status Register read
L	L	H	L	202h		Card Configuration and Status Register write
L	L	L	H	204h		Pin Replacement Register read
L	L	H	L	204h		Pin Replacement Register write
L	L	L	H	208h		I/O Event Indication Register read
L	L	H	L	208h		I/O Event Indication Register write
Notation Key: L = LOW, H = HIGH, and X = don't care.						

Table 9. I/O Address Space Decoding

-CE1	-REG	-IORD	-IOWR	Selected Action
H	X	X	X	Standby
L	L	L	H	I/O read
L	L	H	L	I/O write
Notation Key: L = LOW, H = HIGH, and X = don't care.				

Attribute Memory Timing Requirements

The following conditions apply for all timing descriptions:

1. VDD = +5.0 ± 5% V.
2. Data bus output load = 100 pF, 470 µA sink, 170 µA source.
3. -INPACK, -IREQ, , -STSCHG, -CSCIS output load = 50 pF, 400 µA sink, 100 µA source.

Attribute Memory Timing Diagrams and Parameters

The CIS Memory Chip Select (-CSCIS) Timing Diagram is illustrated in Figure 6, and the associated timing parameters are listed in Table 10.

The Card Configuration Register Read Timing Diagram is found in Figure 7, and the associated timing parameters are found in Table 11.

The Card Configuration Register Write Timing Diagram is found in Figure 8, and the associated timing parameters are found in Table 12.

The I/O Read Timing Diagram is found in Figure 9, and the associated timing parameters are found in Table 13.

The I/O Write Timing Diagram is found in Figure 10, and the associated timing parameters are found in Table 14.

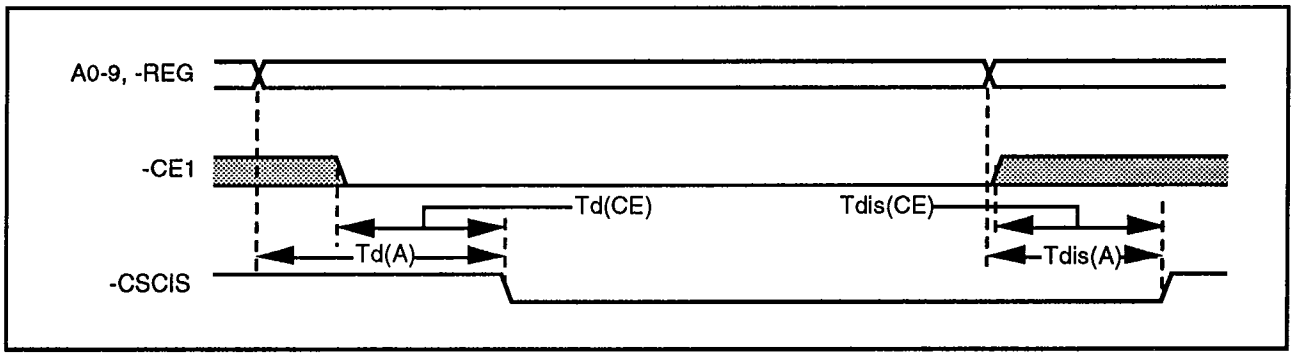


Figure 6. CIS Memory Chip Select (-CSCIS) Timing Diagram

Table 10 -CSCIS Timing Parameters

Parameter	Symbol	Min	Max	Units
Address valid to -CSCIS valid delay	Td(A)	-	50	ns
-CE1 valid to -CSCIS valid delay	Td(CE)	-	50	ns
Address invalid to -CSCIS disabled delay	Tdis(A)	-	50	ns
-CE1 invalid to -CSCIS disabled delay	Tdis(CE)	-	50	ns

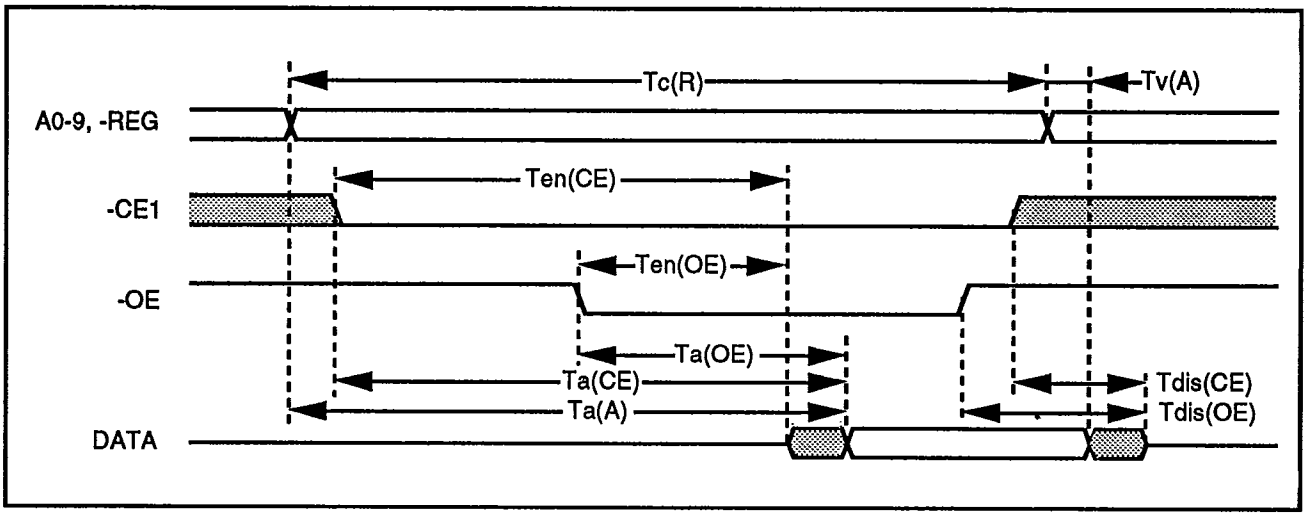


Figure 7. Card Configuration Register Read Timing Diagram

Table 11. Card Configuration Register Read Timing Parameters

Parameter	Symbol	Min	Max	Units
Read cycle time	Tc(R)	300	-	ns
Address access time	Ta(A)	-	300	ns
Card Enable access time	Ta(CE)	-	300	ns
Output Enable access time	Ta(OE)	-	150	ns
Output disable time from -CE1 HIGH	Tdis(CE)	-	100	ns
Output disable time from -OE HIGH	Tdis(OE)	-	100	ns
Output enable time from -CE1 LOW	Ten(CE)	5	-	ns
Output enable time from -OE LOW	Ten(OE)	5	-	ns
Data valid from address change	Tv(A)	-	0	ns

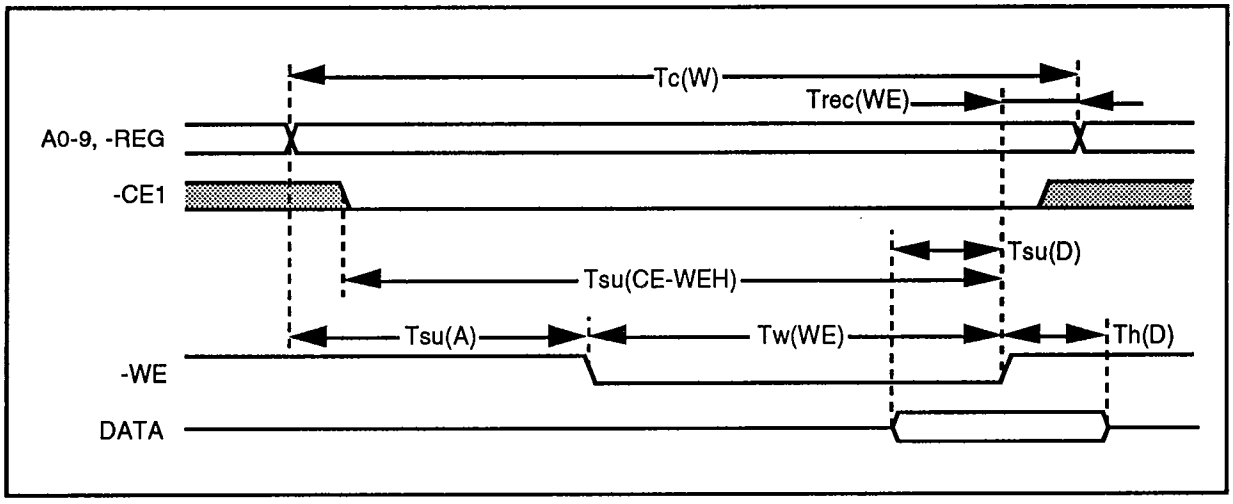


Figure 8. Card Configuration Register Write Timing Diagram

Table 12. Card Configuration Register Write Timing Parameters

Parameter	Symbol	Min	Max	Units
Write cycle time	Tc(W)	250	-	ns
-WE pulse width	Tw(WE)	150	-	ns
Address, -REG setup time	Tsu(A)	30	-	ns
-CE1 LOW to -WE HIGH setup time	Tsu(CE-WEH)	180	-	ns
Data setup time	Tsu(D)	80	-	ns
Data hold time	Th(D)	30	-	ns
Write recover time	Trec(WE)	30	-	ns

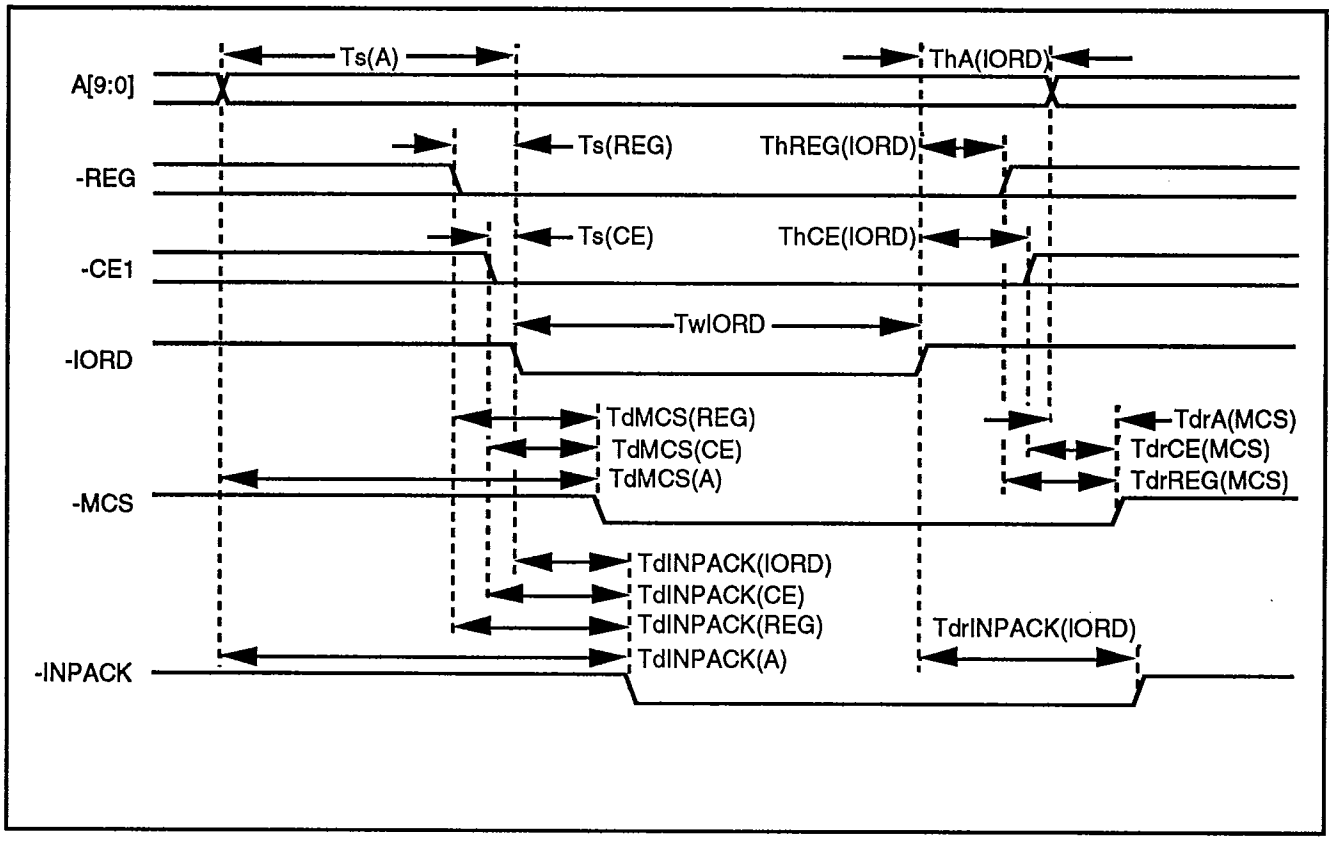


Figure 9. I/O Read Timing Diagram

Table 13. I/O Read Timing Parameters

Parameter	Symbol	Min	Max	Units
Address setup before -IORD	Ts(A)	70	-	ns
-CE1 setup before -IORD	Ts(CE)	5	-	ns
-REG setup before -IORD	Ts(REG)	5	-	ns
-IORD LOW width	Tw(IORD)	165	-	ns
Address hold following -IORD	ThA(IORD)	20	-	ns
-CE1 hold following -IORD	ThCE(IORD)	20	-	ns
-REG hold following -IORD	ThREG(IORD)	0	-	ns
Address valid to -MCS LOW delay	TdMCS(A)	-	100	ns
-CE1 LOW to -MCS LOW delay	TdMCS(CE)	-	40	ns
-REG LOW to -MCS LOW delay	TdMCS(REG)	-	40	ns
Address valid to -INPACK delay	TdINPACK(A)	-	115	ns
-CE1 LOW to -INPACK LOW delay	TdINPACK(CE)	-	50	ns
-REG LOW to -INPACK LOW delay	TdINPACK(REG)	-	50	ns
-IORD LOW to -INPACK LOW delay	TdINPACK(IORD)	0	45	ns
Address invalid to -MCS rising	TdrA(MCS)	-	100	ns
-CE1 HIGH to -MCS rising	TdrCE(MCS)	-	40	ns
-REG HIGH to -MCS rising	TdrREG(MCS)	-	40	ns
-IORD HIGH to -INPACK rising	TdrINPACK(IORD)	-	45	ns

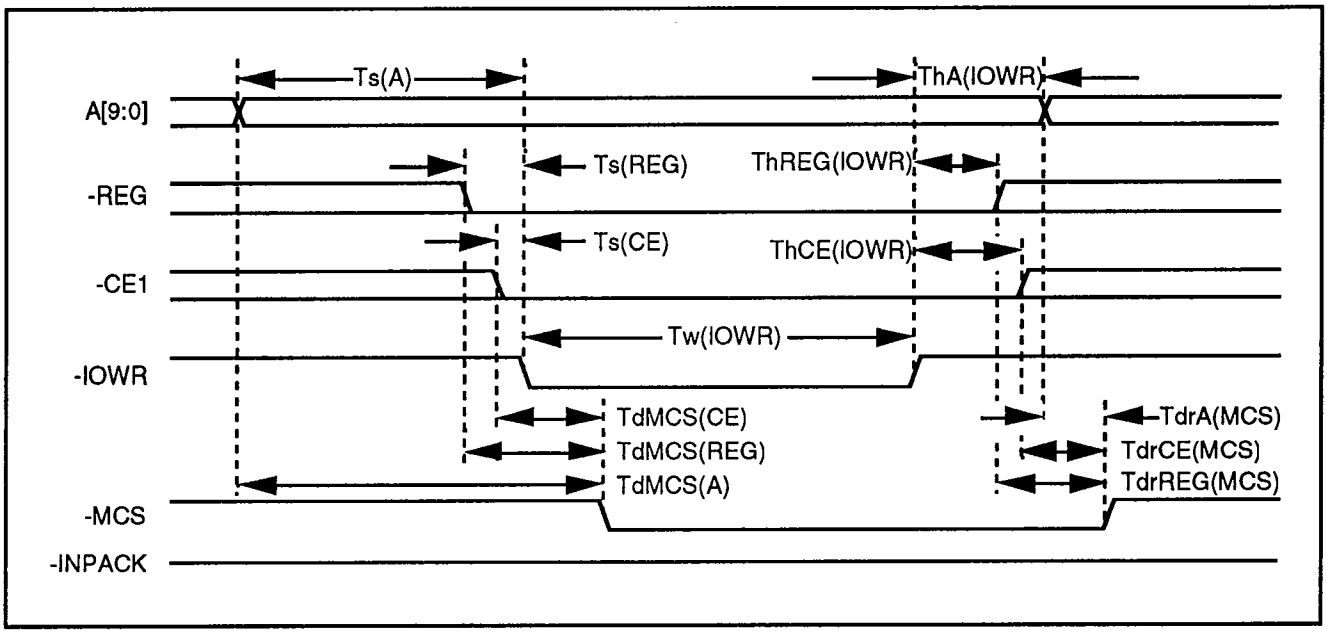


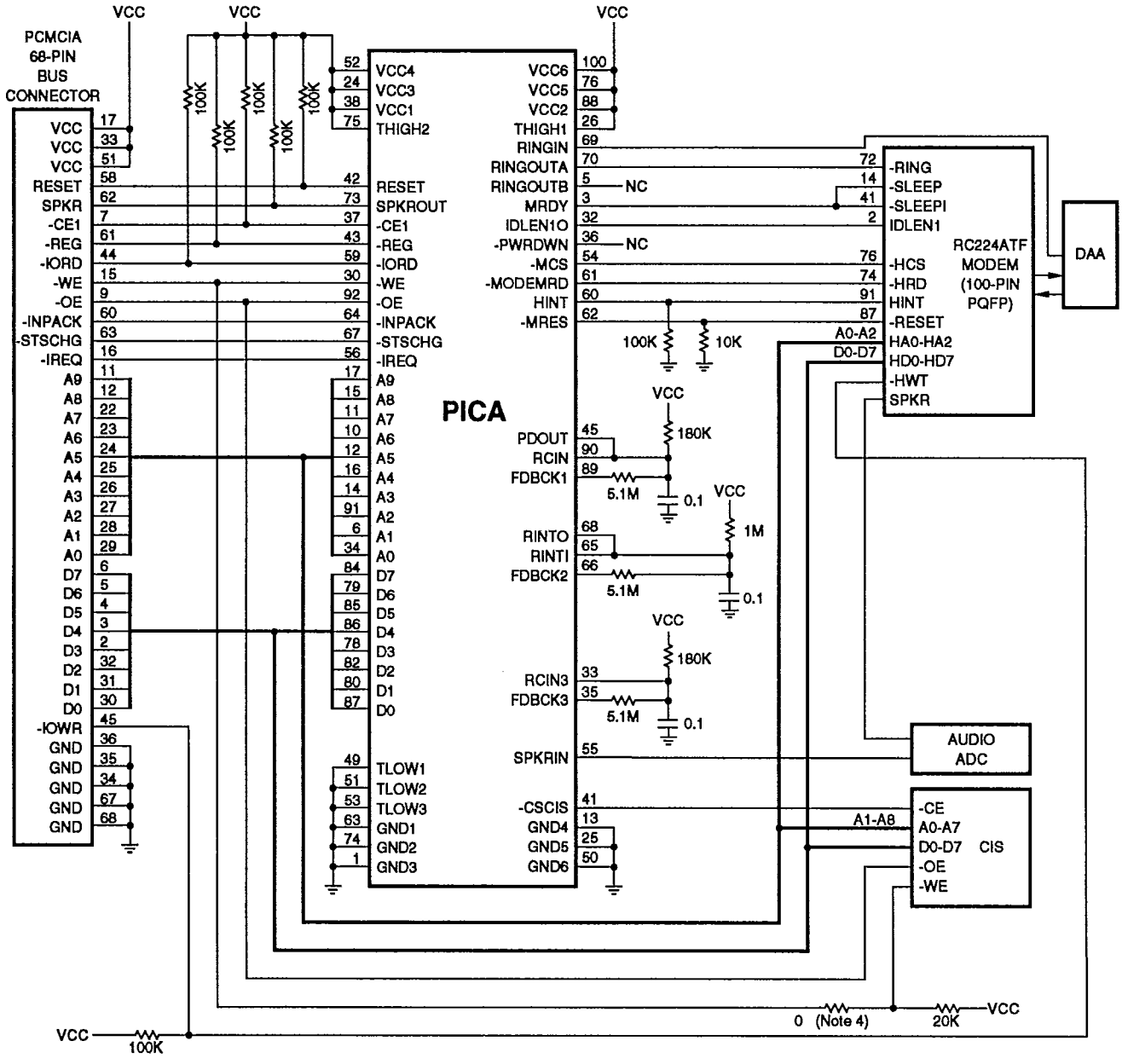
Figure 10. I/O Write Timing Diagram

Table 14. I/O Write Timing Parameters

Parameter	Symbol	Min	Max	Units
Address setup before -IOWR LOW	Ts(A)	60	-	ns
-CE1 setup before -IOWR LOW	Ts(CE)	5	-	ns
-REG setup before -IOWR LOW	Ts(REG)	5	-	ns
-IOWR LOW width	Tw(IOWR)	165	-	ns
Address hold following -IOWR HIGH	ThA(IOWR)	20	-	ns
-CE1 hold following -IOWR HIGH	ThCE(IOWR)	20	-	ns
-REG hold following -IOWR HIGH	ThREG(IOWR)	0	-	ns
Address valid to -MCS LOW delay	TdMCS(A)	-	100	ns
-CE1 LOW to -MCS LOW delay	TdMCS(CE)	-	40	ns
-REG LOW to -MCS LOW delay	TdMCS(REG)	-	40	ns
Address invalid to -MCS rising	TdrA(MCS)	-	100	ns
-CE1 HIGH to -MCS rising	TdrCE(MCS)	-	40	ns
-REG HIGH to -MCS rising	TdrREG(MCS)	-	40	ns

PICA DESIGN SCHEMATICS

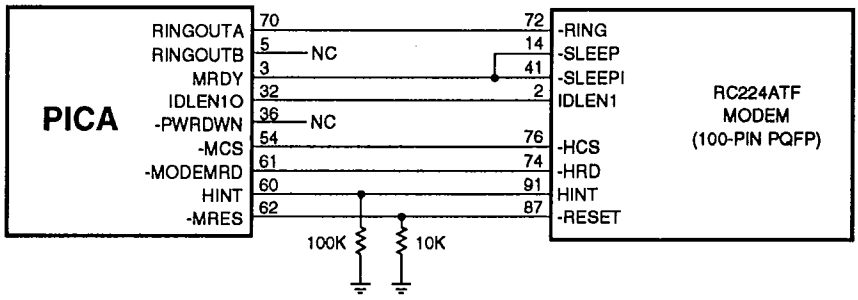
A PICA design schematic supporting a Rockwell RC224ATF family modem is provided in Figure 11, and the PICA/modem-specific interface diagram is provided in Figure 12.



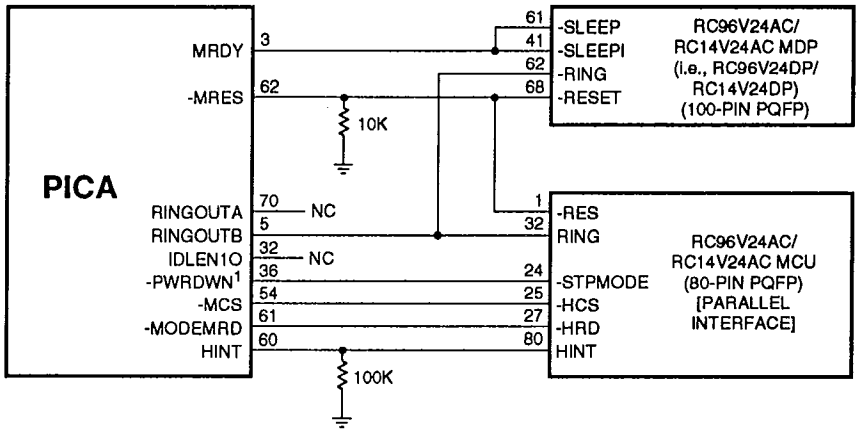
NOTES:

1. COMPONENT TOLERANCES AND RATINGS (UNLESS OTHERWISE NOTED): RESISTOR VALUES IN OHMS, 5%, 1/10W; CAPACITOR VALUES IN µF, 20%, 50V.
2. PICA DON'T CONNECT (DC) PINS (MUST NOT BE CONNECTED): 2, 7-9, 18-23, 27, 29, 32, 39-40, 47-48, 57-58, 71-72, 77, 93, 95-99.
3. PICA NO CONNECTION (NC) PINS (MAY BE LEFT UNCONNECTED OR TIED TO ANY STATE): 4, 28, 31, 44, 46, 83, 94.
4. INSTALL A 0 OHM RESISTOR FOR DEVELOPMENT, BUT REMOVE FOR PRODUCTION.

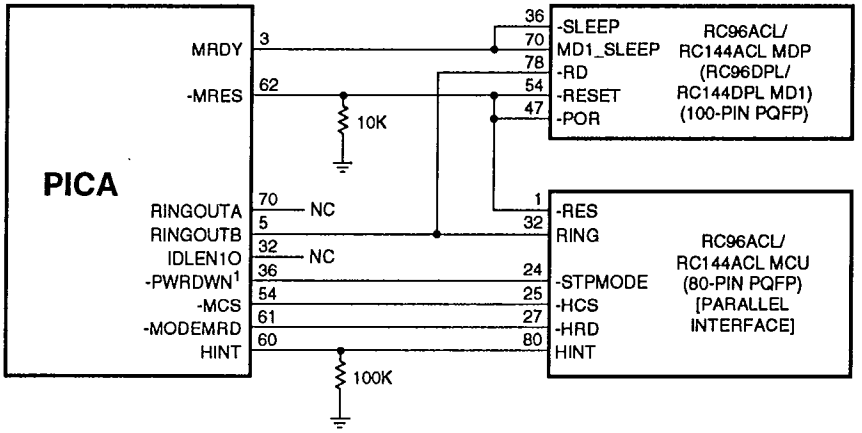
Figure 11. PICA RC224ATF-Modem Family Design Schematic



a. PICA to RC224ATF Modem Interface



b. PICA to RC96V24AC/RC14V24AC Modem Interface



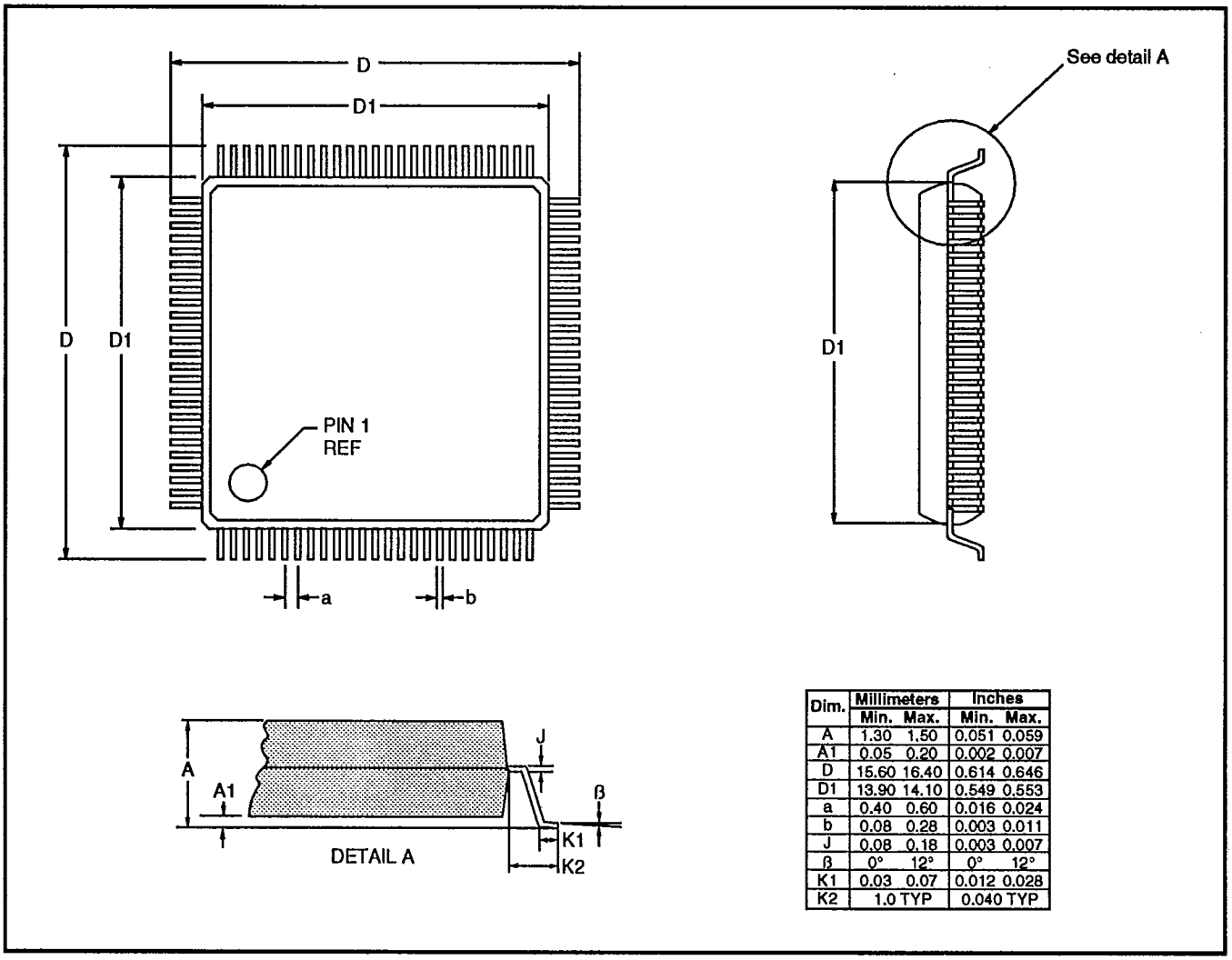
c. PICA to RC96ACL/RC144ACL Modem Interface

Note: 1. The -PWRDWN pin can be connected to C29 controller-based modem -STPMODE, however Power Down Mode control is not provided.

Figure 12. PICA/Modem-Specific Interface Diagram

MODULE DIMENSIONS

The dimensions of the Rockwell PICA industry-standard 100-pin Ultra-Thin Quad Flat Package (TQFP) are illustrated in Figure 13.



Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.30	1.50	0.051	0.059
A1	0.05	0.20	0.002	0.007
D	15.60	16.40	0.614	0.646
D1	13.90	14.10	0.549	0.553
a	0.40	0.60	0.016	0.024
b	0.08	0.28	0.003	0.011
J	0.08	0.18	0.003	0.007
β	0°	12°	0°	12°
K1	0.03	0.07	0.012	0.028
K2	1.0 TYP		0.040 TYP	

Figure 13. PICA 100-Pin TQFP Dimensions