Rockwell

R6522
Versatile Interface Adapter (VIA)

DESCRIPTION

The R6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bidirectional data transfers between VIA's in multiple processor systems.

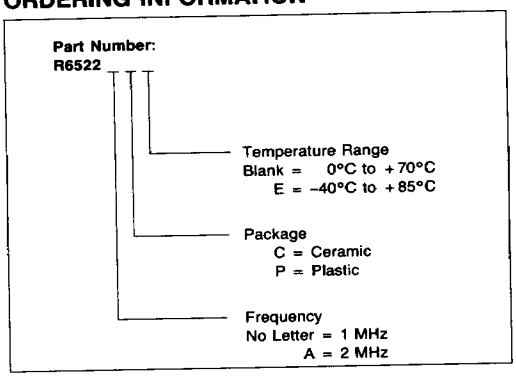
The R6522 includes functions for programmed control of up to two peripheral devices (Ports A and B). These two program controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral units. Each port has input data latching capability. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on an individual line basis.

The R6522 also has two programmable 16-bit Interval Timer/Counters with latches. Timer 1 may be operated in a One-Shot Interrupt Mode with interrupts on each count-to-zero, or in a Free-Run Mode with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register. Application versatility is further increased by various control registers, including—the Interrupt Flag Register, the Interrupt Enable Register, the Auxiliary Control Register and the Peripheral Control Register.

FEATURES

- Two 8-bit bidirectional I/O ports
- Two 16-bit programmable timer/counters
- Serial bidirectional peripheral I/O
- TTL compatible peripheral control lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices.
- Latched output and input registers on both I/O ports
- 1 and 2 MHz operation
- Commercial and industrial temperature range versions
- Single +5 Vdc power requirement

ORDERING INFORMATION



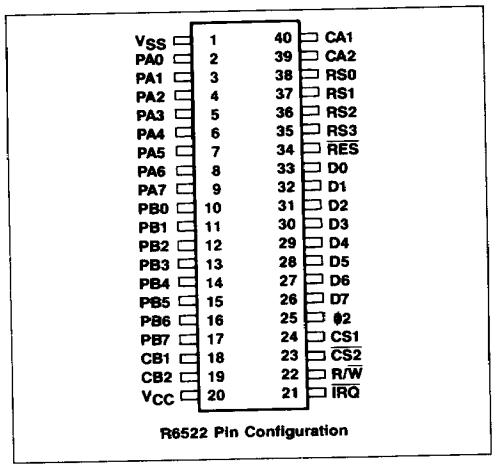


Figure 1. R6522 Pin Assignments

INTERFACE SIGNALS

Figure 1 (on the front page) shows the R6522 VIA pin assignments and Figure 2 groups the signals by functional interface.

RESET ($\overline{RES}$)

Reset ($\overline{RES}$) clears all internal registers (except T1 and T2 counters and latches, and the Shift Register (SR)). In the $\overline{RES}$ condition, all peripheral interface lines (PA and PB) are placed in the input state. Also, the Timers (T1 and T2), SR and interrupt logic are disabled from operation.

INPUT CLOCK (PHASE 2)

The system Phase 2 (Ø2) Input Clock controls all data transfers between the R6522 and the microprocessor.

READ/WRITE (R/$\overline{W}$)

The direction of the data transfers between the R6522 and the system processor is controlled by the R/$\overline{W}$ line in conjunction with the CS1 and $\overline{CS2}$ inputs. When R/$\overline{W}$ is low (write operation) and the R6522 is selected, data is transferred from the processor bus into the selected R6522 register. When R/$\overline{W}$ is high (read operation) and the R6522 is selected, data is transferred from the selected R6522 register to the processor bus.

DATA BUS (D0–D7)

The eight bidirectional Data Bus lines transfer data between the R6522 and the microprocessor. During a read operation, the contents of the selected R6522 internal register are transferred to the microprocessor via the Data Bus lines. During a write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to a selected R6522 register. The Data Bus lines are in the high impedance state when the R6522 is unselected.

CHIP SELECTS (CS1, $\overline{CS2}$)

Normally, the two chip select lines are connected to the microprocessor address lines. This connection may be direct or through decoding. To access a selected R6522 register, CS1 must be high (logic 1) and $\overline{CS2}$ must be low (logic 0).

REGISTER SELECTS (RS0–RS3)

The Register Select inputs allow the microprocessor to select one of 16 internal registers within the R6522. Refer to Table 1 for Register Select coding and a functional description.

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INTERRUPT REQUEST ($\overline{IRQ}$)

The Interrupt Request ($\overline{IRQ}$) output signal is generated whenever an internal Interrupt Flag bit is set and the corresponding Interrupt Enable bit is a Logic 1. The Interrupt Request output is an

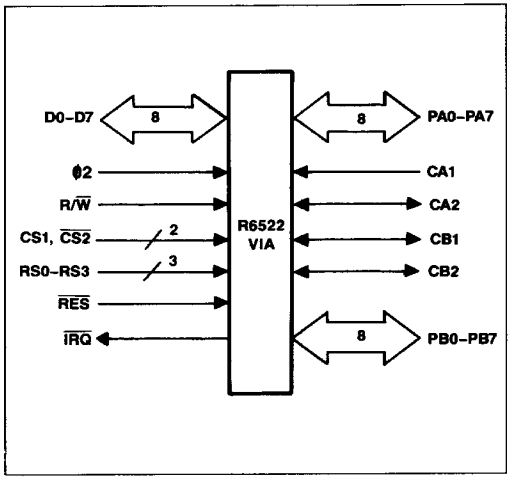


Figure 2. R6522 VIA Interface Signals

open-drain configuration, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

PORT A DATA LINES (PA0–PA7)

Peripheral Data Port A is an 8-line, bidirectional bus for the transfer of data, control and status information between the R6522 and a peripheral device. Each Peripheral Data Port bus line may be individually programmed as either an input or output under control of a Data Direction Register. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. When a "0" is written to any bit position of the Data Direction Register, the corresponding line will be programmed as an input. When a "1" is written into any bit position of the register, the corresponding data line will serve as an output. Polarity of the data output is determined by the Output Register, while input data may be latched into the Input Register under control of the CA1 line. All modes are program controlled by the microprocessor by way of the R6522's internal control registers. Each Peripheral Data Port line represents one TTL load in the input mode and will drive one standard TTL load in the output mode. A typical output circuit for Peripheral Data Port A is shown in Figure 3.

PORT A CONTROL LINES (CA1, CA2)

Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.

PORT B DATA LINES (PB0–PB7)

Peripheral Data Port B is an 8-line, bidirectional bus which is controlled by an Output Register, Input Register and Data Direction Register in a manner much the same as Data Port A. With respect to Port B, the output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on the PB6 line. Port B lines represent one standard TTL load in the input mode and will drive one TTL load in the output mode. Port B lines are also capable of sourcing 1.0 mA at 1.5 Vdc in the output mode. This allows the outputs to directly drive Darlington transistor circuits. A typical output circuit for Port B is shown in Figure 3.

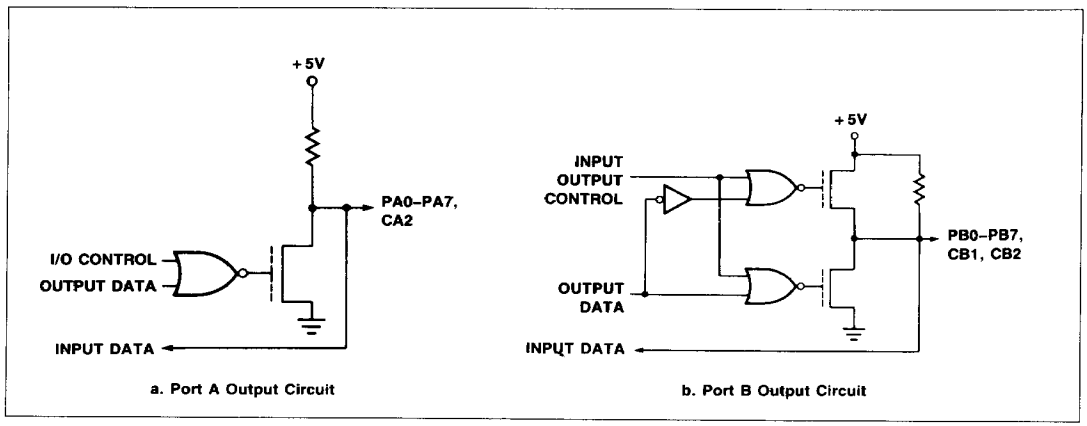
PORT B CONTROL LINES (CB1, CB2)

Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two control lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. Similar to CA1, CB1 controls the latching of input data on Port B. These lines also serve as a serial data port under control of the Shift Register (SR). Each control line represents one standard TTL load in the input mode and can drive one TTL load in the output mode. CB2 can also drive a Darlington transistor circuit; however, CB1 cannot.

Table 1. R6522 Register Addressing

Register Number	RS Coding				Register Desig.	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/$\overline{W}$ = L)	Read (R/$\overline{W}$ = H)
0	0	0	0	0	ORB/IRB	Output Register B	Input Register B
1	0	0	0	1	ORA/IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Output Register A*	Input Register A*

NOTE: *Same as Register 1 except no handshake.



a. Port A Output Circuit

b. Port B Output Circuit

Figure 3. Port A and B Output Circuits

FUNCTIONAL DESCRIPTION

The internal organization of the R6522 VIA is illustrated in Figure 4.

PORT A AND PORT B OPERATION

The R6522 VIA has two 8-bit bidirectional I/O ports (Port A and Port B) and each port has two associated control lines.

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A "1" causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and the Input Register (IRA, IRB). When the pin is programmed as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register. A "1" in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the *level on the pin* determines whether a "0" or a "1" is sensed. When reading IRB, however, the bit stored in the *output register,* ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 5 through 8 illustrate the formats of the port registers.

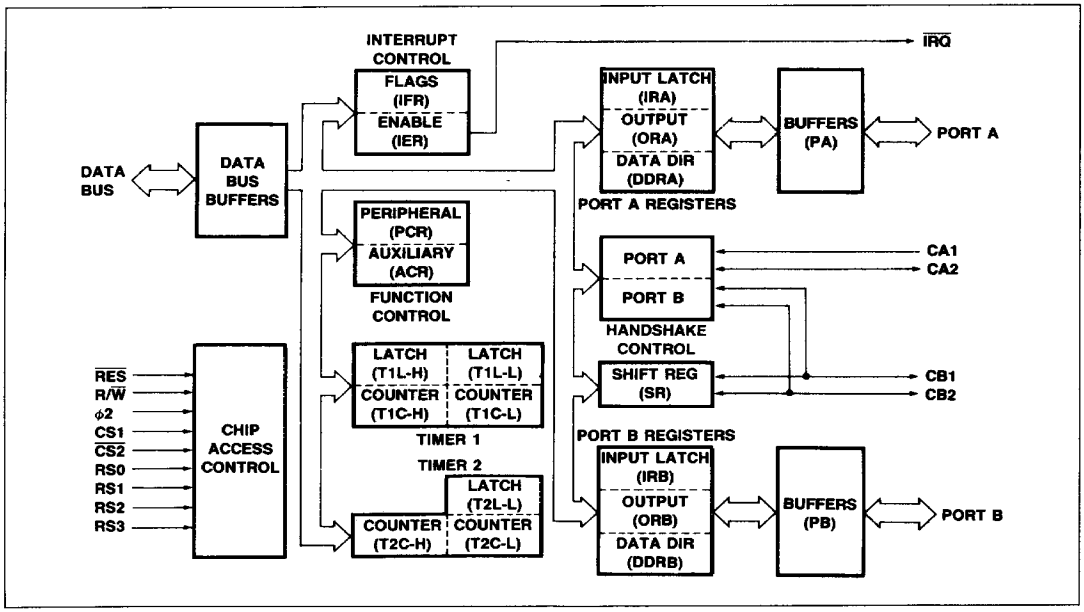


Figure 4. R6522 VIA Block Diagram

HANDSHAKE CONTROL OF DATA TRANSFERS

The R6522 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the R6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 9 which illustrates the normal Read Handshake sequence.

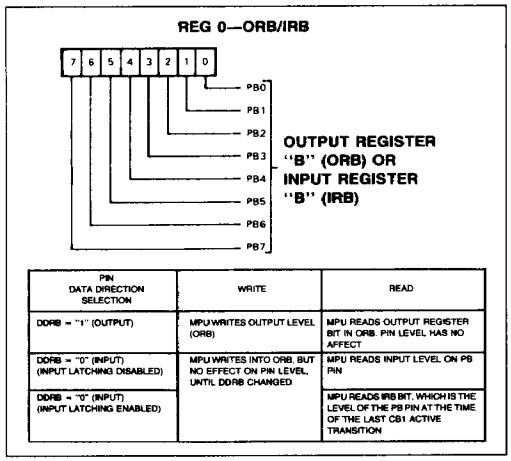


Figure 5. Output Register B (ORB), Input Register B (IRB)

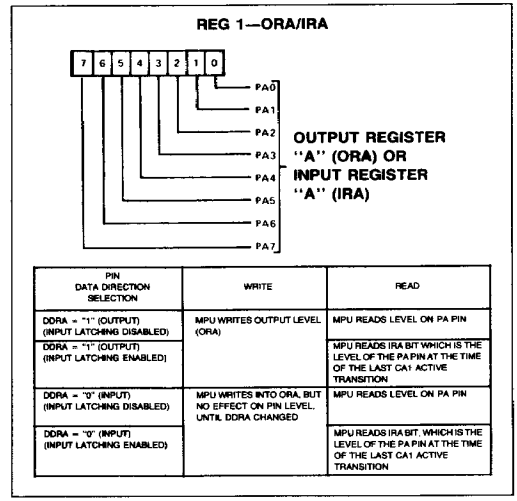


Figure 6. Output Register A (ORA), Input Register A (IRA)

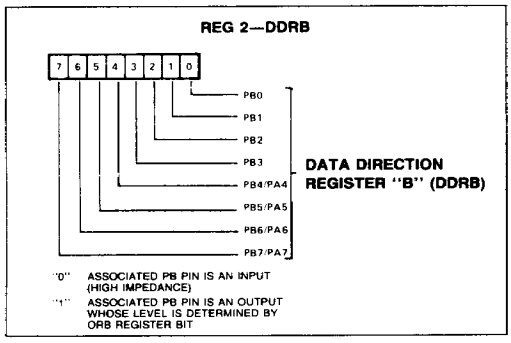


Figure 7. Data Direction Register B (DDRB)

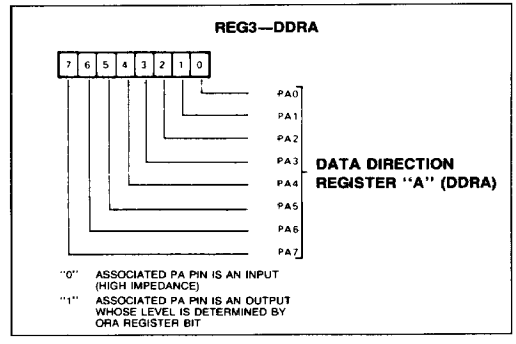


Figure 8. Data Direction Register A (DDRA)

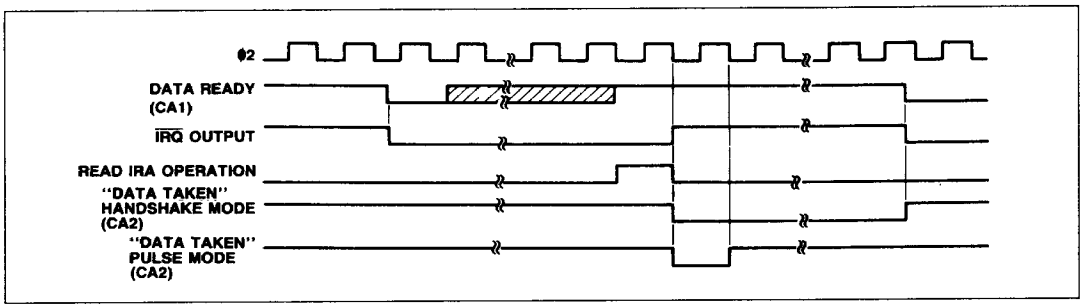


Figure 9. Read Handshake Timing (Port A Only)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the R6522 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the R6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 10.

Latching

The PA port and the PB port on the R6522 can be enabled in the Auxiliary Control Register (Figure 14) to be latched by their individual port control lines (CA1, CB1). Latching is selectable to be on the rising or falling edge of the signal at each individual port control line. Selection of operating modes for CA1, CA2, CB1 and CB2 is accomplished by the Peripheral Control Register (Figure 11).

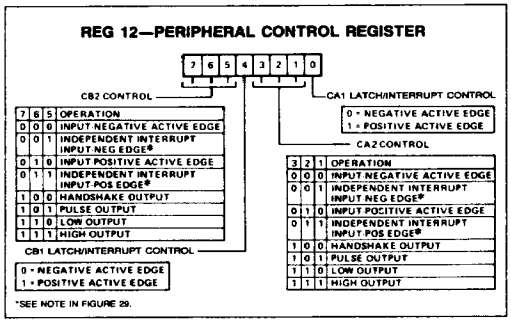


Figure 11. Peripheral Control Register (PCR)

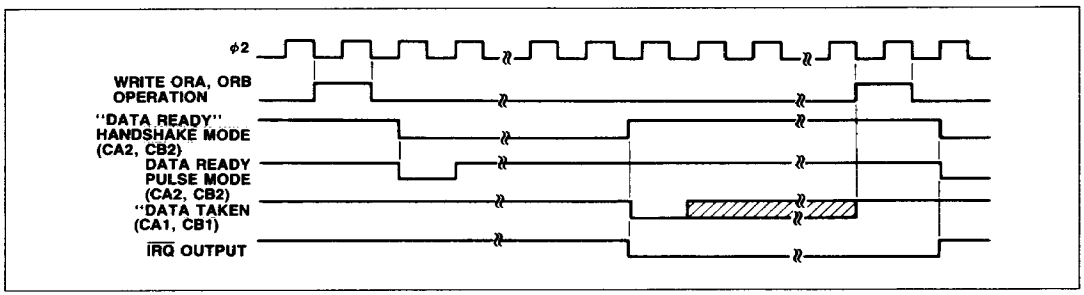


Figure 10. Write Handshake Timing

COUNTER/TIMERS

There are two independent 16-bit counter/timers (called Timer 1 and Timer 2) in the R6522. Each timer is controlled by writing bits into the Auxiliary Control Register (ACR) to select the mode of operation (Figure 14).

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches (Figure 12) and a 16-bit counter (Figure 13). The latches store data which is to be loaded into the counter. After loading, the counter decrements at Ø2 clock rate. Upon reaching zero, an interrupt flag is set, and IRQ goes low if the T1 interrupt is enabled. Timer 1 then disables any further interrupts and automatically transfers the contents of the latches into the counter and continues to decrement. In addition, the timer may be programmed to invert the output signal on peripheral pin PB7 each time it "times-out". Each of these modes is discussed separately below.

Note that the processor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch (T1L-L) when the processor writes into the high order counter (T1C-H). In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order latch.

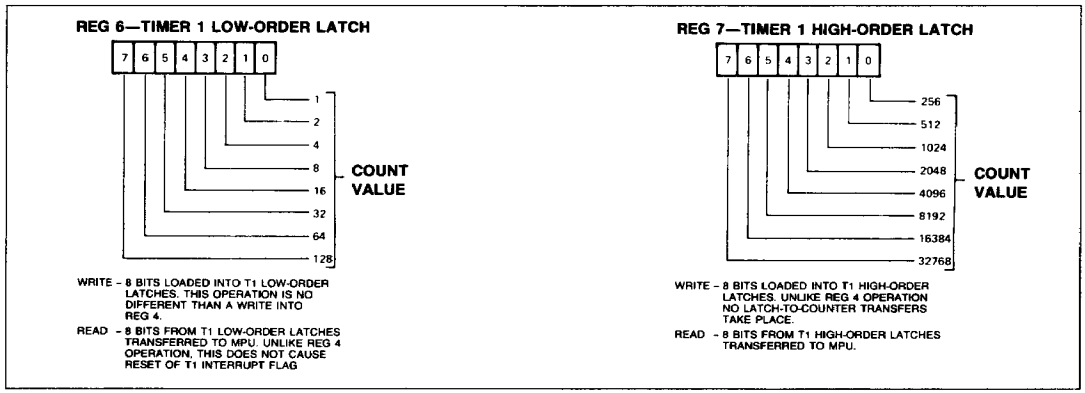


Figure 12. Timer 1 (T1) Latch Registers

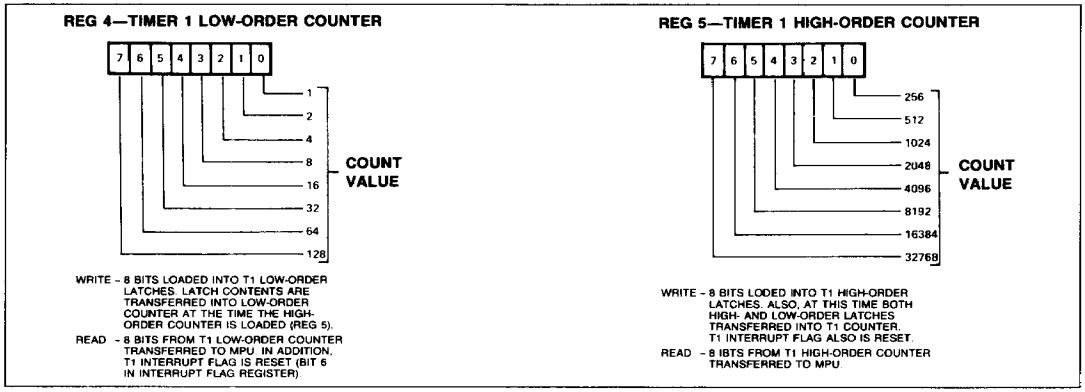


Figure 13. Timer 1 (T1) Counter Registers

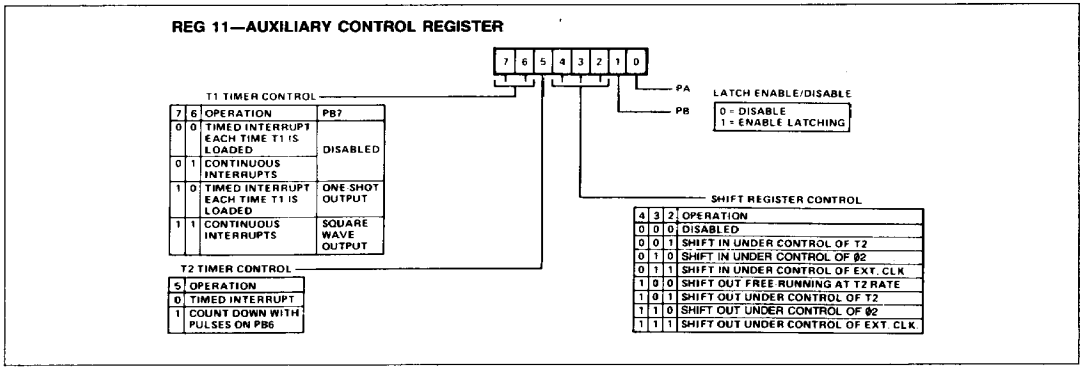


Figure 14. Auxiliary Control Register (ACR)

Timer 1 One-Shot Mode

The Timer 1 one-shot mode generates a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7 = 1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

Timing for the R6522 interval timer one-shot modes is shown in Figure 15.

In the one-shot mode, writing into the T1L-H has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter (T1C-H), the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the falling edge of Ø2 following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

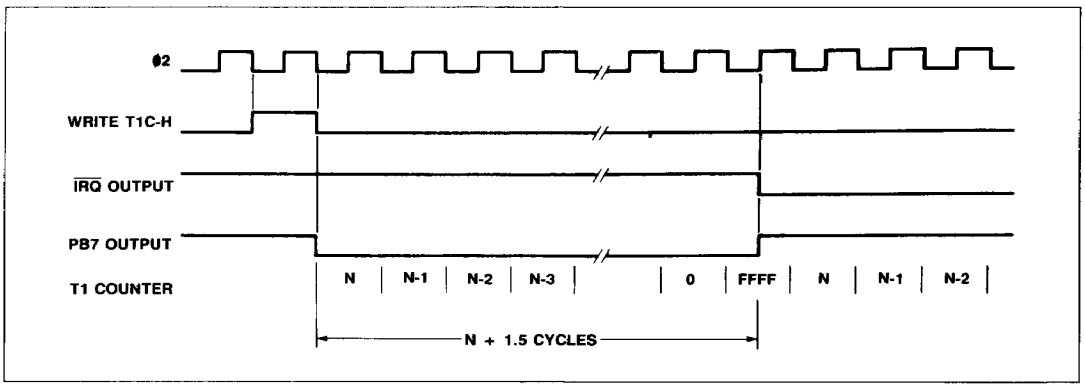


Figure 15. Timer 1 One-Shot Mode Timing

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero at which time the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H or T1L-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the R6522 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated.

A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. *Both* DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and other is 0, then PB7 functions as a normal outpin pin, controlled by ORB bit 7.

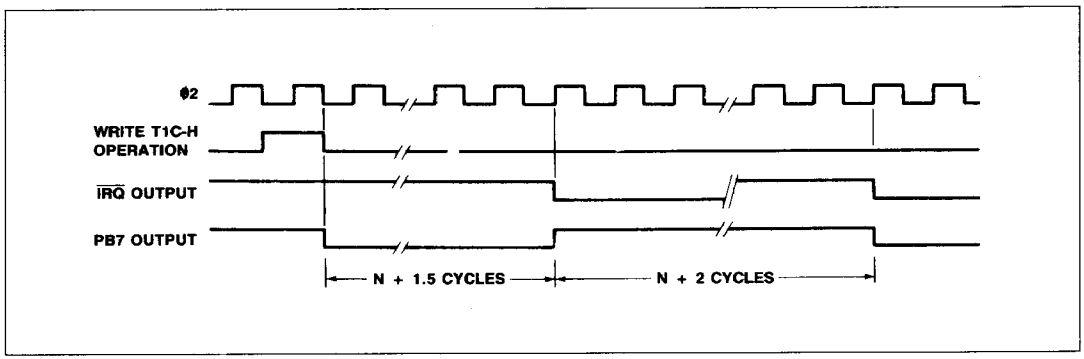


Figure 16. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit in the Auxiliary Control Register selects between these two modes. This timer is comprised of a "write-only" lower-order latch (T2L-L), a "read-only" low-order counter (T2C-L) and a read/write high order counter (T2C-H). The counter registers act as a 16-bit counter which decrements at Φ2 rate. Figure 17 illustrates the T2 Latch/Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag is disabled after initial time-out so that it will not be set by the counter decrementing again through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 counts a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag is set when T2 counts down past zero. The counter will then continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on a subsequent time-out. Timing for this mode is shown in Figure 19. The pulse must be low on the leading edge of Φ2.

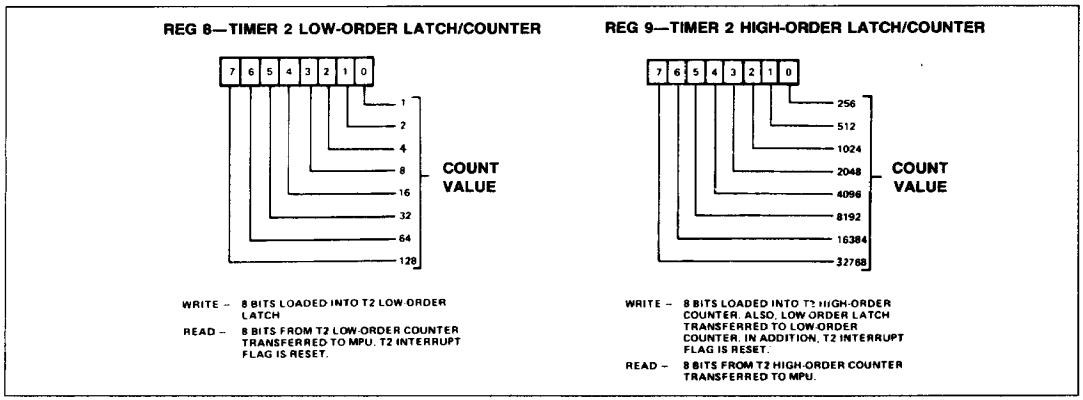


Figure 17. Timer 2 (T2) Latch/Counter Registers

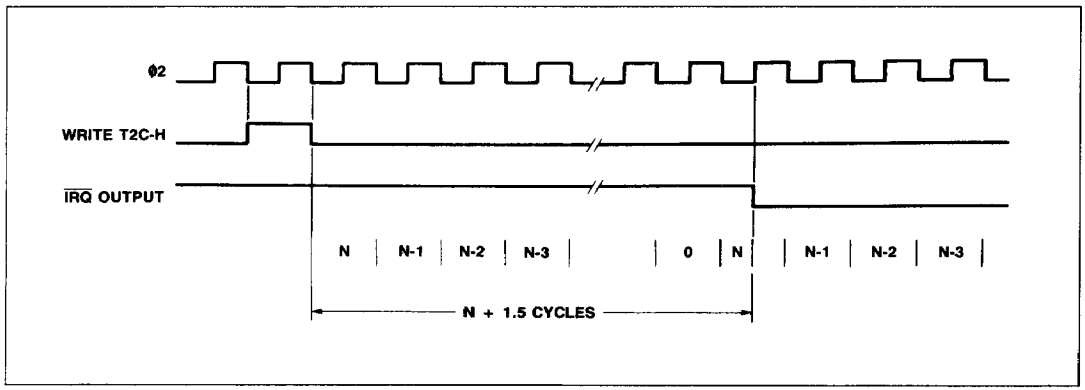


Figure 18. Timer 2 One-Shot Mode Timing

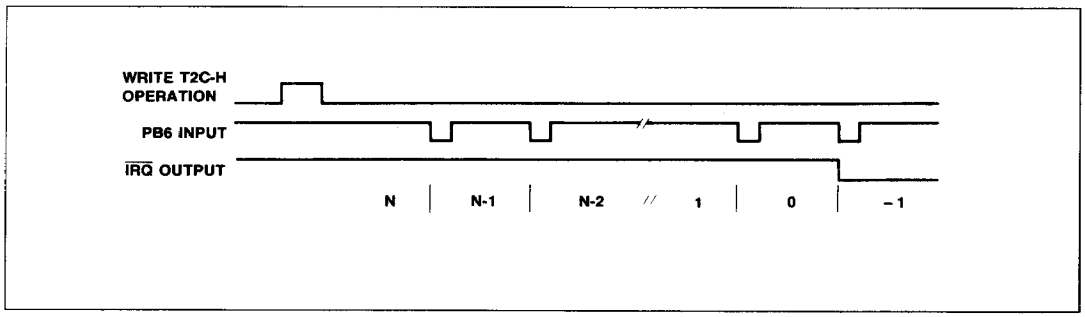


Figure 19. Timer 2 Pulse Counting Mode

SHIFT REGISTER OPERATION

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Serial data transfer in and out of the Shift Register (SR) begin with the most significant bit (MSB) first. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 20 illustrates the configuration of the SR data bits and Figure 21 shows the SR control bits of the ACR.

SR Mode 0 — Shift Register Interrupt Disabled

Mode 0 disables the Shift Register interrupt. In this mode the microprocessor can write or read the SR and the SR will shift on each CB1 positive edge shifting in the value on CB2. In this mode the SR interrupt Flag is disabled (held to a logic 0).

SR Mode 1 — Shift In Under Control of T2

In mode 1, the shifting rate is controlled by the low order 8 bits of T2 (Figure 22). Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR. Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. The input data should change before the positive-going edge of CB1 clock pulse. This data is shifted into the shift register during the $\phi 2$ clock cycle following the positive-going edge of the CB1 clock pulse. The minimum CB1 positive pulse width must be one clock period. After 8 CB1 clock pulses, the shift register interrupt flag will set and $\overline{IRQ}$ will go low.

SR Mode 2 — Shift In Under $\phi 2$ Control

In mode 2, the shift rate is a direct function of the system clock frequency (Figure 23). CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted, first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each $\phi 2$ clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

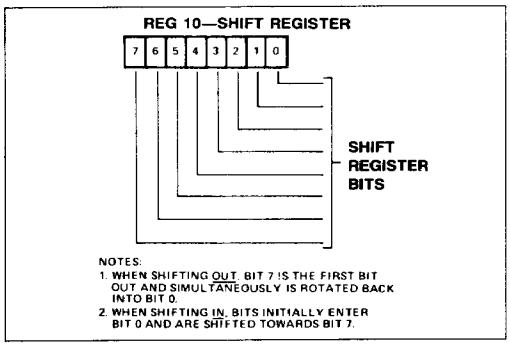


Figure 20. Shift Register

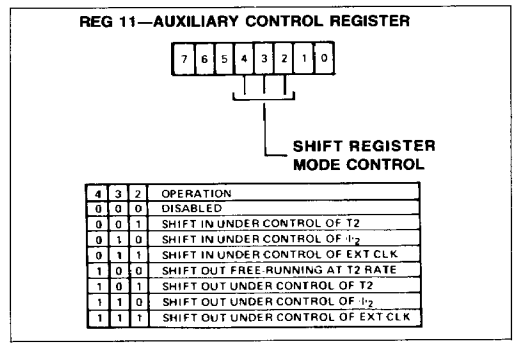


Figure 21. Shift Register Modes

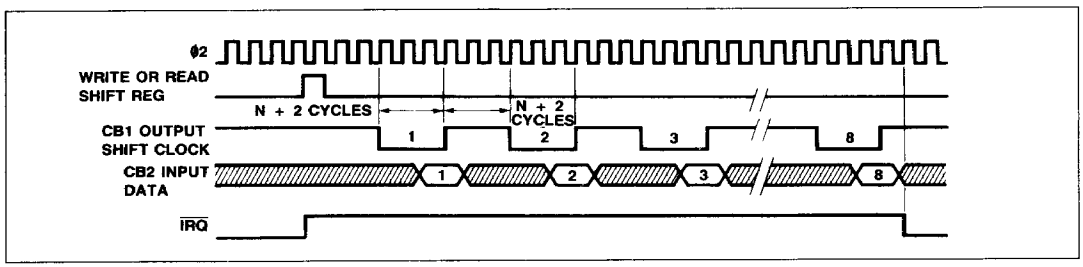


Figure 22. SR Mode 1 — Shift In Under T2 Control

SR Mode 3 — Shift In Under CB1 Control

In mode 3, external pin CB1 becomes an input (Figure 24). This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. The shift register stops after 8 counts and must be reset to start again. Reading or writing the Shift Register resets the Interrupt Flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. The minimum CB1 positive pulse width must be one clock period.

SR Mode 4 — Shift Out Under T2 Control (Free-Run)

Mode 4 is very similar to mode 1 in which the shifting rate is set by T2. However, in mode 4 the SR Counter does not stop the shifting operation (Figure 25). Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

SR Mode 5 — Shift Out Under T2 Control

In mode 5, the shift rate is controlled by T2 (as in mode 1). The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR (Figure 26). Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.

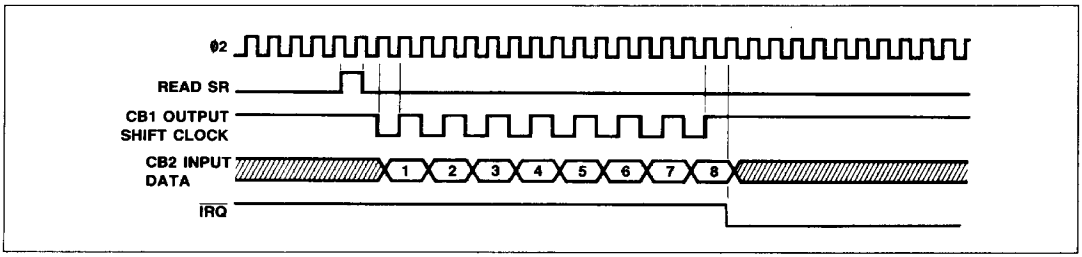


Figure 23. SR Mode 2 — Shift In Under Φ2 Control

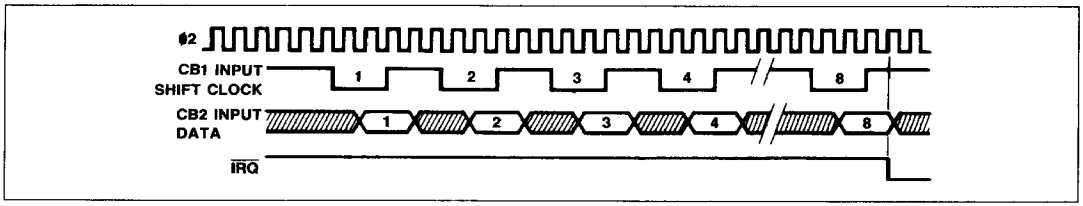


Figure 24. SR Mode 3 — Shift In Under CB1 Control

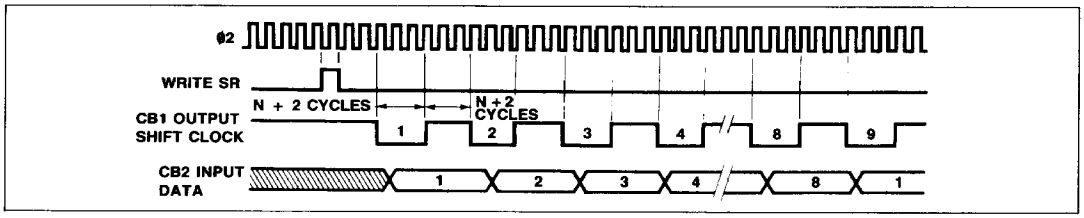


Figure 25. SR Mode 4 — Shift Out Under T2 Control (Free-Run)

SR Mode 6 — Shift Out Under Ø2 Control

In mode 6, the shift rate is controlled by the Ø2 system clock (Figure 27).

SR Mode 7 — Shift Out Under CB1 Control

In mode 7, shifting is controlled by pulses applied to the CB1 pin by an external device (Figure 28). The SR counter sets the SR Interrupt Flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor, writes or reads the shift register, the SR Interrupt Flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the Interrupt Flag is set. The microprocessor can then load the shift register with the next byte of data.

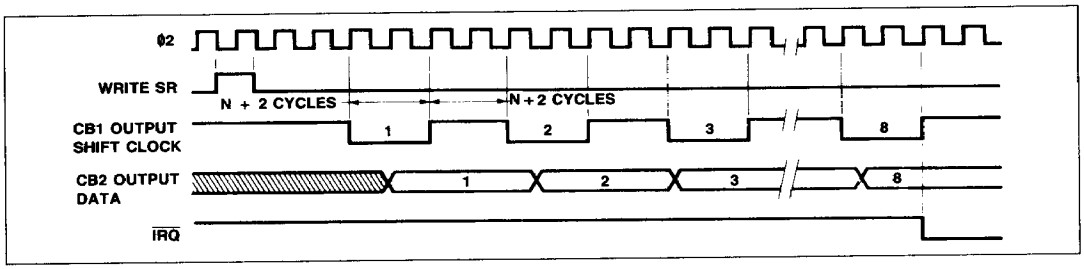


Figure 26. SR Mode 5 — Shift Out Under T2 Control

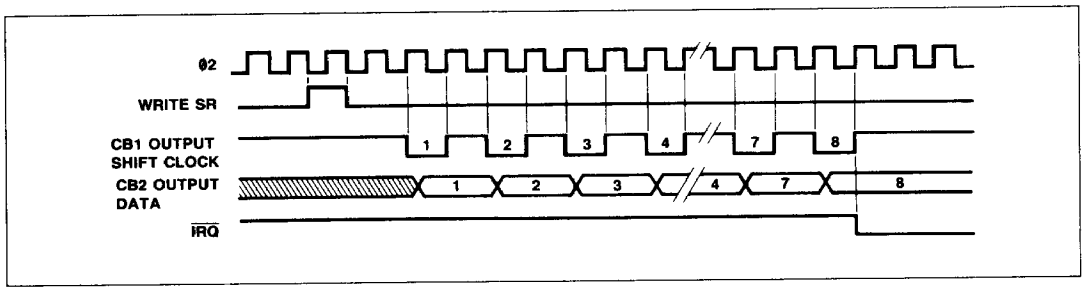


Figure 27. SR Mode 6 — Shift Out Under Ø2 Control

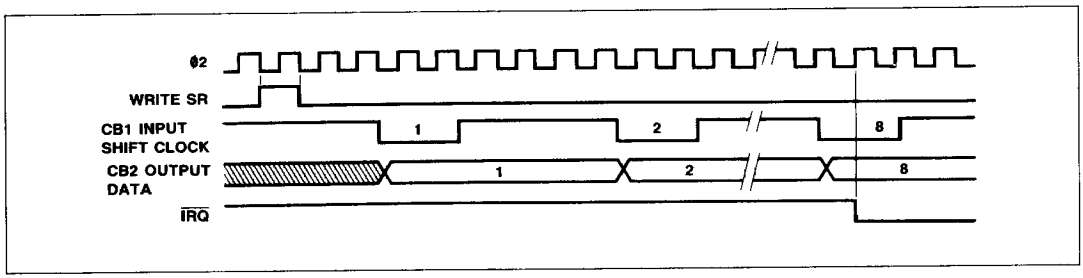


Figure 28. SR Mode 7 — Shift Out Under CB1 Control

INTERRUPT OPERATION

Controlling interrupts within the R6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupts exists within the chip. Interrupt flags are set in the Interrupt Flag Register (IFR) by conditions detected within the R6522 or on inputs to the R6522. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order, from highest to lowest priority.

Associated with each interrupt flag is an interrupt enable bit in the Interrupt Enable Register (IER). This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-OR'ed" with other devices in the system to interrupt the processor.

Interrupt Flag Register (IFR)

In the R6522, all the interrupt flags are contained in one register, i.e., the IFR (Figure 29). In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

The Interrupt Flag Register (IFR) may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: $\overline{IRQ} = IFR6 \times IER6 + IFR5 \times IER5 + IFR4 \times IER4 + IFR3 \times IER3 + IFR2 \times IER2 + IFR1 \times IER1 + IFR0 \times IER0$.

Note:

× = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

Interrupt Enable Register (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register (IER) (Figure 30). Individual bits in the IER can be set or cleared to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to the (IER) after bit 7 set or cleared to, in turn, set or clear selected enable bits. If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Selected bits in the IER can be set by writing to the IER with bit 7 in the data word set to a 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the contents of this register can be read at any time. Bit 7 will be read as a logic 1, however.

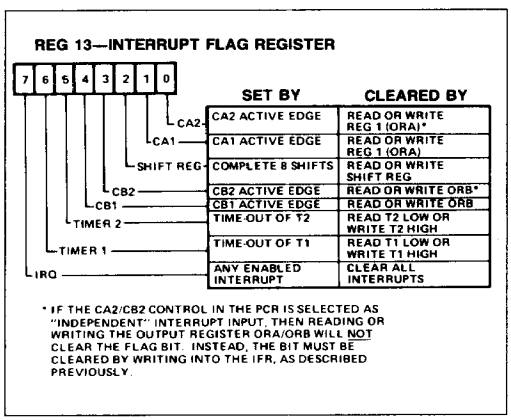


Figure 29. Interrupt Flag Register (IFR)

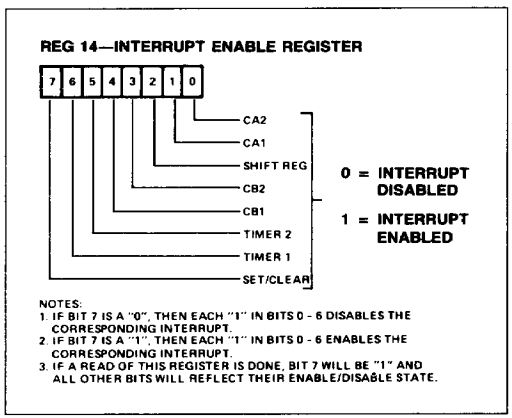


Figure 30. Interrupt Enable Register (IER)

PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Characteristic	Min.	Max.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	—	1.0	μs	—
t_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	—	1.0	μs	31a, 31b
t_{RS1}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	—	1.0	μs	31a
t_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	—	2.0	μs	31b
t_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0	μs	31c, 31d
t_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1.5	μs	31c, 31d
t_{RS3}	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	—	1.0	μs	31c
t_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	—	2.0	μs	31d
t_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	—	ns	31d
t_{IL}	Setup Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	—	ns	31e
t_{AL}	CA1, CB1 Setup Prior to Transition to Arm Latch	300	—	ns	31e
t_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	—	ns	31e
t_{SR1}	Shift-Out Delay Time — Time from ϕ_2 Falling Edge to CB2 Data Out	—	300	ns	31f
t_{SR2}	Shift-In Setup Time — Time from CB2 Data In to ϕ_2 Rising Edge	300	—	ns	31g
t_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}	ns	31g
t_{IPW}	Pulse Width — PB6 Input Pulse	2 x T_{CY}	—		31i
t_{ICW}	Pulse Width — CB1 Input Clock	2 x T_{CY}	—		31h
t_{IPS}	Pulse Spacing — PB6 Input Pulse	2 x T_{CY}	—		31i
t_{ICS}	Pulse Spacing — CB1 Input Pulse	2 x T_{CY}	—		31h

PERIPHERAL INTERFACE WAVEFORMS

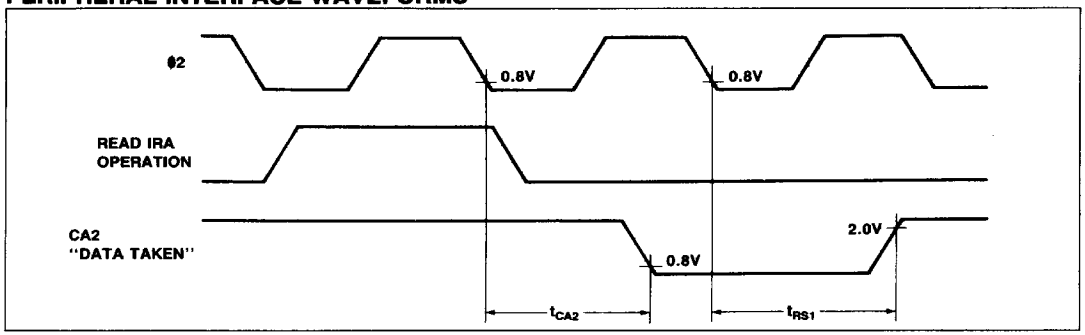


Figure 31a. CA2 Timing for Read Handshake, Pulse Mode

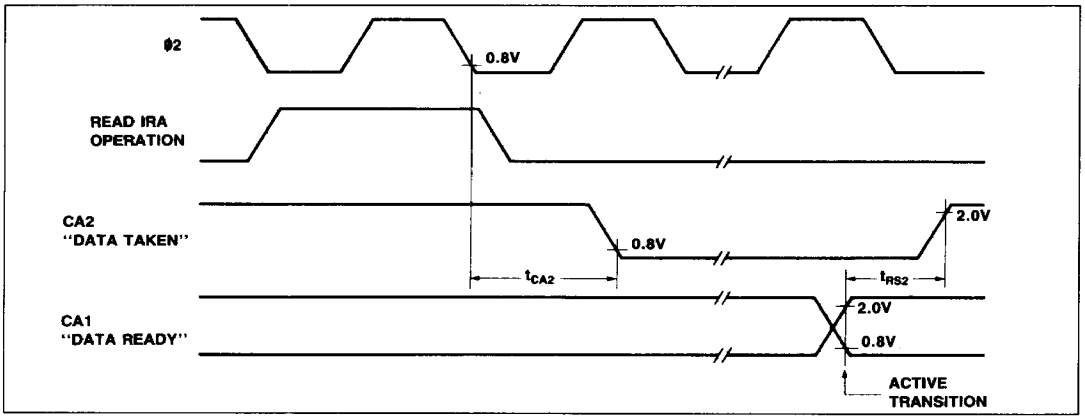


Figure 31b. CA2 Timing for Read Handshake, Handshake Mode

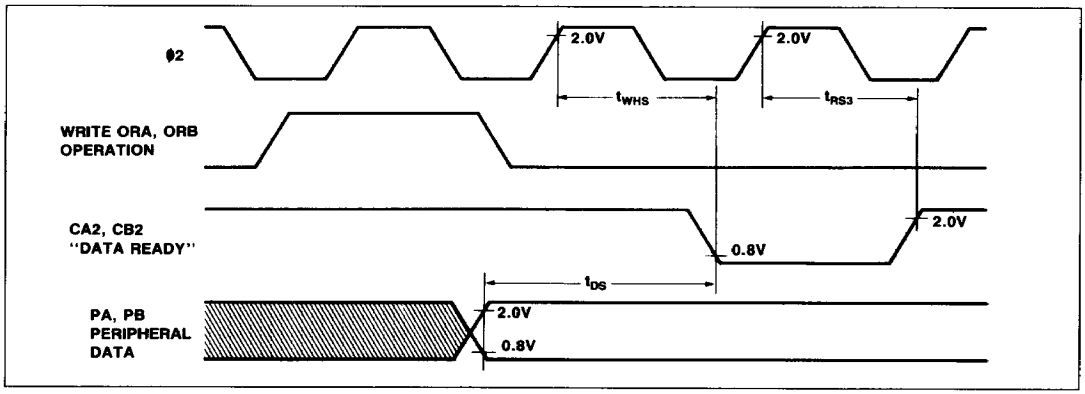


Figure 31c. CA2, CB2 Timing for Write Handshake, Pulse Mode

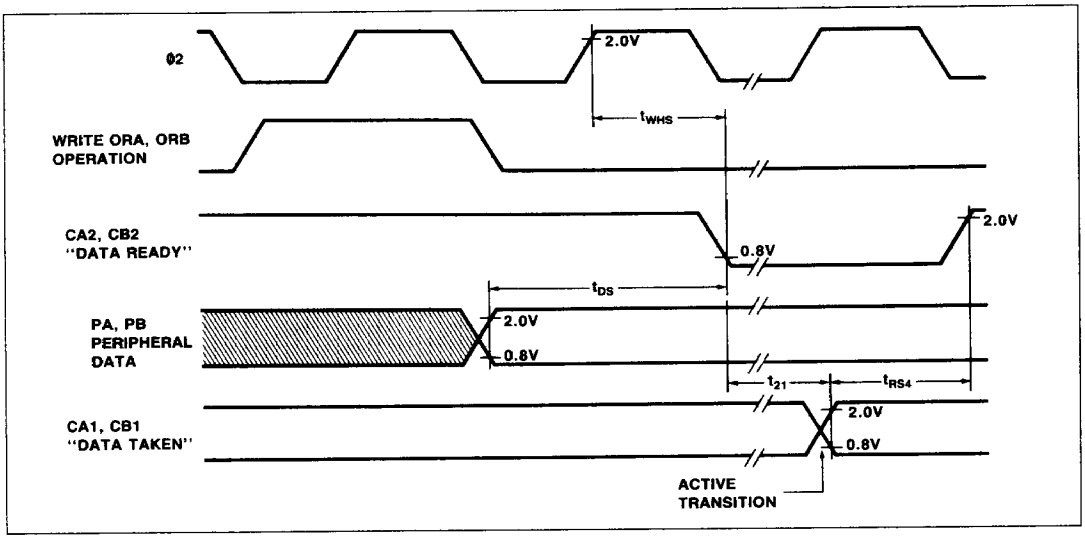


Figure 31d. CA2, CB2 Timing for Write Handshake, Handshake Mode

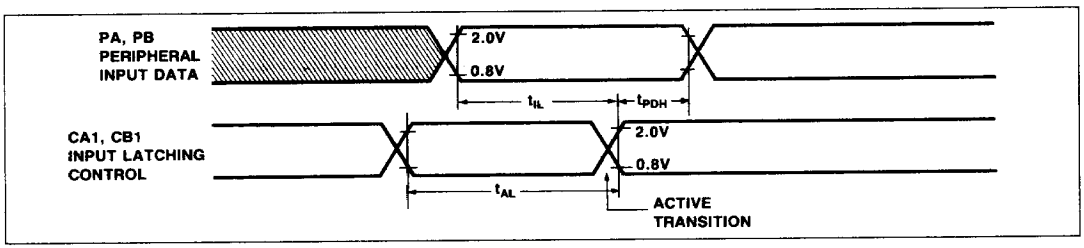


Figure 31e. Peripheral Data Input Latching Timing

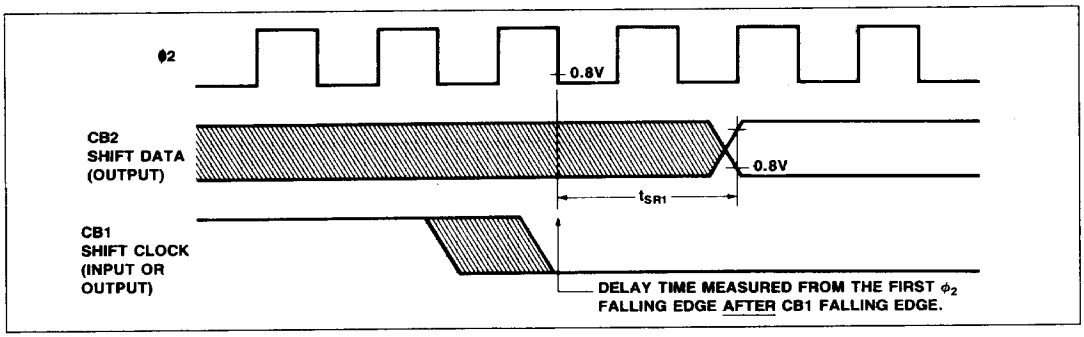


Figure 31f. Timing for Shift Out with Internal or External Shift Clocking

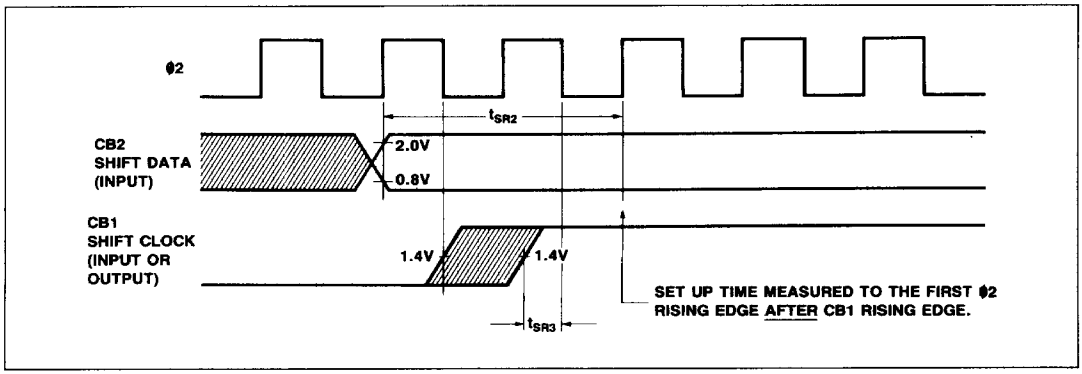


Figure 31g. Timing for Shift in with Internal or External Shift Clocking

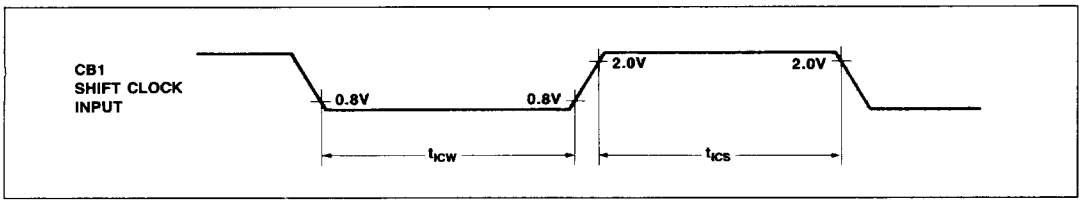


Figure 31h. External Shift Clock Timing

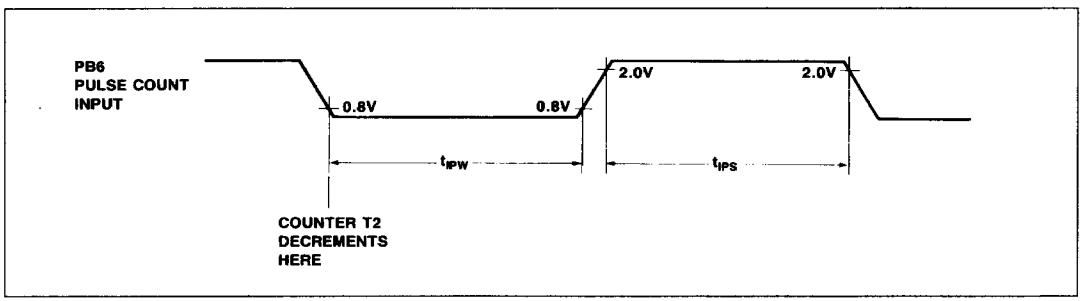
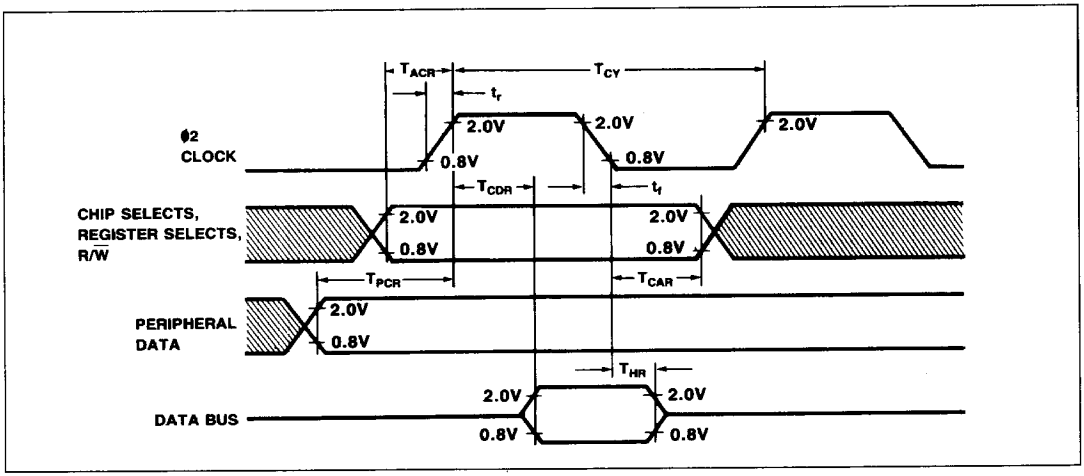


Figure 31i. Pulse Count Input Timing

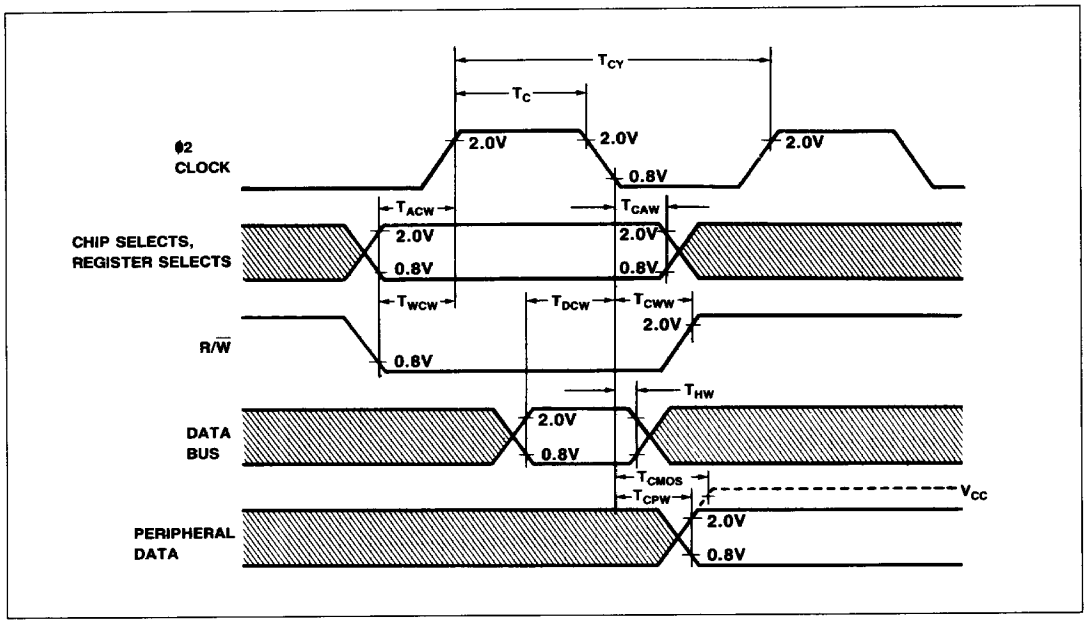
BUS TIMING CHARACTERISTICS

Parameter	Symbol	R6522 (1 MHz)		R6522A (2 MHz)		Unit
		Min.	Max.	Min.	Max.	
READ TIMING						
Cycle Time	T_{CY}	1	10	0.5	10	μs
Address Set-Up Time	T_{ACR}	180	—	90	—	ns
Address Hold Time	T_{CAR}	0	—	0	—	ns
Peripheral Data Set-Up Time	T_{PCR}	300	—	150	—	ns
Data Bus Delay Time	T_{CDR}	—	365	—	190	ns
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
WRITE TIMING						
Cycle Time	T_{CY}	1	10	0.50	10	μs
Ø2 Pulse Width	T_C	470	—	235	—	ns
Address Set-Up Time	T_{ACW}	180	—	90	—	ns
Address Hold Time	T_{CAW}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	T_{WCW}	180	—	90	—	ns
R/$\overline{W}$ Hold Time	T_{CWW}	0	—	0	—	ns
Data Bus Set-Up Time	T_{DCW}	200	—	90	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	T_{CPW}	—	1.0	—	0.5	μs
Peripheral Data Delay Time to CMOS Levels	T_{CMOS}	—	2.0	—	1.0	μs
Note: t_R and t_F = 10 to 30 ns.						

BUS TIMING WAVEFORMS



Read Timing Waveforms



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	 °C °C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial	T_A	 0°C to 70°C

DC CHARACTERISTICS

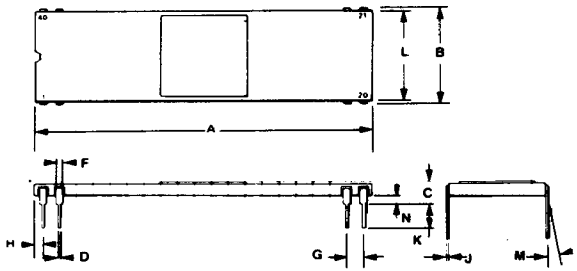
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.4	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	0.4	V	
Input Leakage Current R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, CA1, ϕ2	I_{IN}	—	±1	±2.5	μA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Input Leakage Current for Three-State Off D0-D07	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0-PA7, CA2, PB0-PB7, CB1, CBS	I_{IH}	−100	−200	—	μA	V_{IN} = 2.4V V_{CC} = 5.25V
Input Low Current PA0-PA7, CA2, PB0-PB7, CB1, CB2	I_{IL}	—	−0.9	−1.8	mA	V_{IL} = 0.4V V_{CC} = 5.25V
Output High Voltage All outputs PB0-PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	 V V	V_{CC} = 4.75V I_{LOAD} = −100 μA I_{LOAD} = −1.0 mA
Output Low Voltage	V_{OL}	—	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0-PB7, CB2 (Darlington Drive)	I_{OH}	 −100 −1.0	 −1000 −2.5	 — −10	 μA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (Off State) IRQ	I_{OFF}	—	4	±10	μA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	450	700	mW	
Input Capacitance R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7 CB1, CB2 ϕ2 Input	C_{IN}	 — — —	 — — —	 7 10 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (DC) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.

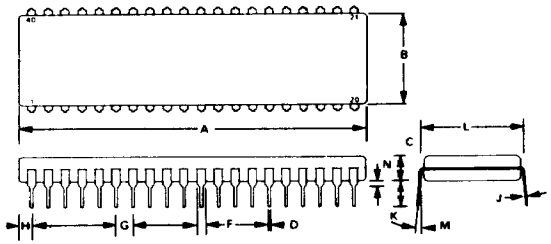
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.80	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040