



High Speed CMOS 10-bit Bus Switches

QS54/74QST3384
QS54/74QST3584
PRELIMINARY

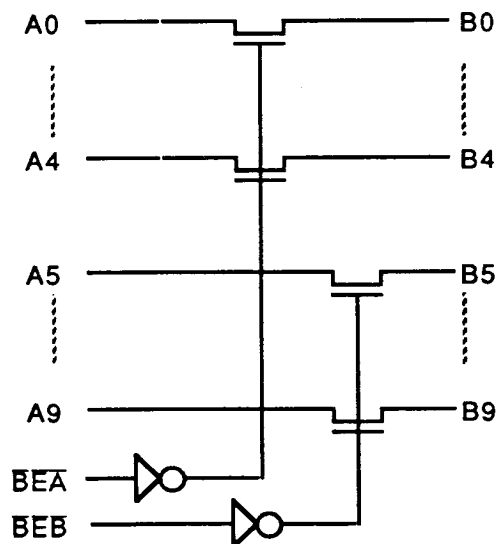
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Direct bus connection when switches on
- Zero propagation delay
- Undershoot Clamp diodes on all inputs
- Low power CMOS proprietary technology
- 3584 is 25Ω version for low noise
- Two enables control 5 bits each
- Zero ground bounce in flow-through mode
- TTL-compatible input and output levels
- Available in 24-pin PDIP, ZIP, SOIC and Cerdip

DESCRIPTION

The QS54/74QST3384 and 3584 each provide a set of ten high-speed CMOS TTL-compatible bus switches. The low on resistance (5Ω) of the 3384 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The 3584 adds an internal 25Ω resistor to reduce reflection noise in high speed applications. The bus enable (BE) signals turn the switches on. Two bus enable signals are provided, one for each of the upper and lower five bits of the two 10-bit buses.

FUNCTIONAL BLOCK DIAGRAM



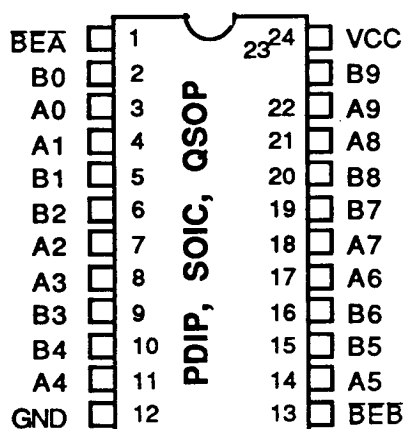
PIN DESCRIPTION

Name	I/O	Function
A0-9	I/O	Bus A
B0-9	I/O	Bus B
BEA, BEB	I	Bus Switch Enable

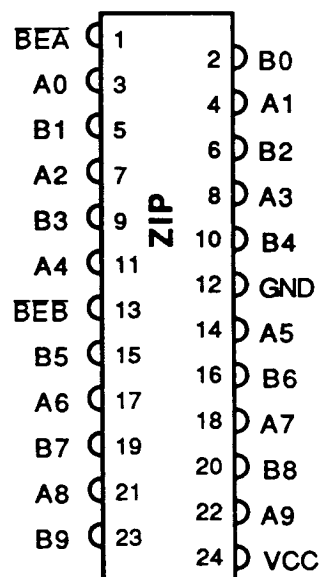
FUNCTION TABLE

BEA	BEB	B0-4	B5-9	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A0-4	Hi-Z	Connect
H	L	Hi-Z	A5-9	Connect
L	L	A0-4	A5-9	Connect

PIN CONFIGURATIONS



ALL PINS TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Switch Voltage V_S	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Current Max. sink current/pin.....	120 mA
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0V$, $V_{out} = 0V$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance, Controls	$V_{in} = 0\text{ V}$	6		pF
Coff	A/B I/O Capacitance, Switch Off	$V_{in} = 0\text{ V}$	6		pF
Con	A/B I/O Capacitance, Switch On	$V_{in} = 0\text{ V}$	10		pF

Capacitance is guaranteed but not tested

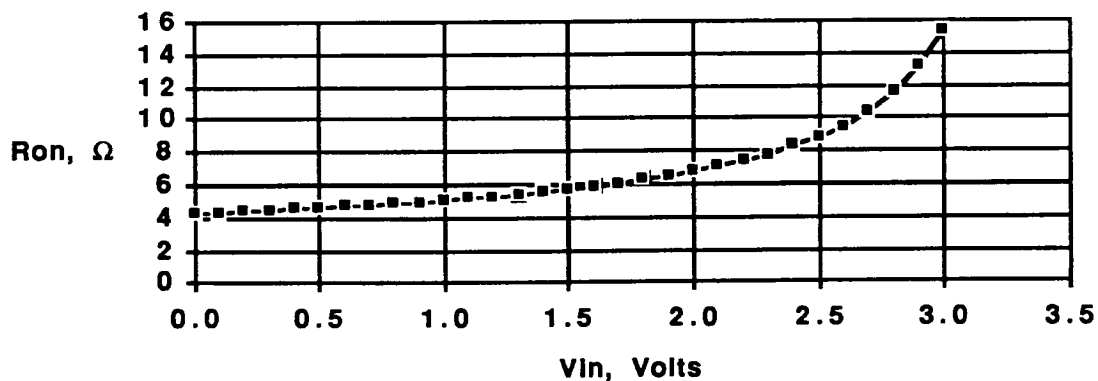
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
V _{ih}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	-	-	Volts	
V _{il}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	-	-	0.8	Volts	
I _{in}	Input Leakage Current	0 ≤ V _{in} ≤ V _{cc}	-	-	1	μA	
I _{oz}	Off State Current (Hi-Z)	0 ≤ A, B ≤ V _{cc}	-	.001	1	μA	
I _{os}	Short Circuit Current (2)	A (B) = 0V, B (A) = V _{cc}	100	-	-	mA	
V _{ic}	Clamp Diode Voltage	V _{cc} = Min, I _{in} = -18 mA	-	-0.7	-1.2	Volts	
R _{on}	Switch On Resistance (Note 3)	V _{cc} = Min, V _{in} = 0.0 Volts I _{on} = 48 mA	33XX	-	5	7	Ω
			35XX	24	28	35	Ω
		V _{cc} = Min, V _{in} = 2.4 Volts I _{on} = 15 mA	33XX	-	10	15	Ω
			35XX	24	35	48	Ω

Notes:

1. Typical values indicate VCC=5.0V and TA=25°C.
2. Not more than one output should be used to test this high power condition, and the duration is ≤1 second.
3. Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A, B) pins.

On Resistance vs Vin @ 4.75 Vcc

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Typ	Max	Unit
I_{cc}	Quiescent Power Supply Current	$V_{cc} = \text{MAX}, V_i = \text{GND or } V_{cc}, f = 0$	-	-	1.5	mA
ΔI_{cc}	Pwr Supply Current, per Input High (2)	$V_{cc} = \text{MAX}, \text{Input} = 3.4 \text{ V}, f = 0$ Per control input	-	-	2.5	mA
Q_{ccd}	Dynamic Pwr Supply Current per mHz (3)	$V_{cc} = \text{MAX}, \text{A \& B pins open,}$ Control input toggling @ 50% duty cycle	-	-	0.25	mA/ mHz
I_c	Total Power Supply Current (4,5)	$V_{cc} = \text{MAX}, \text{A \& B pins at } 0.0 \text{ V},$ Control inputs toggling @ 50% duty cycle $V_{ih} = 3.4 \text{ V}, f_{\text{clock}} = 10 \text{ mHz}$	-	-	9.0	mA

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_i=3.4\text{V}$, control inputs only). A and B pins do not contribute to I_{cc} .
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
- $I_c = I_{\text{Quiescent}} + I_{\text{Inputs}} + I_{\text{Dynamic}}$
 $I_{cc} = I_{\text{Quiescent Current}}$
 $\Delta I_{cc} = \text{Power Supply Current for each TTL High input } (V_i=3.4\text{V, control inputs only})$
 $D_h = \text{Duty Cycle for each TTL input that is High (control inputs only).}$
 $N_t = \text{Number of TTL inputs that are at DH (control inputs only).}$
 $f_i = \text{frequency that the inputs are toggled (control inputs only).}$
- Note that activity on A and/or B inputs do not contribute to I_c if A and B inputs are between gnd and V_{cc} . The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, I_c will be equal to I_{cc} only regardless of activity on the A and B pins.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Note	Com		MII		Unit
			Min	Max	Min	Max	
t PLH t PHL	Data Propagation Delay Ai to Bi, Bi to Ai	3		**		**	ns
t PZH t PZL	Switch Turn On Delay BEA, BEB to Ai, Bi		1.5	6.5	1.5	7.5	
t PLZ t PZL	Switch Turn Off Delay BEA, BEB to Ai, Bi	2	1.5	5.5	1.5	6.5	

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and aloa alone is of the order of 0.25 ns for 50 pf load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.