QUALITY SEMICONDUCTOR, INC.

High-Speed CMOS Bus Interface 10-Bit Latch

QS54/74FCT841T
QS54/74FCT2841T

FEATURES/BENEFITS

- Pin and function compatible to the Am29841 74FCT841 and 74FCT841T
- Industrial temperature –40°C to 85°C
- CMOS power levels: <7.5mW static
- Available in DIP, SOIC, QSOP, ZIP
- Undershoot Clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

FCT-T 841T

- JEDEC-FCT spec compatible
- A, B, and C speed grades with 5.5ns t_{PD} for C
- I_{OL} = 48mA Ind., 32mA Mil.

FCT-T 2841T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B, and C speed grades with 5.5ns t_{PD} for C
- I_{OL} = 12mA Ind.

DESCRIPTION

The QSFCT841T is a 10-bit high-speed CMOS TTL-compatible buffered latch with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The device comes in A, B, and C speed grades with 5.5ns (Max.) t_{PLH}/t_{PLH} for the C grade. The 2841 devices is a 25Ω resistor output version useful for driving transmission lines and reducing system noise. The 2841 eliminates the need for external series resistor in high speed systems and can replace the 841 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

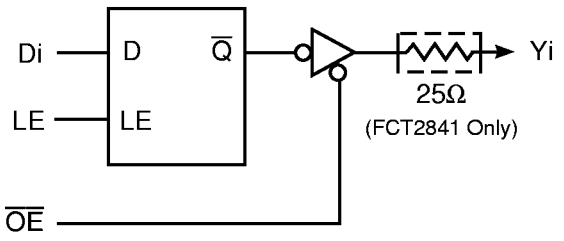

Figure 2. Pin Configurations (All Pins Top View)

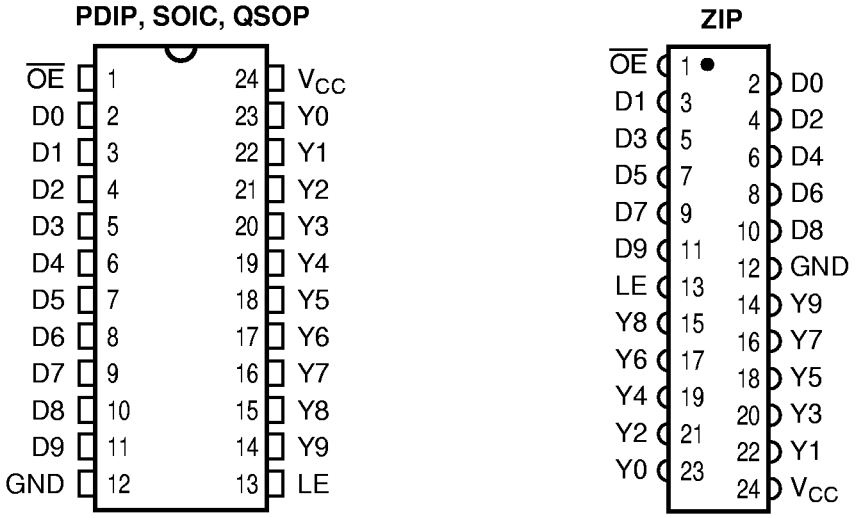

Figure 2. Logic Symbol

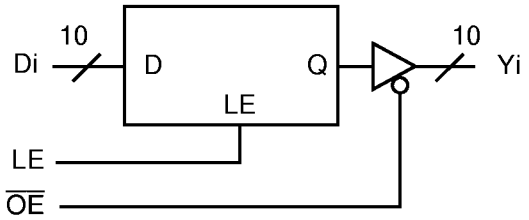

Table 1. Pin Description

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
LE	I	Latch Enable
$\overline{OE}$	I	Output Enable

Table 2. Function Tables

Inputs			Internal	Outputs	
$\overline{OE}$	LE	Di	Qi	Yi	Function
H	X	X	X	Z	Hi-Z
L	X	X	H	H	Output Enabled
L	X	X	L	L	Output Enabled
X	H	H	H	X	Transparent
X	H	L	L	X	Transparent
X	L	X	NC	X	Latched

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Output Voltage V_{OUT}	–0.5V to 7.0V
DC Input Voltage V_{IN}	–0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Diode Current with $V_{OUT} < 0$	–50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 4. Capacitance(1)

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins(2)	SOIC	QSOP	PDIP	ZIP	Unit
1-11, 13, 14, 23	4	4	5	7	pF
15-22	6	6	7	9	pF

Notes:
1. Capacitance is characterized but not tested.
2. Pin reference for 24-pin package

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions(1)	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or V_{CC}-0.2V ≤ V_{IN} ≤ V_{CC}	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max., V_{IN} = 3.4V, freq = 0(2)	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	V_{CC} = Max., Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V_{CC}(3,4)	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 6. DC Electrical Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current (FCT841)	V_{CC} = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive (FCT2841 – 25Ω)	V_{CC} = Min., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = –12mA (MIL) I_{OH} = –15mA (IND)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCT841)	V_{CC} = Min. I_{OL} = 32mA (MIL) I_{OL} = 48mA (IND)	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2841 – 25Ω)	V_{CC} = Min. I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2841 – 25Ω)	V_{CC} = Min. I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

Table 7. Switching Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description		841A 2841A Min	841A 2841A Max	841B 2841B Min	841B 2841B Max	841C 2841C Min	841C 2841C Max	Unit
t_{PHL}	Data to Y Delay	IND	—	9.0	—	6.5	—	5.5	ns
t_{PLH}	$\overline{OE}$ = LOW, 841	MIL	—	10	—	7.5	—	6.3	
t_{PHL}	Data to Y Delay(2,3)	IND	—	13	—	13	—	13	ns
t_{PLH}	$\overline{OE}$ = LOW, 841	MIL	—	15	—	15	—	15	
t_{PHL}	Data to Y Delay	IND	—	9.5	—	6.5	—	5.5	ns
t_{PLH}	$\overline{OE}$ = LOW, 2841	MIL	—	11	—	7.5	—	6.3	
t_{PHL}	Data to Y Delay(2,3)	IND	—	20	—	13	—	13	ns
t_{PLH}	$\overline{OE}$ = LOW, 2841	MIL	—	20	—	15	—	15	
t_S	Data to LE Setup	IND	2.5	—	2.5	—	2.5	—	ns
		MIL	2.5	—	2.5	—	2.5	—	
t_H	Data to LE Hold Time	IND	2.5	—	2.5	—	2.5	—	ns
		MIL	3.0	—	2.5	—	2.5	—	
t_{LEY}	LE to Y Delay	IND	—	12	—	8.0	—	6.4	ns
	$\overline{OE}$ = LOW, 841	MIL	—	13	—	10.5	—	6.8	
t_{LEY}	LE to Y Delay(2,3)	IND	—	16	—	15.5	—	15	ns
	$\overline{OE}$ = LOW, 841	MIL	—	20	—	18	—	16	
t_{LEY}	LE to Y Delay	IND	—	12	—	8	—	8	ns
	$\overline{OE}$ = LOW, 2841	MIL	—	13	—	10.5	—	10.5	
t_{LEY}	LE to Y Delay(2,3)	IND	—	16	—	15.5	—	15	ns
	$\overline{OE}$ = LOW, 2841	MIL	—	20	—	18	—	16	

Notes:
1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3. C_{LOAD} = 300pF.

Table 8. Switching Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		841A 2841A Min	841A 2841A Max	841B 2841B Min	841B 2841B Max	841C 2841C Min	841C 2841C Max	Unit
t_{LEH}	LE Pulse Width HIGH[2]	IND	6	—	4	—	4	—	ns
		MIL	6	—	4	—	4	—	
t_{PZH}	Output Enable Time	IND	—	11.5	—	8	—	6.5	ns
t_{PZL}	$\overline{OE}$ to Yi, 841	MIL	—	13	—	8.5	—	8.5	
t_{PZH}	Output Enable Time[2,3]	IND	—	23	—	14	—	12	ns
t_{PZL}	$\overline{OE}$ to Yi, 841	MIL	—	25	—	15	—	13	
t_{PZH}	Output Enable Time	IND	—	11.5	—	8	—	6.5	ns
t_{PZL}	$\overline{OE}$ to Yi, 2841	MIL	—	13	—	8.5	—	8.5	
t_{PZH}	Output Enable Time[2,3]	IND	—	23	—	14	—	12	ns
t_{PZL}	$\overline{OE}$ to Yi, 2841	MIL	—	25	—	15	—	13	
t_{PHZ}	Output Disable Time[2,4]	IND	—	7	—	6	—	5.7	ns
t_{PLZ}	$\overline{OE}$ to Yi	MIL	—	9	—	6.5	—	6	
t_{PHZ}	Output Disable Time[2]	IND	—	8	—	7	—	6	ns
t_{PLZ}	$\overline{OE}$ to Yi	MIL	—	10	—	7.5	—	6.3	

Notes:
1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3. C_{LOAD} = 300pF.
4. C_{LOAD} = 5pF.