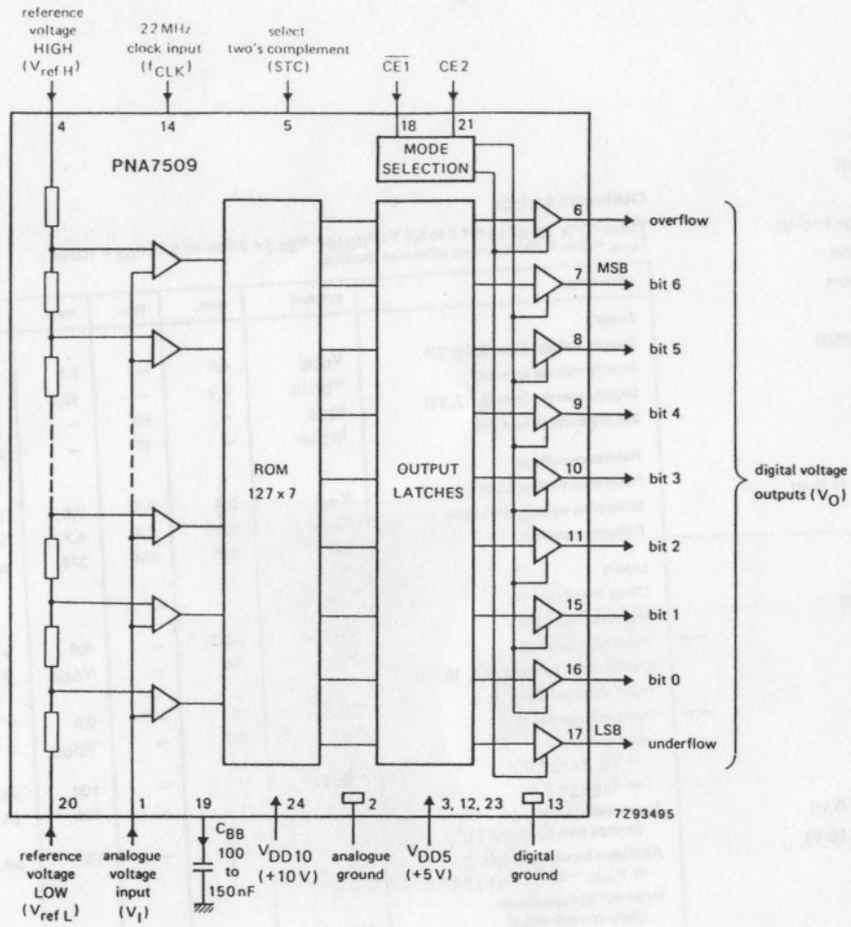
7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

GENERAL DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- Digitizing rates up to 22 MHz
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- Low reference current (250 μA typ.)
- Positive supply voltages (+ 5 V/+ 10 V)
- Low power consumption (400 mW typ.)
- Standard 24-pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Supply voltage range (pins 3, 12, 23)	V_{DD5}		4,5 to 5,5	V
Supply voltage range (pin 24)	V_{DD10}		9,5 to 10,5	V
Supply current (pins 3, 12, 23)	I_{DD5}	typ.	60	mA
Supply current (pin 24)	I_{DD10}	typ.	10	mA
Reference voltage LOW (pin 20)	V_{refL}	min.	2,4	V
Reference voltage HIGH (pin 4)	V_{refH}	max.	5,2	V
Differential non-linearity			± ½ ≙ 0,4%	LSB
Bandwidth (−3 dB)	B	min.	10	MHz
Clock frequency	f_{CLK}	max.	22	MHz
Total power dissipation	P_{tot}	typ.	400	mW

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101).

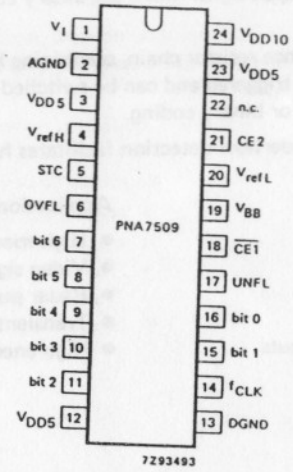


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD5}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD5}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	22 MHz clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE 2	chip enable input 2
22	n.c.	not connected
23	V_{DD5}	positive supply voltage (+ 5 V)
24	V_{DD10}	positive supply voltage (+ 10 V)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0,5 to + 7	V
Supply voltage range (pin 24)	V_{DD10}	−0,5 to + 12	V
Input voltage range	V_I	−0,5 to + 7	V
Output current	I_O	5	mA
Total power dissipation	P_{tot}	tbf	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3,\,12,\,23\text{-}13}$ = 4,5 to 5,5 V; $V_{DD10} = V_{24\text{-}2}$ = 9,5 to 10,5 V; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)	V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	I_{DD5}	–	60	–	mA
Supply current (pin 24)	I_{DD10}	–	10	–	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)	V_{refH}	5,0	5,1	5,2	V
Reference current	I_{ref}	175	250	375	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
→ Input voltage HIGH	V_{IH}	3,0	–	V_{DD5}	V
Digital input levels (pins 5, 18, 21)*					
Input voltage LOW	V_{IL}	0	–	0,8	V
→ Input voltage HIGH	V_{IH}	2,0	–	V_{DD5}	V
Input current					
at $V_{5,\,21\text{-}13}$ = 0 V	$-I_{5,\,21}$	–	–	100	μA
at $V_{18\text{-}13}$ = 5 V	I_{18}	–	–	100	μA
Input leakage current (except pins 5, 18 and 21)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at V_{refL} = 2,5 V; V_{refH} = 5,1 V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p\text{-}p)}$	–	2,6	–	V
Input voltage (underflow)	V_I	–	2,5	–	V
Input voltage (overflow)	V_I	–	5,1	–	V
Offset input voltage (underflow)	$V_I - V_{refL}$	–	10	–	mV
Offset input voltage (overflow)	$V_I - V_{refH}$	–	−10	–	mV
Input capacitance	$C_{1\text{-}2}$	–	–	60	pF

* When pin 5 is LOW binary coding is selected.
When pin 5 is HIGH two's complement is selected.
If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
For output coding see Table 1 and mode selection see Table 2.