SIEMENS

Memory Time Switch CMOS (MTSC)

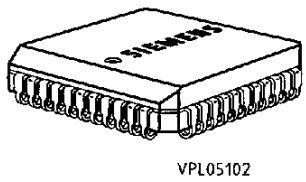
PEB 2045
PEF 2045

Preliminary Data

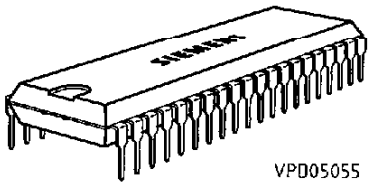
CMOS IC

1 Features

- Time/space switch for 2048-, 4096- or 8192-kbit/s PCM systems
- Switching of up to 512 incoming PCM channels to up to 256 outgoing PCM channels
- 16-input and 8-output PCM lines
- Different kinds of modes (2048, 4096, 8192 kbit/s or mixed mode)
- Configurable for primary access and standard applications
- Programmable clock shift with half clock step resolution for input and output in primary access configuration
- Configurable for a 4096- and 8192-kHz device clock
- Tristate function for further expansion and tandem operation
- Tristate control signals for external drivers in primary access configuration
- 2048-kHz clock output in primary access configuration
- Space switch mode
- 8-bit µP interface
- Single + 5 V power supply
- Advanced low power CMOS technology
- Pin and software compatible to the PEB 2040



P-LCC-44



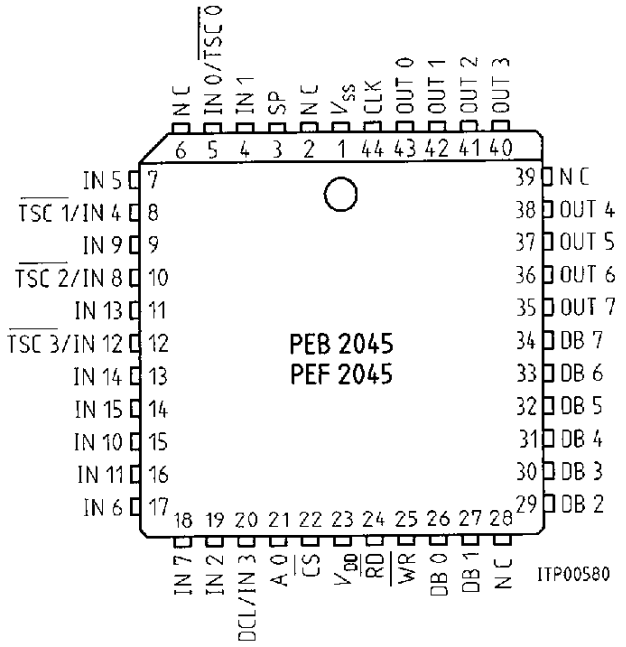
P-DIP-40

Type	Version	Ordering Code	Package
PEB 2045-N	V 2.0	Q67100-H8602	P-LCC-44 (SMD)
PEB 2045-P	V 2.0	Q67100-H8322	P-DIP-40
PEF 2045-N	V 2.0	Q67100-H6055	P-LCC-44 (SMD)
PEF 2045-P	V 2.0	Q67100-H6056	P-DIP-40

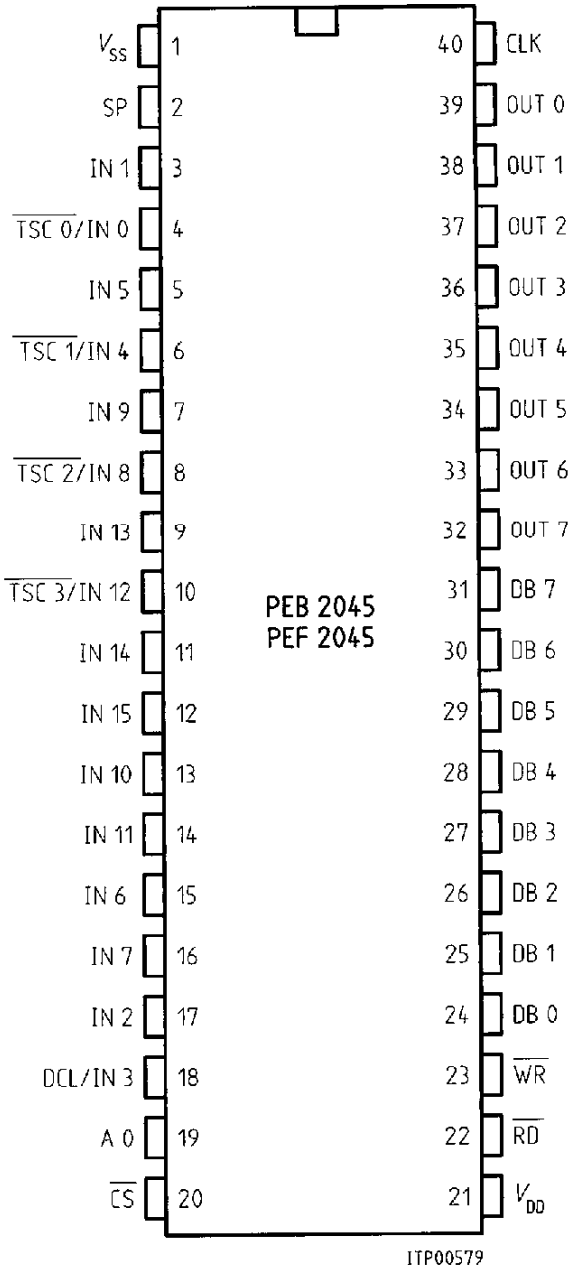
Pin Configurations

(top view)

P-LCC-44



P-DIP-40



1.1 Pin Definitions and Functions

Pin No. P-LCC	Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
1	1	V_{SS}	I	**Ground** (OV)
3	2	SP	I	**Synchronization Pulse:** The PEx 2045 is synchronized relative to the PCM system via this line.
4	3	IN1	I	**PCM-Input Ports:** Serial data is received at these lines at standard TTL levels.
7	5	IN5	I	
9	7	IN9	I	
11	9	IN13	I	
13	11	IN14	I	
14	12	IN15	I	
15	13	IN10	I	
16	14	IN11	I	
17	15	IN6	I	
18	16	IN7	I	
19	17	IN2	I	
5	4	IN0/$\overline{\text{TSC0}}$	I/O	**PCM-Input Port / Tristate Control:** In standard configuration these pins are used as input lines, in primary access configuration they supply control signals for external devices.
8	6	IN4/$\overline{\text{TSC1}}$	I/O	
10	8	IN8/$\overline{\text{TSC2}}$	I/O	
12	10	IN12/$\overline{\text{TSC3}}$	I/O	
20	18	IN3/DCL	I/O	**PCM-Input Port / Data Clock:** In standard configuration IN3 is the PCM input line 3, in primary access configuration it provides a 2048-kHz data clock for the synchronous interface.
21	19	A0	I	**Address 0:** When high, the indirect register access mechanism is enabled. If A0 is logical 0 the mode and status registers can be written to and read respectively.
22	20	$\overline{\text{CS}}$	I	**Chip Select:** A low level selects the PEx 2045 for a register access operation.
23	21	V_{DD}	I	**Supply voltage:** 5 V ± 5 %.
24	22	$\overline{\text{RD}}$	I	**Read:** This signal indicates a read operation and is internally sampled only if $\overline{\text{CS}}$ is active. The MTSC puts data from the selected internal register on the data bus with the falling edge of $\overline{\text{RD}}$. $\overline{\text{RD}}$ is active low.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
25	23	$\overline{WR}$	I	**Write:** This signal initiates a write operation. The $\overline{WR}$ input is internally sampled only if $\overline{CS}$ is active. In this case the MTSC loads an internal register with data from the data bus at the rising edge of $\overline{WR}$. $\overline{WR}$ is active low.
26	24	DB0	I/O	**Data Bus:** The data bus is used for communication between the MTSC and a processor.
27	25	DB1	I/O	
29	26	DB2	I/O	
30	27	DB3	I/O	
31	28	DB4	I/O	
32	29	DB5	I/O	
33	30	DB6	I/O	
34	31	DB7	I/O	
35	32	OUT7	0	**PCM-Output Port:** Serial data is sent by these lines at standard CMOS or TTL levels. These pins can be tristated.
36	33	OUT6	0	
37	34	OUT5	0	
38	35	OUT4	0	
40	36	OUT3	0	
41	37	OUT2	0	
42	38	OUT1	0	
43	39	OUT0	0	
44	40	CLK	I	**Clock:** 4096- or 8192-kHz device clock.

1.2 Functional Symbol

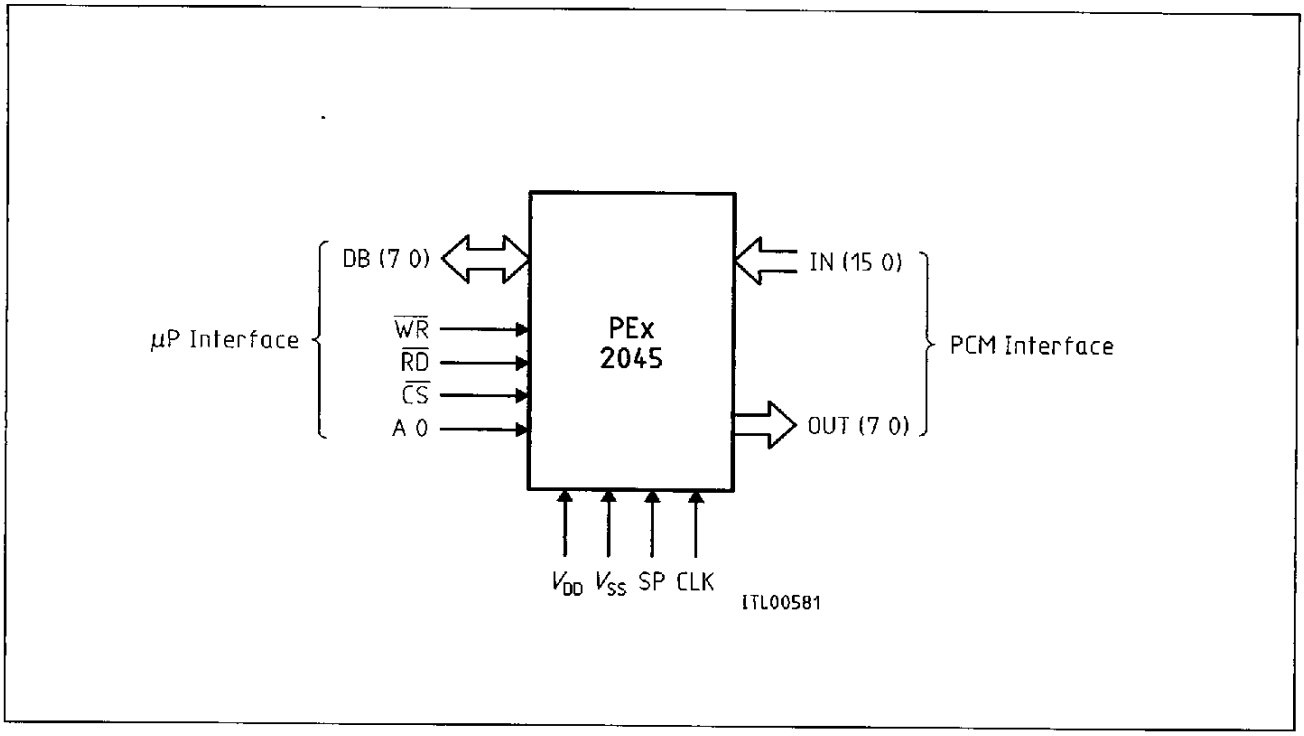


Figure 1
Functional Symbol for the Standard Configuration

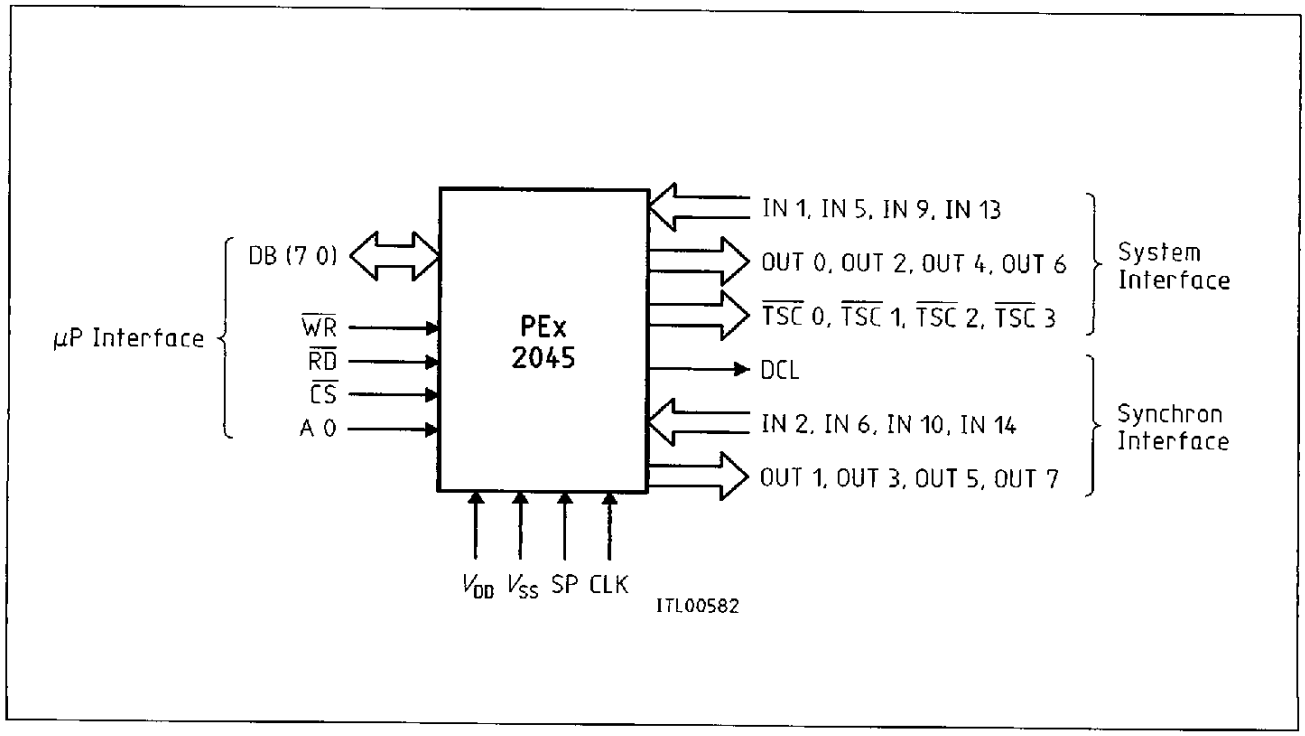


Figure 2
Functional Symbol for the Primary Access Configuration

1.3 Device Overview

The Siemens Memory Time Switch PEx 2045 is a monolithic CMOS circuit connecting any of 512 incoming PCM channels to any of 256 outgoing PCM channels. The on-chip connection memory is accessed via the 8-bit µP interface.

The PEx 2045 is fabricated using the advanced CMOS technology from Siemens and is mounted in a P-DIP-40 or a P-LCC-44 package. Inputs and outputs are TTL-compatible.

The PEx 2045 is pin and software compatible to the PEB 2040. In addition, it includes the following features:

- 4096-kHz device clock
- 4096-kbit/s PCM-data rate
- Primary access configuration
- Fast connection memory access

1.4 System Integration

The main application fields for the PEx 2045 are in switches and primary access units. **Figure 3** shows a non-blocking switch for 512 input and 512 output channels using only two devices. **Figure 4** shows how 8 devices can be arranged to form a non-blocking 1024-channel switch.

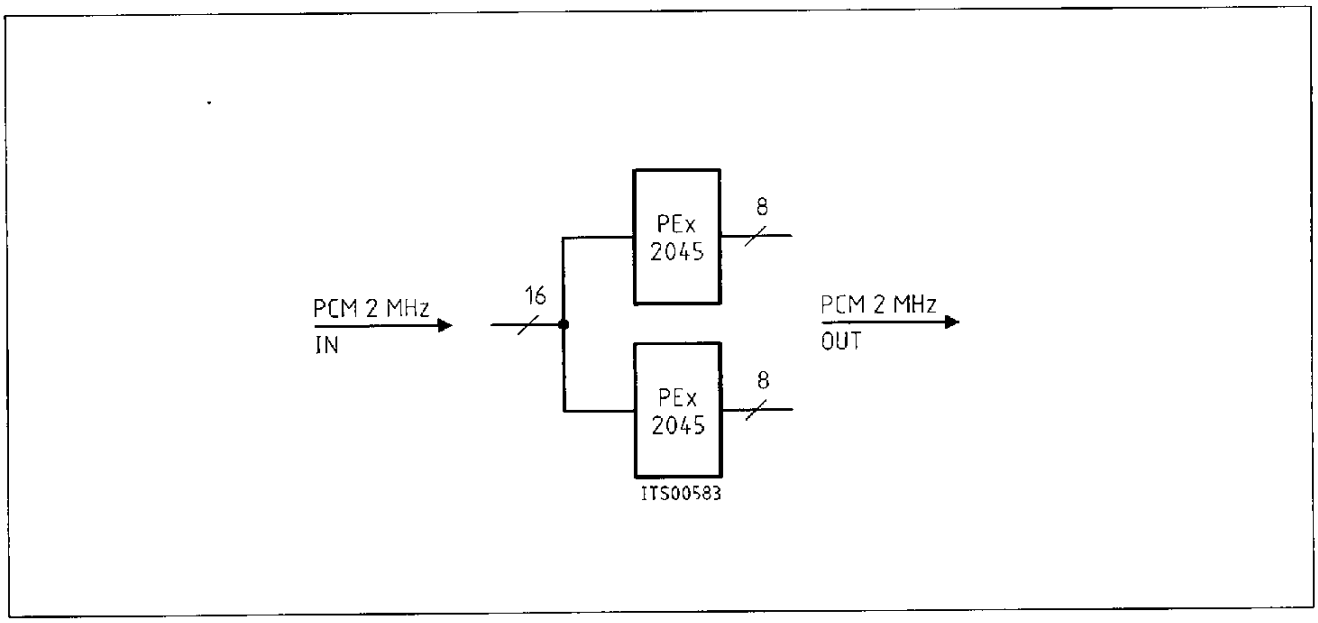


Figure 3
Memory Time Switch 16/16 for a Non-Blocking 512-Channel Switch

This is possible due to the tristate capability of the PEx 2045.

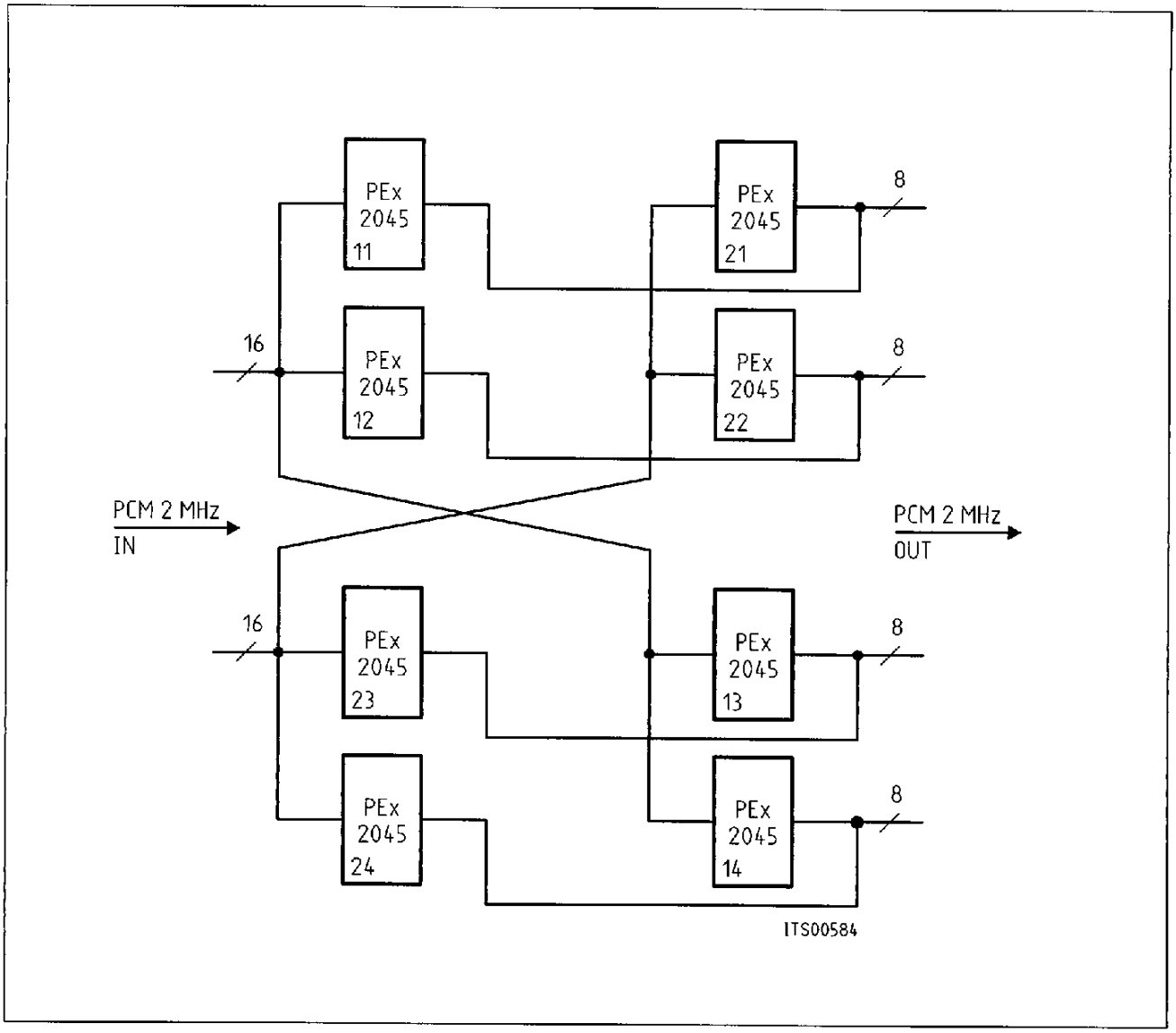


Figure 4
Memory Time Switch 32/32 for a Non-Blocking 1024-Channel Switch

Figure 5 shows the architecture of a primary access board with common channel signaling using four CMOS devices. It exhibits the following functions:

- Line Interface (PEB 2235)
- Clock and Data Recovery (PEB 2235)
- Coding/Decoding (PEB 2035)
- Framing (PEB 2035)
- Elastic Buffer (PEB 2035)
- Switch (PEx 2045)
- System Adaptation (PEx 2045)
- Data Link Signaling Handling (SAB 82520)
- µP Interface (all devices)

Since the PEx 2045 is a switch for 256 output channels and the SAB 82520 is actually a dual channel controller a quad primary access unit with a non-blocking switch requires a total of 11 devices,

- 4 IPAT® (PEB 2235)
- 4 ACFA (PEB 2035)
- 2 HSCC (SAB 82520)
- 1 MTSC (PEx 2045),

as shown in **figure 6**.

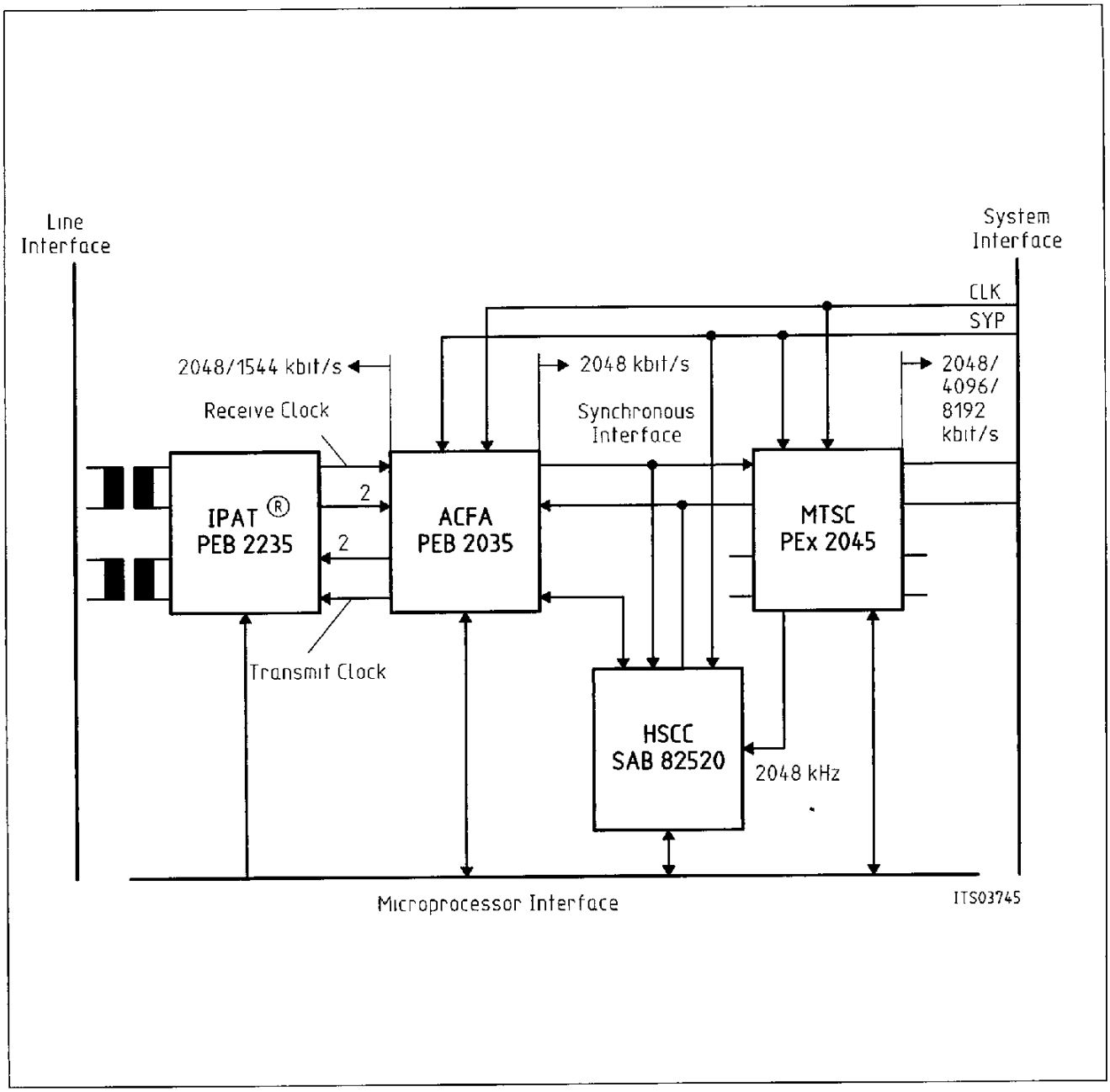


Figure 5
Architecture of a Primary Access Board

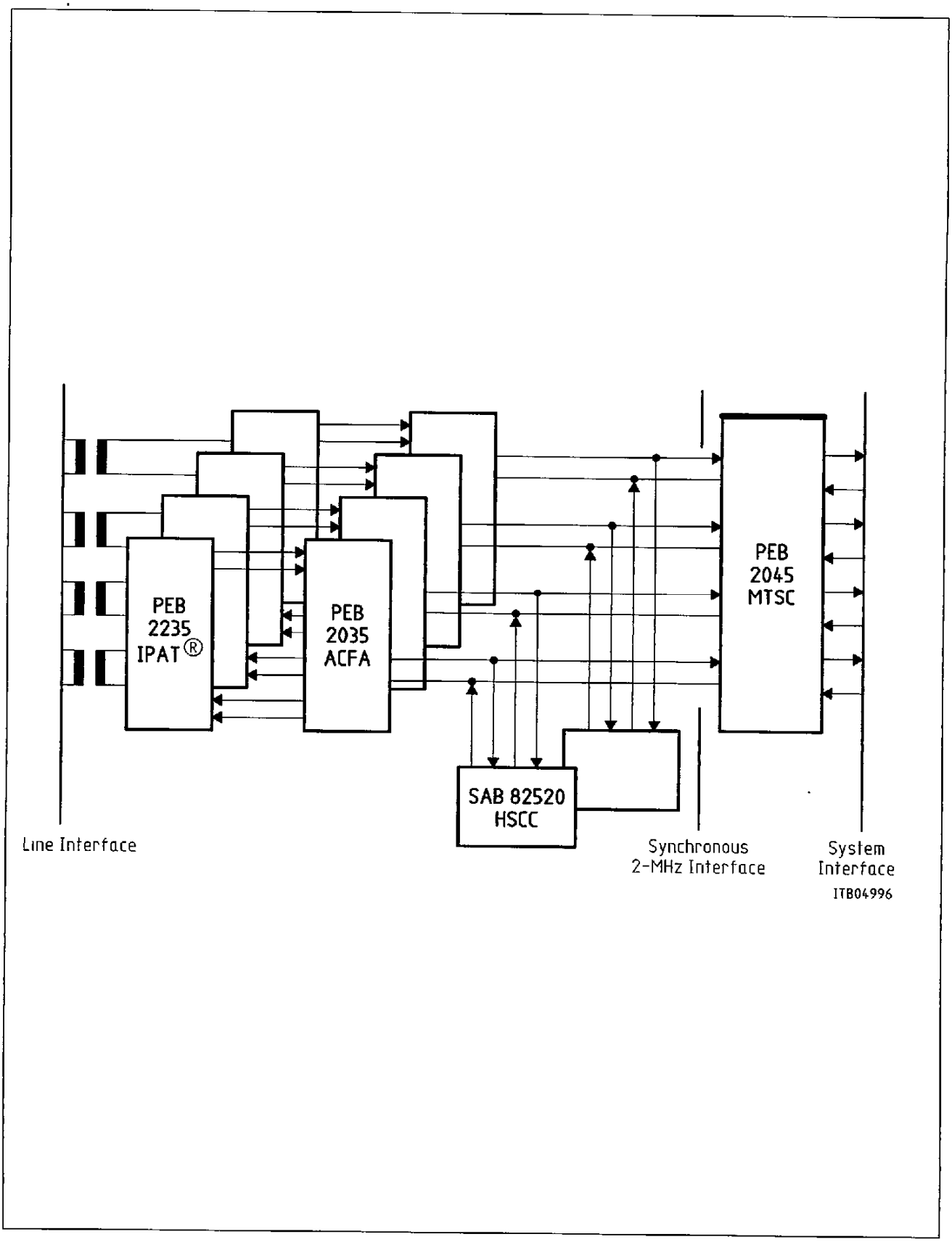


Figure 6
Realization of a Quad Primary Access Interface and Switch with 11 CMOS Devices

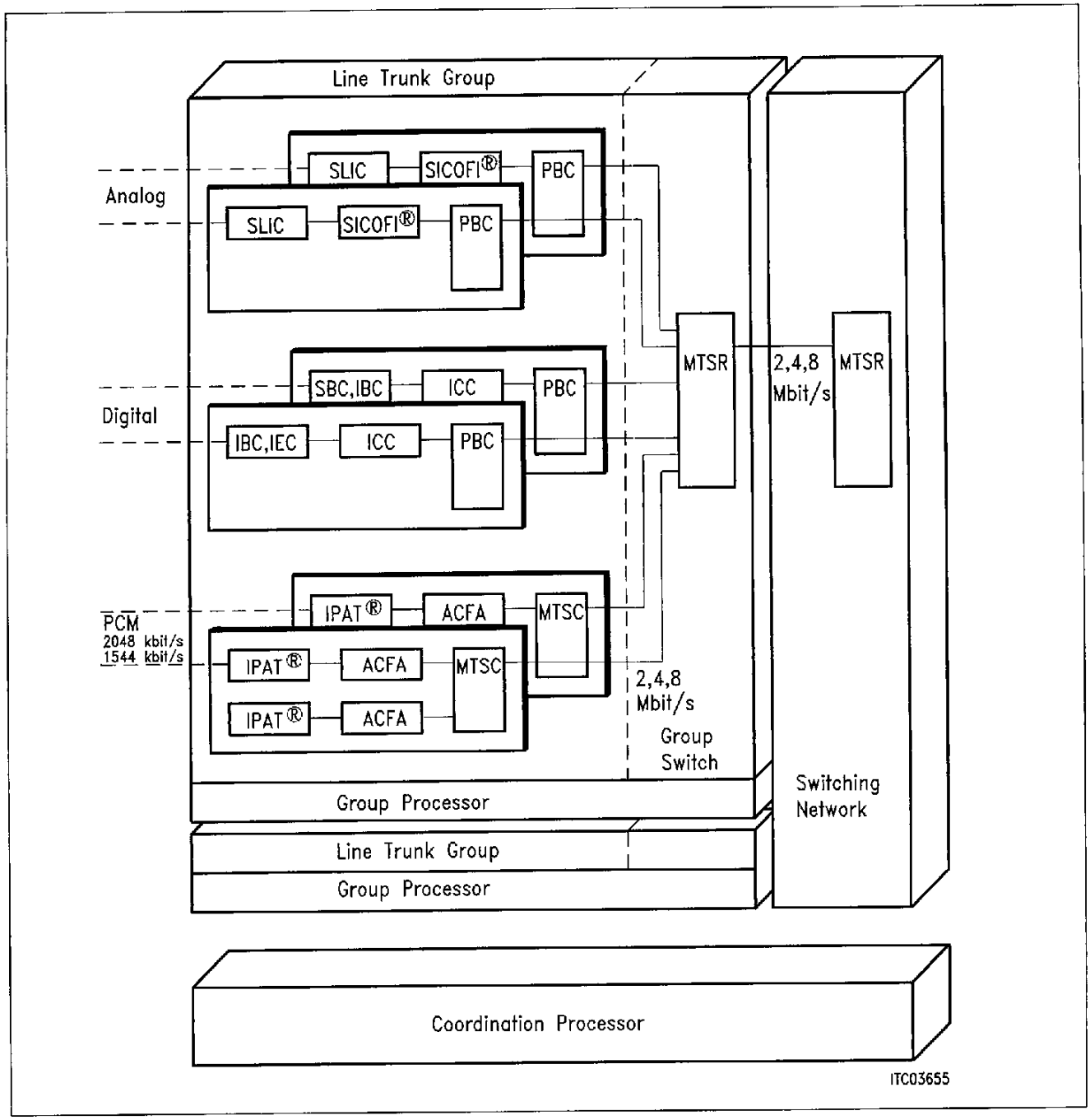


Figure 7
Basic Connections to a Digital Switching System

Figure 7 shows the PEx 2045 in its different applications in a digital switching system. It is used here as the main device in the switching network (SN), as a group switch (GS) to connect different digital or analog subscriber line modules (SLMA, SLMD) or digital interface units (DIU) with one another and as the interface device for the digital interface units. The SLICs and SICOFIs (PEB 2060) are subscriber line drivers and codec-filter devices, respectively, for the analog line. SBC (PEB 2080), IEC (PEB 2090), IBC (PEB 2095) and ICC (PEB 2070) are the layer-1 and layer-2 ISDN devices for the digital line. The peripheral board controller PBC (PEB 2050) multiplexes the different lines in a subscriber line module to the 2- or 4-Mbit/s highways, which are input to the group switch.

2 Functional Description

The PEx 2045 is a memory time switch device. It can connect any of 512 PCM input channels to any of 256 output channels.

The input information of a complete frame is stored in the on-chip 4-Kbit speech memory SM (**see figure 8**). The incoming 512 channels of 8 bits each are written in sequence into fixed positions in the SM. This is controlled by the input counter in the timing control block with a 8-kHz repetition rate.

For outputting, the connection memory (CM) is read in sequence. Each location in CM points to a location in the speech memory. The byte in this speech memory location is read into the current output time-slot. The read access of the CM is controlled by the output counter which also resides in the timing control block.

Hence the CM needs to be programmed beforehand for the desired connection. The CM address corresponds to one particular output time-slot and line number. The contents of this CM-address points to a particular input time-slot and line number (now resident in the SM).

The PEx 2045 works in standard configuration for usual switching applications, and in the primary access configuration where it realizes, together with the PEB 2035 (ACFA) and the PEB 2235 (IPAT), the system interface for up to four primary multiplex access lines.

In the following chapters the functions of the PEx 2045 will be covered in more detail.

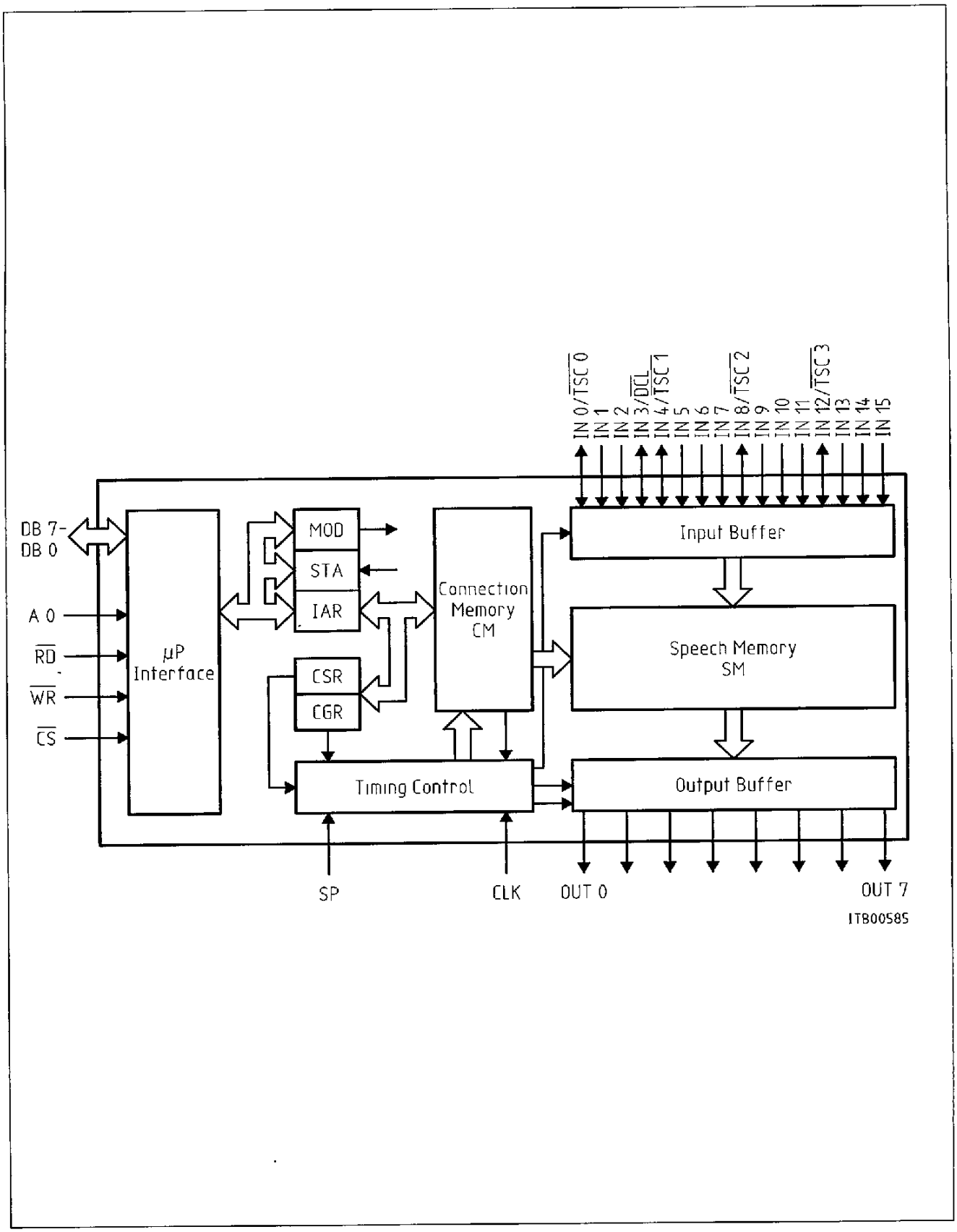


Figure 5
Block Diagram of the PEx 2045

2.1 Basic Functional Principles

Preparation of the Input Data

The PEx 2045 works in 2048-, 4096- or 8192-kbit/s PCM systems. The frame frequency is 8000 Hz in all 3 types of systems. Therefore a frame consists of 32-, 64- or 128 time-slots of 1 byte each, respectively. In order to fill the speech memory, which has a fixed capacity of 512 channels, either 16-, 8- or 4 input lines are necessary, respectively. Thus, in 4- and 8-MHz systems only some of the 16 input lines can be used.

Moreover, the PEx 2045 can also work with two different input data rates simultaneously. In this case some of the PCM input lines operate at one data rate, while others operate at another. **Table 1** states how many input lines are operating at the different data rates for all possible input data rate combinations. In the following they will be referred to as input modes.

The input mode the PEx 2045 is actually working in has to be programmed into the mode register, bits MI1, MI0, MO1, MO0. In **chapter 4.1** you will find a complete description which input line is connected to which system, for each of the input modes.

Table 1
Possible Input Modes

Input Modes				Type
16	×	2048	kbit/s	Single mode
8	×	4096	kbit/s	Single mode
4	×	8192	kbit/s	Single mode
2 × 8192	+	8 × 2048	kbit/s	Mixed mode
4 × 4096	+	8 × 2048	kbit/s	Mixed mode

The PEx 2045 runs with either a 4096- or a 8192-kHz device clock as selected with CFG:CPS. Data rates and clock frequencies may be combined freely. However, processing 8192-kbit/s data, a 8192-kHz clock must be supplied.

The preparation of the input data according to the selected input mode is made in the input buffer. It converts the serial data of a time-slot to parallel form.

In standard configuration time-slot 0 begins with the rising edge of the SP pulse as shown in upper half of **figure 9** denoted CSR: (0000XXXX).

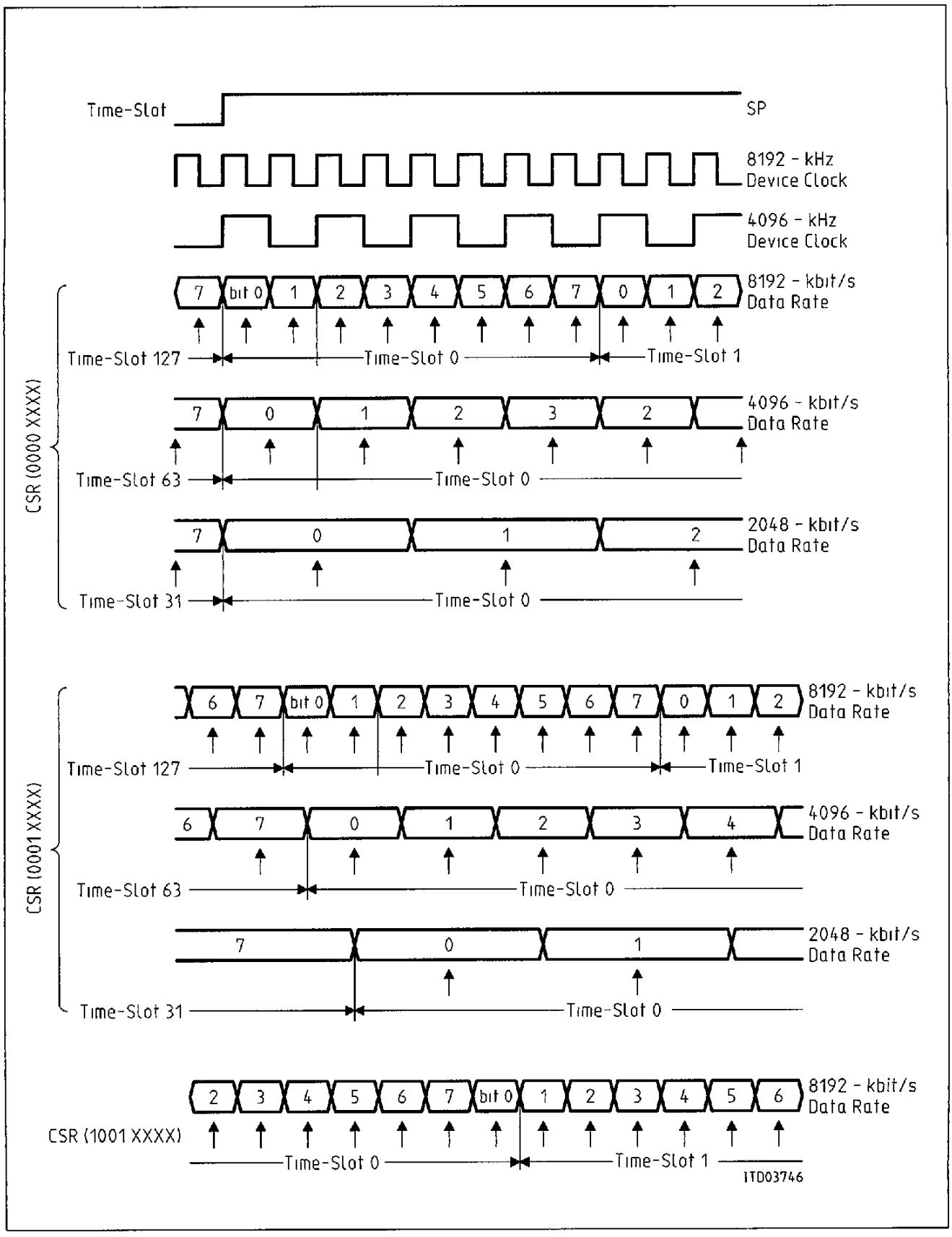


Figure 9
Latching Instant for Input Data

As can be seen there the beginning of a input time-slot is defined such, that the input lines have settled to a stable value, when the datum is actually sampled.

4096- and 8192-kbit/s data is sampled in the middle of the bit period at the falling edge of the respective data clock. 2048-kbit/s data is sampled after 3/4 of the according bit period, i.e. with the rising edge of the 4th 8192-kHz clock cycle or the falling edge of the 2nd 4096-kHz clock cycle of the considered bit period.

In the primary access configuration a different timing scheme may apply to the odd input lines. They are affected by the content of the clock shift register (CSR), which can be programmed via the µP interface (**see section Indirect Register Access**).

The clock shift register holds the information, how the frame structure is shifted in the primary access configuration. Its content defaults to 00_H after power up and is also set to this value, whenever the standard configuration is selected.

The four most significant bits of the clock shift register are of interest for the input lines. They only affect the odd input lines (**see section Clock Shift Register Access**): The frame structure can be advanced by the number of bit periods programmed to the RS2, RS1 and RS0 bits of the CSR. For example, programming the CSR with (1100XXXX) a new frame starts 6-bit periods before the rising edge of the SP pulse.

Selecting RRE to logical 1 the frame is delayed by half a bit period (**see figure 9**). The data is then sampled in the middle of the respective bit period for all data rates.

The last line of **figure 9** shows the sampling instants for the CSR entry (1001XXXX). Then the input frame is advanced by 4-bit periods and delayed by a half resulting in an 3 1/2-clock period advancement of the input frame. For further examples refer to **figure 21**.

Thus the frame structure may be selected to begin at any 1/2-bit period value between a resulting advancement of 7-bit periods and a resulting delay of 1/2 a bit period.

Setting CSR = $0X_H$ the same timing conditions apply to even and odd inputs. Then all system interface inputs are processed in the same way they are in the standard configuration.

Speech Memory

The prepared input data is written into the speech memory SM. It has a capacity of 512 bytes to store one frame of all active input lines. The destination SM addresses are supplied by the input counter, which resides in the timing control block. They ensure that a certain input channel is always written to the same physical speech memory location. The input counter is synchronized with the rising edge of the SP signal.

The 9-bit addresses to read the speech memory are supplied by the connection memory. These are programmable and need not follow any recognizable sequence.

Write and read accesses of the SM occur alternately.

Connection Memory

The connection memory (CM) is a RAM organized as 256 × 10 bits. It contains the 9-bit speech memory address and a validity bit for the 256 possible output channels. While the speech memory address points to a location in the SM, the validity bit is processed in the timing control block: If the TE bit in the mode register (**see paragraph 4.1**) is set to logical 0, the validity bit is directly

forwarded to the output buffer as the tristate control signal. Otherwise (if TE = high), an all-zero speech memory address causes the output for the associated channel to be tristate. In this case the all-zero speech memory address (time-slot 0 on output line 0) cannot be used for switching purposes.

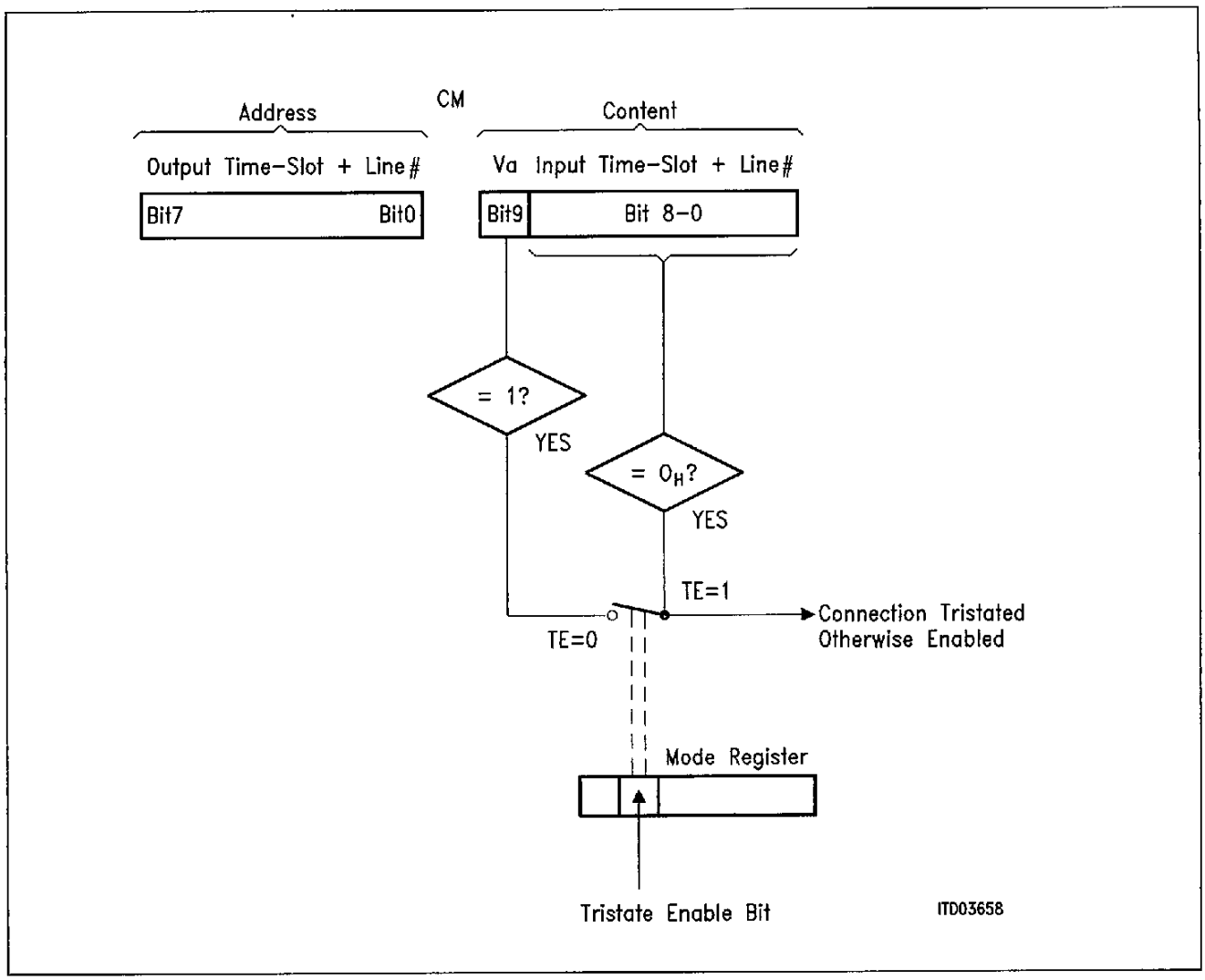


Figure 10
The Influence of the Connection Memory on the Output Validity

The CM is written via the µP interface using the indirect register access scheme (**see section Indirect Register Access**). It is read using addresses supplied by the output counter which resides in the timing control block. The output counter generates addresses that form an enumerative sequence. Thus the connection memory is read cyclically and establishes the correct time-slot sequence of the outputs.

The output counter is synchronized with the falling and rising edge of the SP signal in standard and primary access configurations, respectively.

The connection memory addresses and data encode the number of the output and input channels, respectively. For a detailed description of the code please refer to **section Indirect Register Access and Connection Memory Access.**

Output Buffer

The output buffer rearranges the data read from the speech memory. It basically converts the parallel data to serial data. Depending on the tristate control signal from the timing control block the output buffer outputs the data or switches the line to high impedance.

The mode register (MOD) bits MI1, MI0, MO1 and MO0 control this process. The possible output modes are listed in **table 2**.

Table 2
Possible Output Modes

Output Modes				Type
8	×	2048	kbit/s	Single mode
4	×	4096	kbit/s	Single mode
2	×	8192	kbit/s	Single mode
1 × 8192	+	4 × 2048	kbit/s	Mixed mode
2 × 4096	+	4 × 2048	kbit/s	Mixed mode

Figure 11 shows, when the single bits are output. In standard configuration they are clocked off at the rising clock edge at the beginning of the considered bit period. Time-slot 0 starts two t_{CPS} before the falling edge of the SP pulse.

In primary access configuration the even output lines are affected by the XS2, XS1, XS0 and XFE entries in the clock shift register. The output frame is synchronized with the rising edge of the SP-signal.

Assuming a CSR entry $X0_H$ the output frame starts with the rising edge of the SP pulse. Programming the XS2, XS1 and XS0 bits with a value deviating from binary 000 the output frame is delayed by 8_D - (XS2, XS1, XS0) $_B$ bit periods. E.g., a CSR entry of (XXXX0010) delays the output frame by 7-bit periods relative to the rising SP-pulse edge.

Programming CSR:(XXXXXXX1) the output frame is delayed by another half a device clock period. In **figure 11** the outputting instants are shown for a device clock of 4096 and 8192 kHz and a CSR:(XXXX0001).

The last line in **figure 11** shows an even 8192-kbit/s output line for the CSR entry (XXXX0111) and a 8192-kHz device clock. The output frame is delayed by 5 1/2-bit periods. For further examples refer to **figure 21**.

If the CSR is programmed such that XS2 is identical to RS2, XS1 to RS1, XS0 to RS0 and RRE to XFE the time-slot boundaries of input and output coincide. Programming XS2, XS1, XS0 as well as RS2, RS1, RS0 to logical 0 input and output time-slots coincide. Otherwise the system interface output frame starts one time-slot after the system interface input. This can be seen comparing for example the lines 0100XXXX and XXXX0100 in **figure 21**.

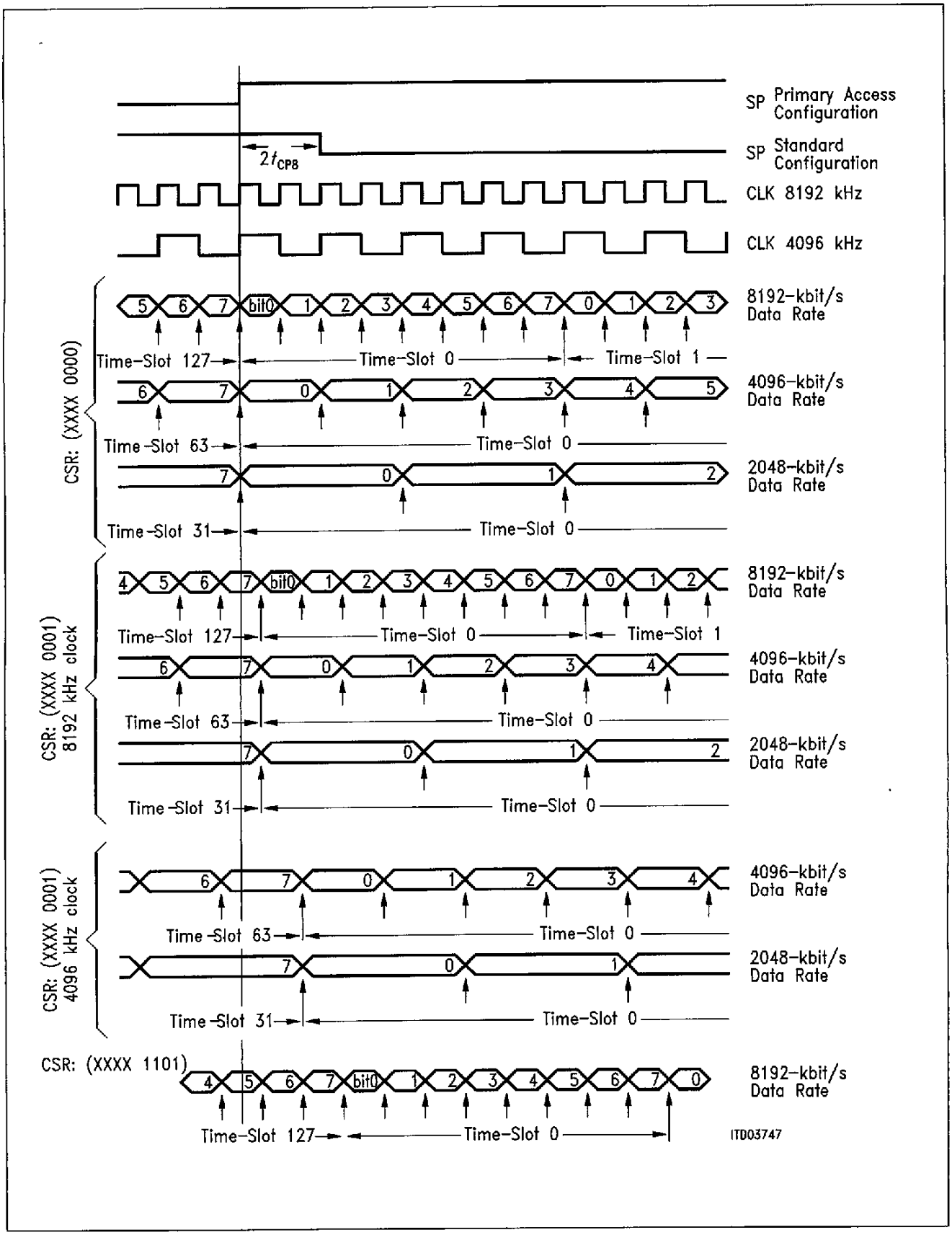


Figure 11
Clocking Off Instant of Output Data

2.2 Microprocessor Interface and Registers

The PEx 2045 is programmed via the µP interface. It consists of the data bus DB7 ... DB0, the address bit A0, the Write ($\overline{WR}$), the Read ($\overline{RD}$) and Chip Select ($\overline{CS}$) signal, as shown in **figure 12.**

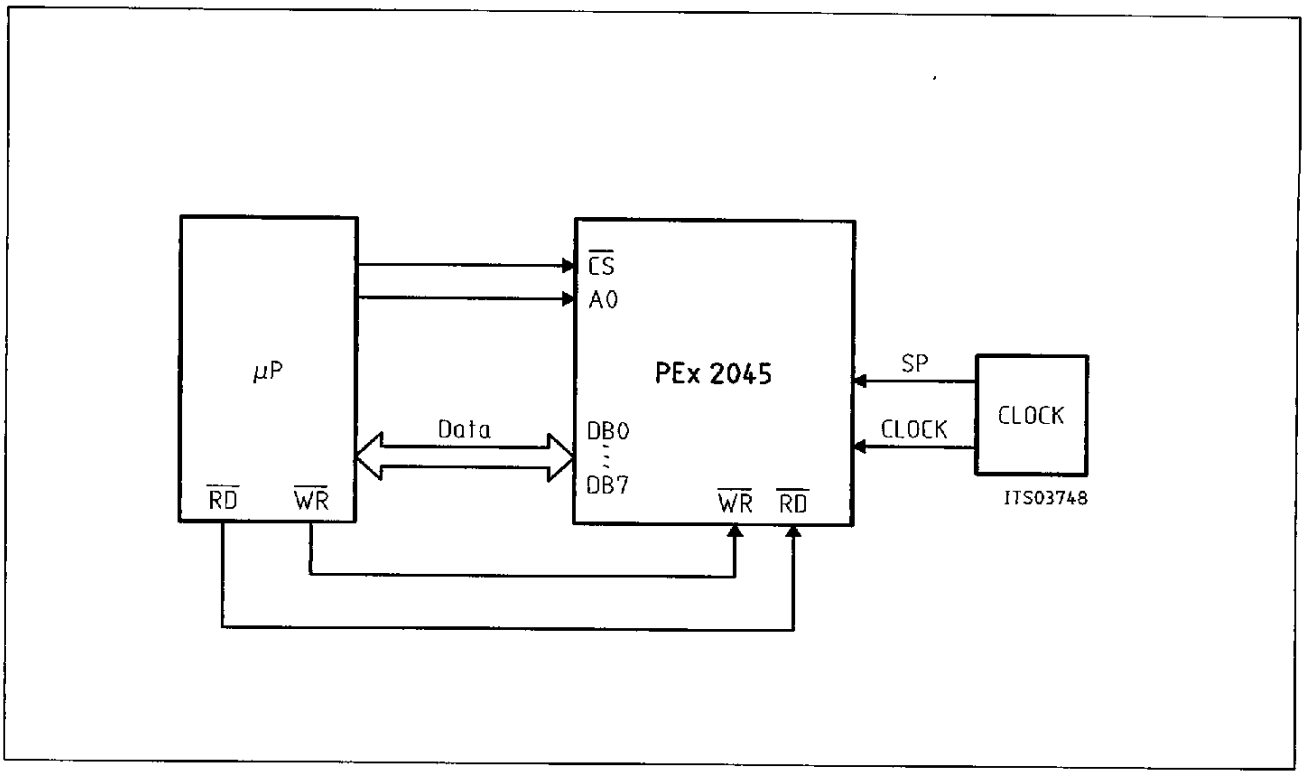


Figure 12
The PEx 2045 Controlled by a Microprocessor

To perform any register access, CS has to be zero. This pin is provided, so that a single chip can be activated in an environment where one microprocessor controls many slave processors (**see figure 20**).

The PEx 2045 incorporates 4 user programmable registers,

- the mode register (MOD)
- the status register (STA)
- the configuration register (CFR) and
- the clock shift register (CSR)

as well as

- the connection memory (CM).

The mode register is a write only register; the status register is a read only register. CFR, CSR and CM can be read and written. The single address bit A0 does not offer enough address space to encode all access possibilities. Therefore the indirect access scheme is used to access the CFR, CSR and CM. It uses the indirect access register (IAR), which is provided on chip.

Using the 3 signals A0, $\overline{WR}$ and $\overline{RD}$ the IAR, MOD and STA registers can be identified according to **table 3**.

Table 3
Addressing of the Direct Registers

A0	Write Operation	Read Operation
0	MOD	STA
1	IAR	IAR

The A0 address distinguishes between the IAR and the directly accessible registers. The $\overline{WR}$ and $\overline{RD}$ strobes combined with an A0 equal to logical 0 identify the mode- and status registers, respectively. The data bus contains the associated information. In the following paragraphs the indirect register access and the register contents will be described.

Indirect Register Access (A0 = 1)

To perform an indirect register access 3 consecutive instructions have to be programmed. One indirect register access has to be completed before the next one can begin. The 3 instructions of the indirect access operate on the indirect access register. It receives, in sequence the control byte, the data byte and the address byte according to **table 4**.

Table 4
IAR Byte Structure

Bit 7							Bit 0	
0	0	K1	K0	0	0	C1	C0	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The data byte contains the information which shall be written into the connection memory or the indirect registers, i.e. the CSR or the CFR. The address byte indicates which one of the indirect registers shall be accessed or in which location of the CM the data shall be written. The control byte determines whether the connection memory or one of the indirect registers shall be accessed and whether a write or read operation shall be performed.

Before an indirect access is started, the Z- and B-bits of the status register must be 0. With the first instruction the Z bit is set (**see chapter 4.2**). After the third instruction the PEx 2045 accesses the physical register or memory location. This access requires maximally 900 ns. After the access finishes the Z bit is reset. The 3 instructions are separated by intervals where both $\overline{WR}$ and $\overline{RD}$ are in a high state.

Figure 13 illustrates a write operation on the IAR.

It is possible to read or write the direct access registers (i.e. the mode or status register) while an indirect access is in progress. Thus the status register may be read in the time intervals that separate the three sequential indirect access instructions. Also, the current indirect access may be aborted by setting the MOD:RI.

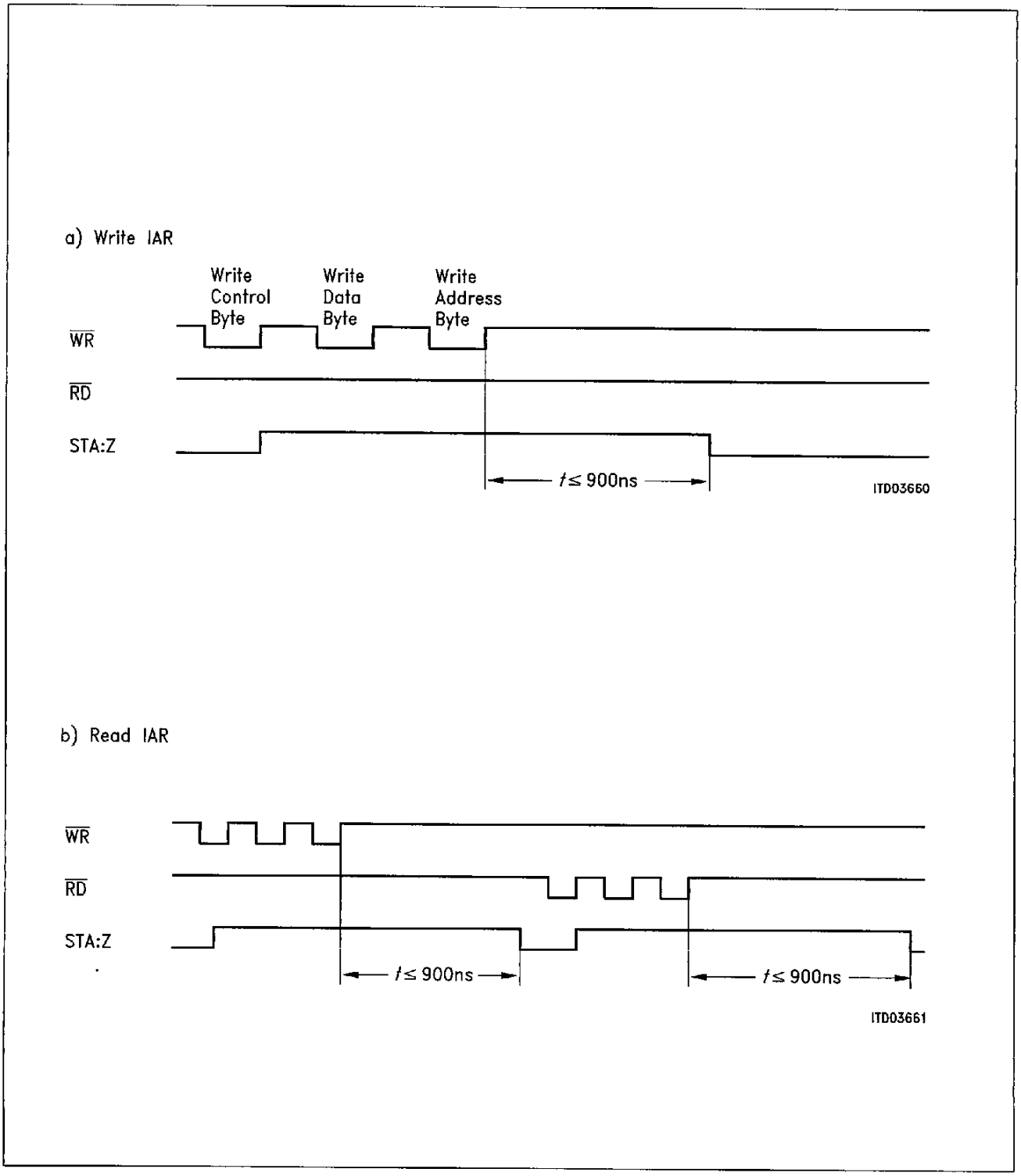


Figure 13
Timing Diagrams for IAR

Bits K1 and K0 of the control byte determine whether a CM or an indirect register access shall be performed. When K1 and K0 are both logical 1, one of the indirect registers is accessed. For all other combinations the connection memory is accessed.

Table 5
Decoding the K1 and K0 Bits

K1	K0	Accessed Register	R/W
0	0	CM	R
0	1	CM	W
1	0	CM	W
1	1	indirect register	R or W

In the case of a CM access the K1 and K0 bits also indicate the type of the access: One bit being logical 1 indicates a write, both bits being logical 0 a read operation.

The same distinction function is performed by bit C0 of the control byte in the case of an indirect register access. According to **table 6** a high on C0 initiates a read, a low a write operation. The value of the C1 bit is of no significance in this application. However to avoid future incompatibility problems, it is strongly recommended to set C1 to logical 0.

The address byte holds the CM address for a connection memory access, for indirect register access it indicates which one of the two indirect registers is accessed. A hexadecimal FE_H addresses the configuration register, a hexadecimal FF_H the clock shift register. **Table 6** lists all possible choices of indirect register accesses.

Table 6
Addressing of the Indirect Registers

K1	K0	C0	Address Byte (hex)	Access
1	1	1	FE	CFR read
1	1	0	FE	CFR write
1	1	1	FF	CSR read
1	1	0	FF	CSR write

The data to be written to the different registers or the CM reside in the data byte. For CM accesses not 8 but 10 bits are written into the selected location. The two bits in excess come from the C0 and C1 bits of the control byte and are interpreted as the most significant bits of the data word. (D9 and D8). Accordingly the 3 CM access instructions are interpreted as shown in **table 7**.

Table 7
Connection Memory Access IA Byte Structure

Bit 7							Bit 0	
0	0	K1	K0	0	0	D9	D8	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The following example illustrates how an indirect memory access works.

The instruction sequence

00110000

01010101 A0 = 1, $\overline{WR}$ = 0, $\overline{RD}$ = 1, $\overline{CS}$ = 0

11111111

writes the hexadecimal value 55_H into the clock shift register.

The instruction sequence

00010010

00000000 A0 = 1, $\overline{WR}$ = 0, $\overline{RD}$ = 1, $\overline{CS}$ = 0

10101010

writes the hexadecimal value 200_H into the connection memory location AA_H thus tristating the output.

To read the indirect registers or the CM two sequences of 3 instructions each have to be programmed.

In the first sequence the PEx 2045 is instructed which register or CM address to read. The data transferred to the PEx 2045 in this first sequence is of no importance.

With the first write instruction STA:Z is set.

After the first 3 instructions the PEx 2045 needs 900 ns to read the specified location and to write the result to the IAR. It overwrites the data byte and in the case of a CM-read operation additionally bits 1 and 0 of the control byte. The status register bit Z is reset after maximally 900 ns. Then 3 read operations follow. Again, STA:Z is set with the first read instruction. The 3 instructions read 3 bytes from the IAR. **Figure 13b** shows this procedure. The data byte and, in the case of a CM-read operation, the C1 and C0 bits in the control byte show the values read from the indirect registers or the CM. The K0, K1 bits and the address byte have not changed their values since the proceeding write instruction sequence.

After the third read operation the PEx 2045 needs another 900 ns to reset the indirect access mechanism and the Z bit in the status register.

With the following instruction sequence

00000001

11111111 A0 = 1, $\overline{WR}$ = 0, $\overline{RD}$ = 1, $\overline{CS}$ = 0

10101010

the byte sequence

11001110

00000000 A0 = 1, $\overline{WR}$ = 1, $\overline{RD}$ = 0, $\overline{CS}$ = 0

10101010

can be read.

The CM location AA_H, which has been written to 200_H in the last example is read again.

Bits 7, 6, 3, 2, of the control byte showing logical 0 in the first byte at the beginning of the read access reappear as logical 1 in the fourth byte. This is due to the internal device architecture. These bits are unused and are recommended to be set to logical 0 to avoid future incompatibility problems.

In CSR and CFR read accesses, bit 1 and bit 0 (C1 and C0) of the read control byte have a value of logical 1.

Register Contents

You will find a detailed description of the different register contents in **section 4**. This paragraph only gives a short overview of the different registers:

The mode register contains bits to determine the operation mode and the output tristating scheme, to control the CM reset mechanism, to interrupt the indirect access mechanism and to switch the chip to standby.

The status register consists of 3 bits. They tell whether the PEx 2045 is busy resetting its connection memory or performing an indirect access or whether operational conditions have occurred which might lead to a partial or complete loss of data in the connection and speech memory. Bits 4 to 0 of the status register default to logical 0.

The clock shift register holds information on how the frame structure is advanced or delayed relative to the synchronization pulse. It is only active for the system interface in the primary access configuration. **See chapter 2.4.** In standard configuration it is set to logical 0.

The configuration register is used to select the device clock frequency and the configuration in which the device is used. The most significant 6 bits default to logical 1, if the register is read.

The connection memory content and address contain the connection information. Specifics are explained in the following sections.

2.3 Standard Configuration

A logical 1 in the CFS bit of the configuration register sets the PEx 2045 in standard mode (default after power up). All modes from **table 9** can be used. The space switch mode (MI1, MI0, MO1, MO0 = 0_H) is a special mode and will be covered in **chapter 2.5.**

It has to be ensured that the data rate is not higher than the selected device clock (4096 or 8192 kHz).

In this application 512 channels per frame are written into the speech memory. Each one of them can be connected to any output channel.

According to **table 10** and **table 14** and depending on the selected mode the least significant bits of the connection memory address and data contain the logical pin numbers, the most significant bits the time-slot number of the output and input channels.

The following example explains the programming sequence.

Time-slot 7 of the incoming 8192-kbit/s input line IN14 shall be connected to time-slot 6 of the output line OUT 5 of an 2048-kbit/s system. According to **table 10** in 8192-kbit/s systems the input line IN14 is the logical input line 2. Output line number and logical output number are identical to one another.

Therefore the following byte sequence on the data bus has to be used to program the CM properly (**see table 14**):

00010000

00011110

00110101

The frame, for all input channels, starts with the rising edge of the SP signal. The frame for all output channels begins two t_{CP8} (with 8192-kHz device clock) or one t_{CP4} period (4096-kHz device clock) before the falling SP edge. The period of time between the rising and the falling edge of the SP pulse should be

$t_{SPH} = (2 + N \times 4)\, t_{CP8} \qquad (0 \leq N \leq 255)$

$= (1 + N \times 2)\, t_{CP4}$

N is an user defined integer. By varying N, t_{SPH} can be varied in 2048-kHz clock period steps. For an example using N = 2 refer to **figure 14.**

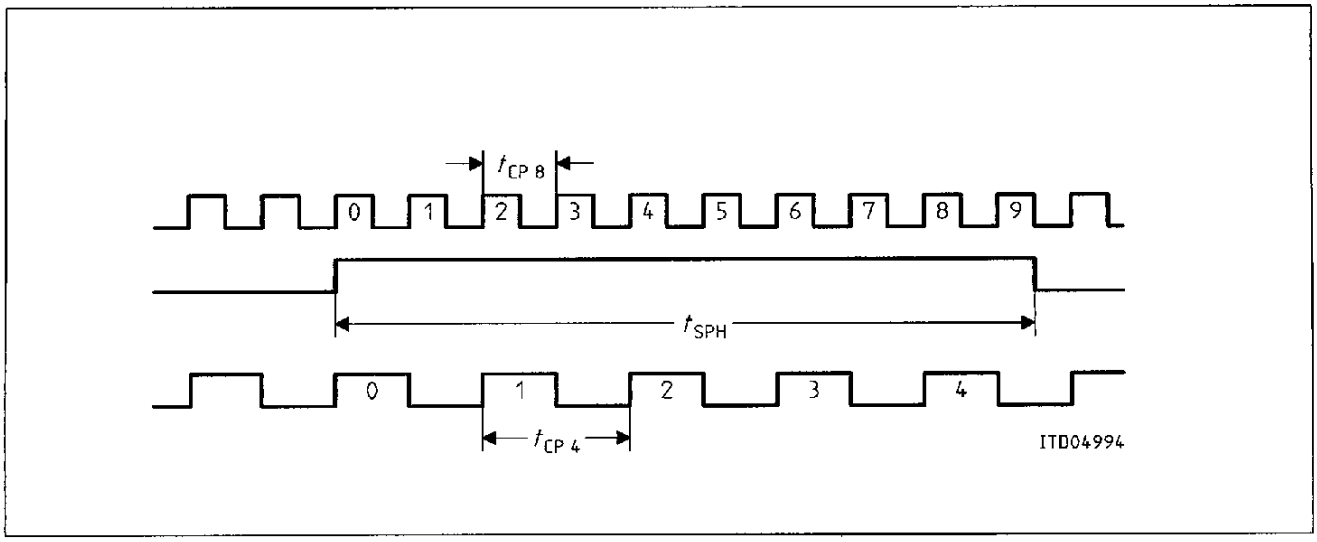


Figure 14
SYP Duration for N = 2

The device is synchronized after 3 SP pulses (**see chapter 3.2**).

2.4 Primary Access Configuration

A logical 0 in the CFS bit of the configuration register selects the PEx 2045 for primary access applications. In this case the PEx 2045 is an interface device connecting a standard PCM interface (system interface) with another PCM interface e.g. an intermediate interface for connections to primary loops (synchronous interface). For both a serial interface is provided.

- The synchronous 2048-kbit/s interface consists of four input and four output lines with a bit rate of 2048-kbit/s. This interface can be used to connect the PEx 2045 to up to four primary trunk lines via coding / decoding devices with frame alignment function (e.g. PEB 2035 ACFA) and line transceivers with clock and data recovery (e.g. PEB 2235 IPAT) and to signaling processors (e.g. the SAB 82520 HSCC).
- The system interface is not confined to one data rate but can operate at the full choice of the PEx 2045 data rates: 2048, 4096 and 8192 kbit/s. A clock shift in a range of 7 1/2 clock steps with half clock step resolution may be programmed independently for inputs and outputs.

The frame for all input- and output lines starts with the rising edge of the SP signal.

In the primary access mode the signals $\overline{TSC0}$, $\overline{TSC1}$, $\overline{TSC2}$ and $\overline{TSC3}$ indicate when the associated system interface output is valid. The signal DCL supplies a 2-MHz clock which can be used for other devices at the synchronous interface, e.g. the High Level Serial Communication Controller HSCC (SAB 82520).

In the primary access configuration only those modes which support at least 4 input and 4 output lines at 2048 kbit/s can be used. These are the modes MI1, MI0, MO1, MO0 = 0_H, A_H, F_H (**see table 9**). Programming the CM in the primary access configuration is described in **tables 17 and 18.** The least significant 2 bits of the data byte and the least significant bit of the address byte determine the type of interface, the more significant bits define the logical line number and time-slot number.

The following example explains how to program the CM in primary access configuration and how the clock shift works:

Time-slot 31 of the synchronous 2048-kbit/s interface logical line 2 shall be switched to the system interface logical line 1 of a 2048-kbit/s system, time-slot 2. The system interface logical output line 1 and the synchronous interface logical input line 2 correspond to the pins OUT 2 and IN 10, respectively (**table 11**). The programmed instruction sequence on the data bus for that connection reads (**see table 17 and 18**):

00100001
11111010
00010010

In the same application the instruction sequence

00010001
11111101
00010001

connects the time-slot 31 of the system interface logical line 3 (IN 13) to the synchronous interface logical line 0 (OUT 1) time-slot 2.

Assuming CSR:00_H the frame for input and output lines starts with the rising edge of the SP pulse. The CSR entry 11011101 shifts the beginning of the frame for the system interface: The input frame is advanced by 6 data bits because of the shift, but delayed by the 1/2-bit delay facility, resulting in a 5 1/2-bit period advancement. The output frame structure is delayed by 2 data bit periods and one half of a device clock period. **Figure 15** illustrates these 2 connections for a 4096-kHz device clock.

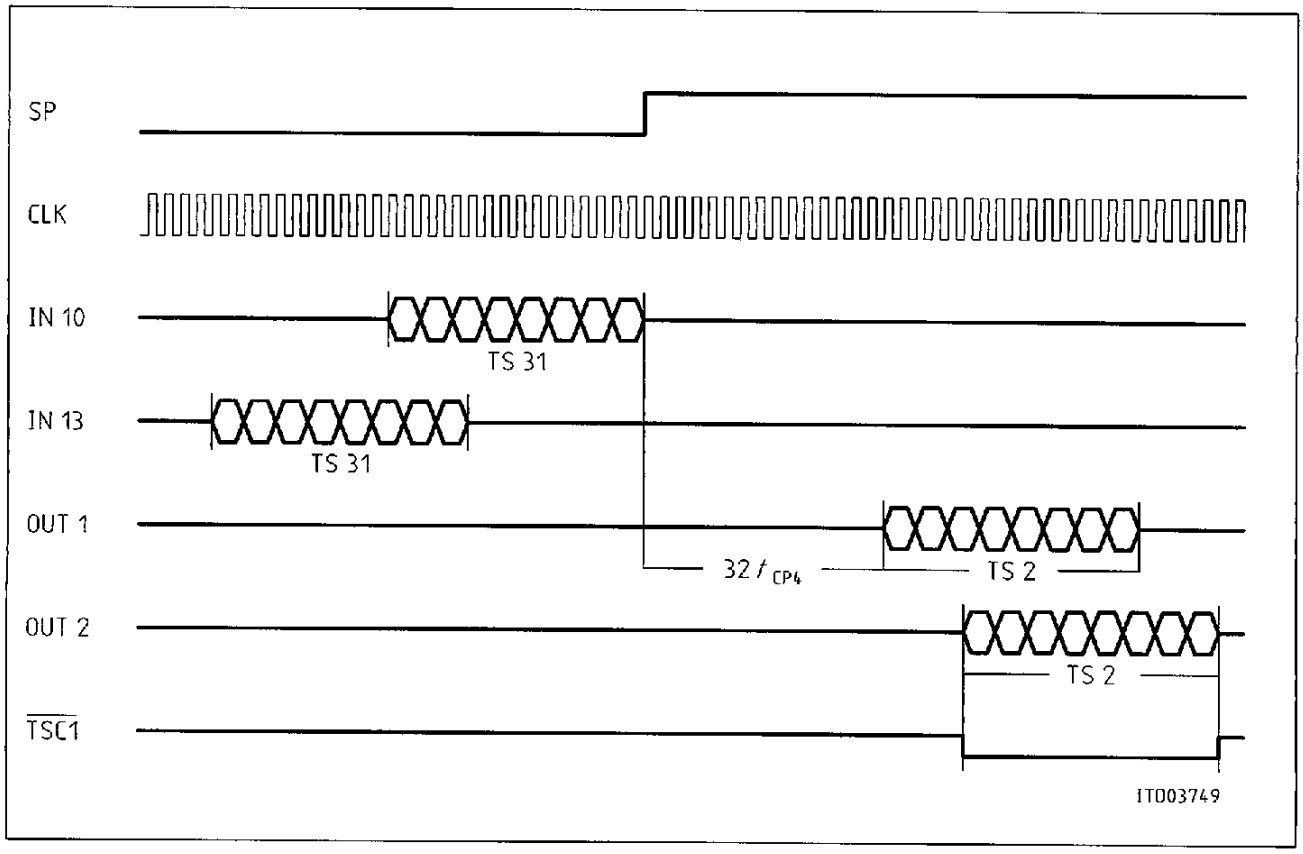


Figure 15
Example Connections in the Primary Access Configuration

According to **figure 16** in the primary access configuration the connection memory is usually programmed to switch the system and synchronous interface inputs to the synchronous and system interface outputs, respectively. However, it is also possible to connect the system interface inputs to the system interface outputs as well as the synchronous interface inputs to the synchronous interface outputs. This connection possibility allows for test loops at the system and the synchronous interfaces.

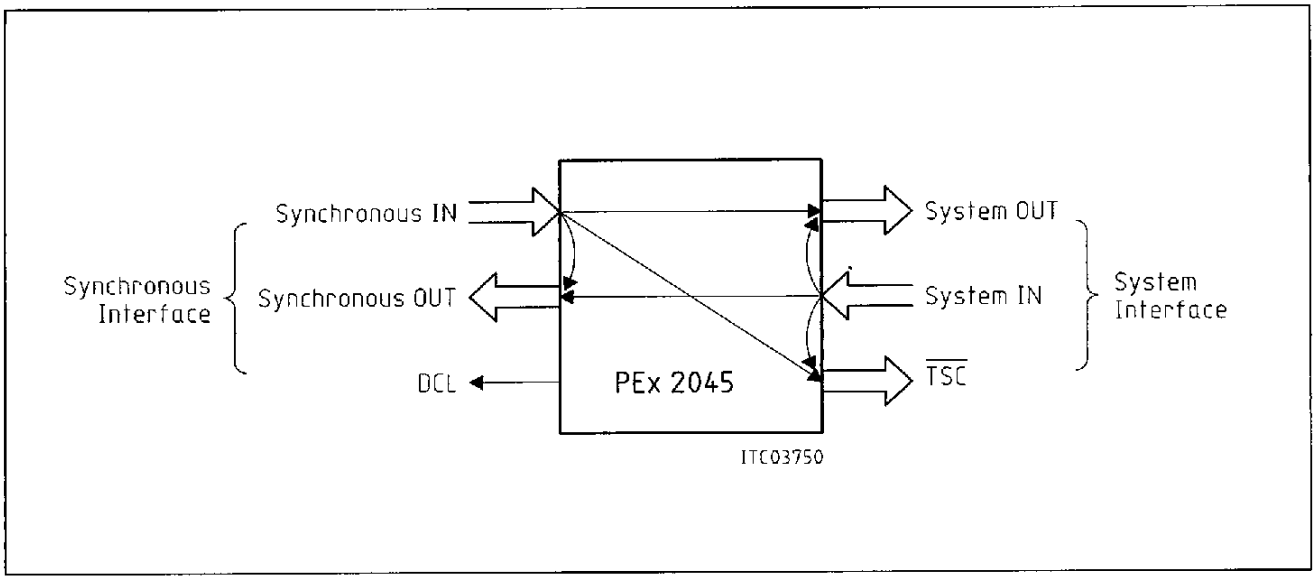


Figure 16
Connection Choices in the Primary Access Configuration

2.5 Space Switch Mode

The space switch mode is selected by the mode bits MI1, MI0, MO1, MO0 = D_H.

In the space switch mode the basic operational principles differ from those outlined in **chapter 2.1**. In the speech memory only a quarter frame is stored restricting the connection capabilities of the PEx 2045.

All 16 input lines run at a data rate of 8192 kbit/s delivering 2048 bytes of data in each frame. Since the speech memory can only hold 512 bytes, the data bytes must be read within a quarter of a frame period to be outputted on one of the two 8192-kbit/s output lines.

In space switch mode it is recommended that the SP pulse be 282 t_{CP8} long (N = 70). For proper functionality the time-slot numbers of a programmed connection must be equal. In the following only this case considered.

The output time-slot is encoded in the connection memory address. Since the input time-slot has to be the same it is not necessary to fully specify it in the CM data. However the 5 least significant bits must be programmed (**see tables 15 and 16**).

The speech memory address is composed of 4 bits (D0 through D3) for the coding of the 16 input (logical line number and pin names match) lines and 5 bits (D4 through D8) for the coding of 32 time-slots. Which of the four blocks of 32 time-slots each is switched to the output lines is determined by the connection memory address. This consists of 1 bit (IA0) for the marking of one of two possible output lines with 7 bits (IA1 through IA7) for the 128 time-slots, as shown below.

The SP signals controls the start of the input and output frame. The output frame starts two t_{CP8} before the falling SP edge. However, the rising edge marks the beginning of time-slot 125.

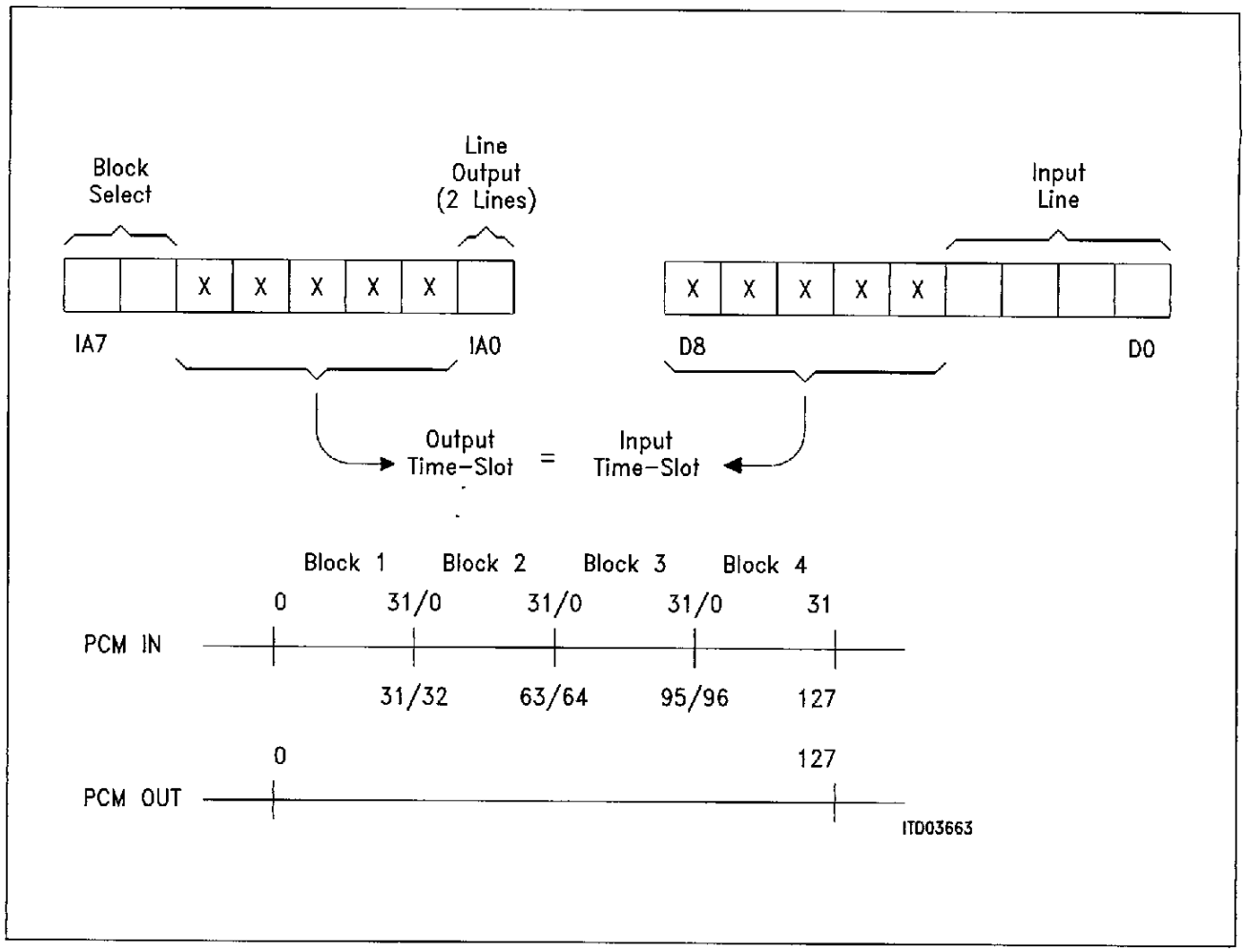


Figure 17
Determination of Input- and Output Time-Slots in Space Switch Mode

The following two examples show how the connection memory is programmed in the space switch mode.

Input line 10, time-slot 31 → output line, time-slot 31

00010011

11111010

00111111

Input line 10, time-slot 63 → output line 1, time-slot 63

00010011

11111010

01111111

3 Operational Description

3.1 Power Up

Upon power up the PEx 2045 is set to its initial state. The mode and configuration register bits are all set to logical 1, the clock shift register bits to logical 0. The status register B bit is undefined, the Z bit contains logical 0, the R bit is undefined.

This state is also reached by pulling the $\overline{WR}$ and $\overline{RD}$ signals to logical 0 at the same time (software reset). For the software reset the state of $\overline{CS}$ is of no significance.

3.2 Initialization Procedure

After power up a few internal signals and clocks need to be initialized. This is done with the initialization sequence. To give all signals and clocks a defined value the MTSC must encounter 3 falling and 2 rising edges of the SP signal. The resulting SP pulses may be of any length allowed in normal operation, the time interval between the two SP pulses may be of any length down to 250 ns.

With all signals being defined, the CM needs to be reset. To do that a logical 0 is written into MOD:RC. STA:B is set. The resulting CM reset is finished after at most 250 µs and is indicated by the status register B bit being logical 0. Changing the pulse shaping factor N during CM reset may result in a CM-reset time longer than 250 µs.

To prepare the PEx 2045 for programming the CM, the RI bit in the mode register must be reset. Note that one mode register access can serve to reset both RC and RI bits as well as configuring to chip (i.e. selecting operating mode etc.).

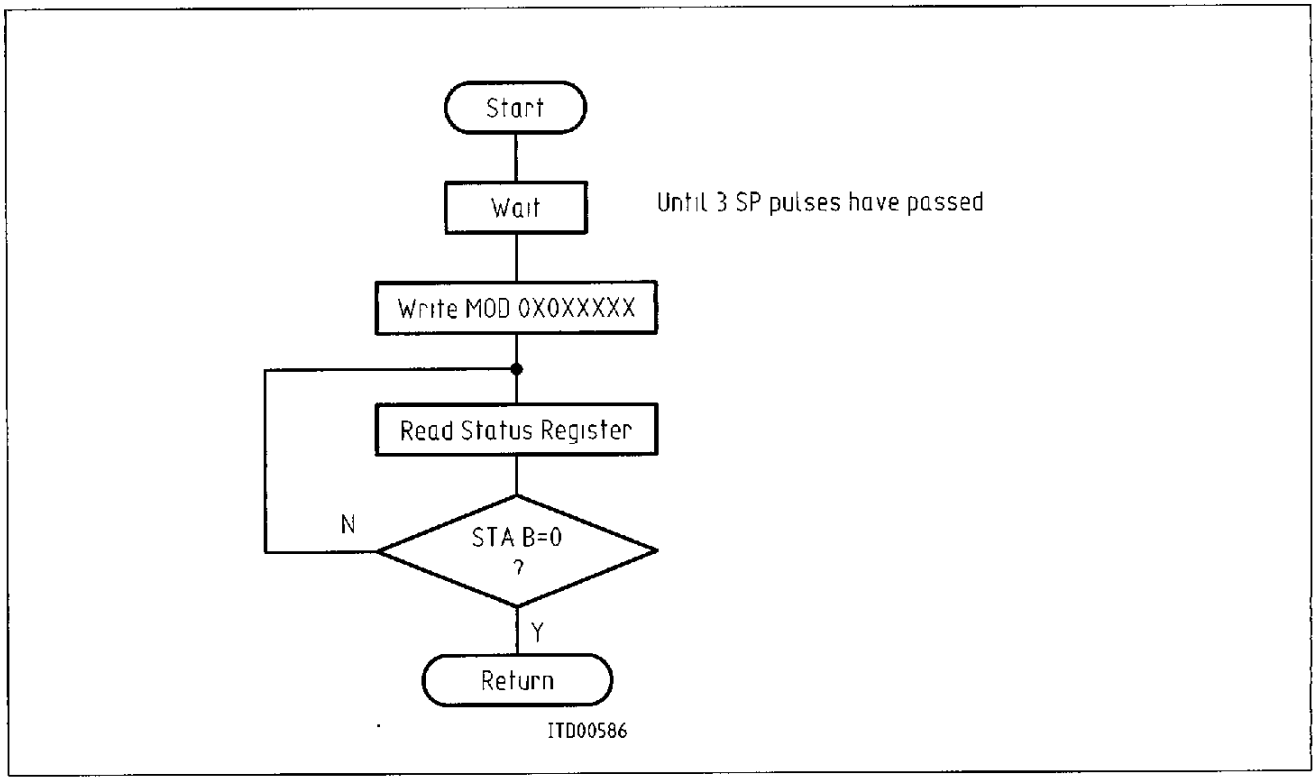


Figure 18
Initializing the PEx 2045 for a 8192-kHz Device Clock

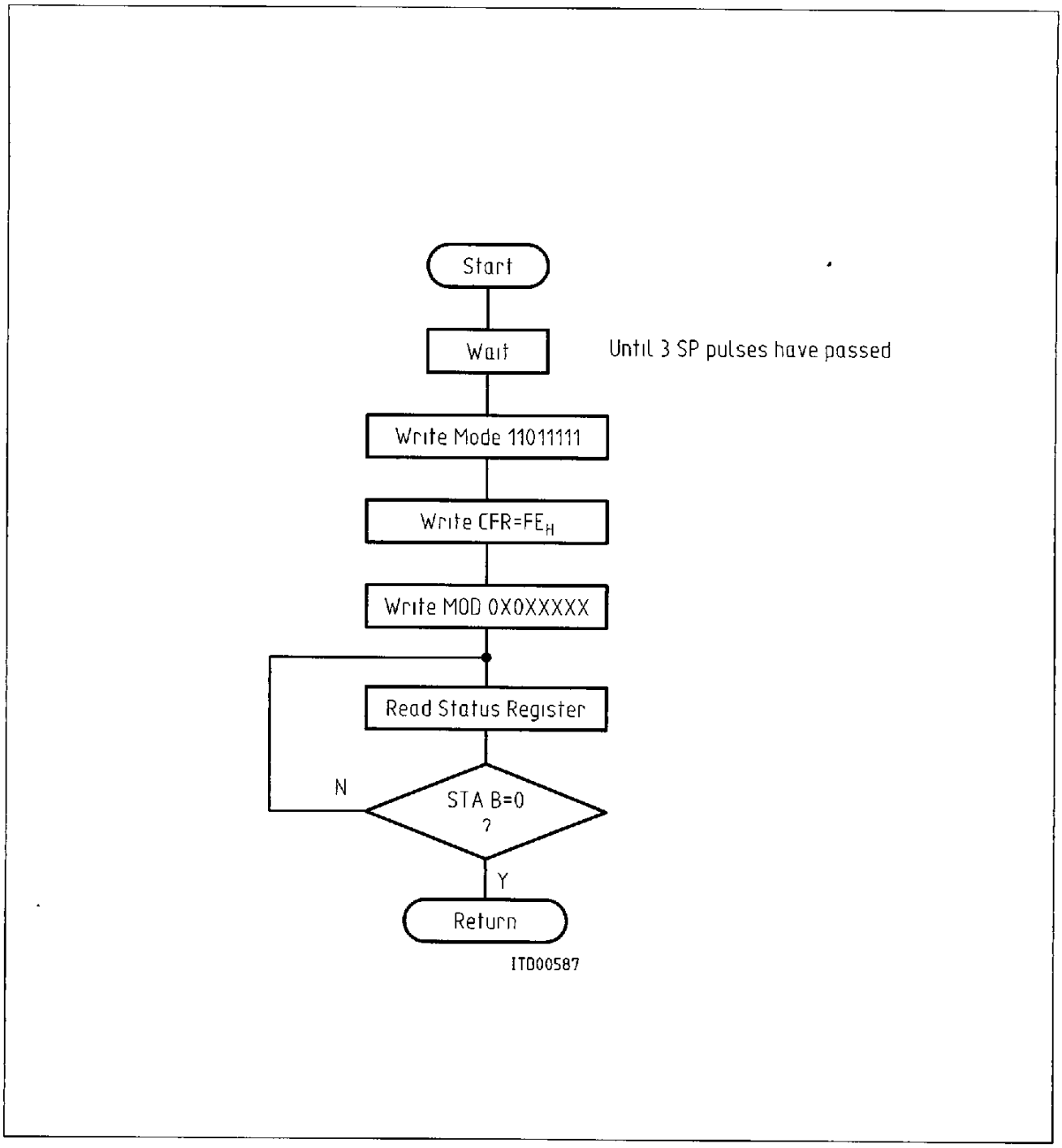


Figure 19
Initializing the PEx 2045 for a 4096-kHz Device Clock

3.3 Operation with a 4096-kHz Device Clock

In order for the MTSC to operate with a 4096-kHz device clock the CPS bit in the CFR register needs to be reset. This has to be done before the CM reset and needs up to 1.8 µs. Please keep in mind, MOD:RI has to be reset prior to performing an indirect register access. For a flow chart of this process refer to **figure 19**.

3.4 Standby Mode

With MOD:SB being logical 1 the PEx 2045 works as a backup device in redundant systems. It can be accessed via the µP interface and works internally like an active device. However, the outputs are high impedance. If the SB bit is reset the outputs are switched to low impedance for the programmed active channels and this MTSC can take over from another device which has been recognized as being faulty. (**See figure 20**)

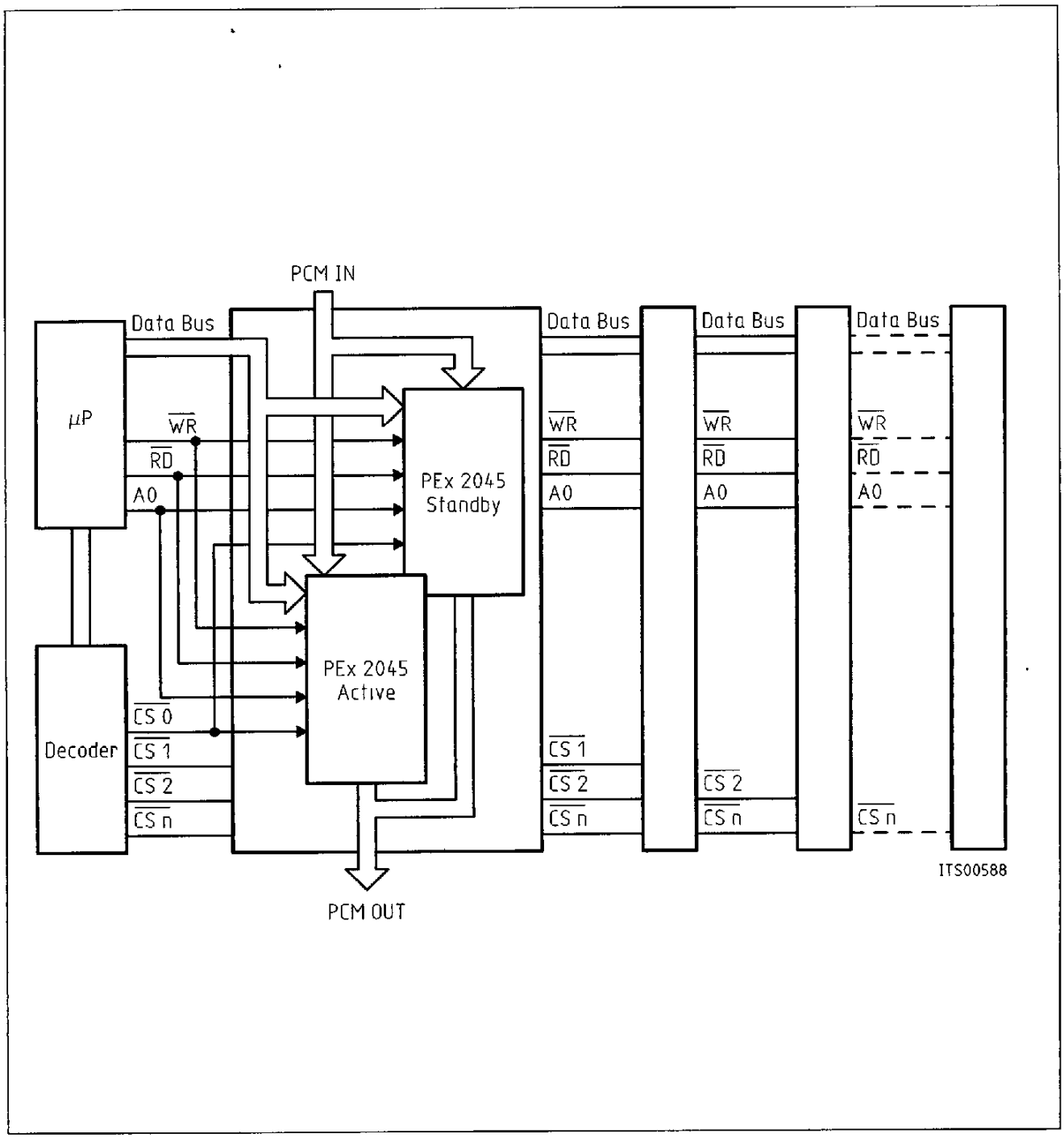


Figure 20
Device Setup in Redundant Systems

4 Detailed Register Description

The following registers may be accessed:

Table 8
Addressing the Direct Registers

Address A0	Write Operation	Read Operation
0	MOD	STA
1	IAR	IAR

The chapters in this section cover the registers in detail.

4.1 Mode Register (MOD)

Access: Write on address 0

DB 7							DB 0
RC	**TE**	**RI**	**SB**	**MI1**	**MI0**	**MO1**	**MO0**

Value after power up: FF_H

RC **Reset Connection** memory; writing a zero to this bit causes the complete connection memory to be overwritten with 200_H (tristate). During this time STA:B is set. The maximum time for resetting the connection memory is 250 µs.

TE **Tristate Enable**; this bit determines which tristating scheme is activated:

TE = 1: If the speech memory address written into the connection memory is S8 – S0 = 0, the output channel is tristated.

TE = 0: The S9 bit written into the connection memory is interpreted as a validity bit: S9 = 0 enables the programmed connection, S9 = 1 tristates the output.

Note: If TE = 1, time-slot 0 of the logical input line 0 cannot be used for switching.

RI **Reset Indirect** access mechanism; setting this bit resets the indirect access mechanism. RI has to be cleared before writing/reading IAR after reset.

SB **Stand By**; by selecting SB = 1 all outputs are tristated. The connection memory works normally. The PEx 2045 can be activated immediately by resetting SB.

MI1/0
MO1/0 **Input/Output** operation **Mode**; these bits define MO1/0: the bit rate of the input and output lines. The bit rates are given in **table 9**, the corresponding pin functions in **table 10** (standard configuration) and **table 11** (primary multiplex access configuration).

Table 9
Input/Output Operating Modes

MI1	MI0	MO1	MO0	Input Mode		Output Mode	
0	0	0	0	16 × 2	Mbit/s	8 × 2	Mbit/s**
0	0	0	1	16 × 2	Mbit/s	2 × 8	Mbit/s
0	0	1	0	16 × 2	Mbit/s	4 × 2 / 1 × 8	Mbit/s
0	1	0	0	4 × 8	Mbit/s	8 × 2	Mbit/s
0	1	0	1	4 × 8	Mbit/s	2 × 8	Mbit/s
0	1	1	0	4 × 8	Mbit/s	4 × 2 / 1 × 8	Mbit/s
1	0	0	0	2 × 8 / 8 × 2	Mbit/s	8 × 2	Mbit/s
1	0	0	1	2 × 8 / 8 × 2	Mbit/s	2 × 8	Mbit/s
1	0	1	0	2 × 8 / 8 × 2	Mbit/s	4 × 2 / 1 × 8	Mbit/s**
0	0	1	1	8 × 4	Mbit/s	4 × 4	Mbit/s
0	1	1	1	4 × 8	Mbit/s	4 × 4	Mbit/s
1	1	1	1	4 × 4 / 8 × 2	Mbit/s	4 × 2 / 2 × 4	Mbit/s**
1	0	1	1	8 × 4	Mbit/s	2 × 8	Mbit/s
1	1	0	1	16 × 8	Mbit/s	2 × 8	Mbit/s*
1	1	0	0	unused			
1	1	1	0	unused			

* for space switch application only
** can also be used for primary access configuration

Note: In the mixed modes the first bit rate refers to the odd line numbers, the second one to the even line numbers.

Table 10
Input and Output Pin Arrangement for the Standard Configuration

Input Pin Arrangement

Pin No.		16 × 8 Mbit/s 16 × 2 Mbit/s	4 × 8 Mbit/s	8 × 2 + 2 × 8 Mbit/s	8 × 4 Mbit/s	8 × 2 + 4 × 4 Mbit/s
P-LCC	P-DIP					
4	3	IN1				
5	4	IN0		IN0		IN0
7	5	IN5				
8	6	IN4		IN4		IN4
9	7	IN9			IN1	IN1
10	8	IN8		IN8	IN0	IN8
11	9	IN13	IN1	IN1	IN5	IN5
12	10	IN12	IN0	IN12	IN4	IN12
13	11	IN14	IN2	IN14	IN6	IN14
14	12	IN15	IN3	IN3	IN7	IN7
15	13	IN10		IN10	IN2	IN10
16	14	IN11			IN3	IN3
17	15	IN6		IN6		IN6
18	16	IN7				
19	17	IN2		IN2		IN2
20	18	IN3				

Note: The input line numbers shown are the logical line numbers to be used for programming the connection memory. In the case of 16 input lines the logical line numbers are identical to the pin names.

Output Pin Arrangement

Pin No.		8 × 2 Mbit/s	2 × 8 Mbit/s	4 × 2 + 1 × 8 Mbit/s	4 × 4 Mbit/s	4 × 2 + 2 × 4 Mbit/s
P-LCC	P-DIP					
35	32	OUT7		OUT7		OUT7
36	33	OUT6				
37	34	OUT5		OUT5		OUT5
38	35	OUT4				
40	36	OUT3		OUT3	OUT3	OUT3
41	37	OUT2			OUT2	OUT2
42	38	OUT1	OUT1	OUT1	OUT1	OUT1
43	39	OUT0	OUT0	OUT0	OUT0	OUT0

Note: The logical output line numbers shown above are identical to the pin names.

Table 11
Input, Output and Tristate Pin Arrangement for the Primary Access Configuration

	Pin No.		System Interface Mode			
Pin Name	**P-LCC**	**P-DIP**	**2 MHz**	**4 MHz**	**8 MHz**	
TSC0 TSC1 TSC2 TSC3	5 8 10 12	4 6 8 10	TSC0 TSC1 TSC2 TSC3	TSC0 TSC1	TSC0	System interface tristate control signals, clock shift programmable
OUT0 OUT2 OUT4 OUT6	43 41 38 36	39 37 35 33	OUT0 OUT1 OUT2 OUT3	OUT0 OUT1	OUT0	System interface outputs clock shift programmable
IN13 IN9 IN5 IN1	11 9 7 4	9 7 5 3	IN3 IN2 IN1 IN0	IN1 IN0	IN0	System interface inputs, clock shift programmable
OUT1 OUT3 OUT5 OUT7	42 40 37 35	38 36 34 32	OUT0 OUT1 OUT2 OUT3	OUT0 OUT1 OUT2 OUT3	OUT0 OUT1 OUT2 OUT3	Synchronous 2-MHz interface outputs
IN14 IN10 IN6 IN2	13 15 17 19	11 13 15 17	IN3 IN2 IN1 IN0	IN3 IN2 IN1 IN0	IN3 IN2 IN1 IN0	Synchronous 2-MHz interface inputs
Mode			0000	1111	1010	MI1, MI0, MO1, MO0

Note: The input, output and tristate control line numbers shown in the center columns of this table are logical line numbers. The corresponding pin names are listed in the left most column.

4.2 Status Register (STA)

Access: Read at address 0

DB 7							DB 0
B	**Z**	**R**	**0**	**0**	**0**	**0**	**0**

B **Busy:** The chip is busy resetting the connection memory (B = 1). B is undefined after power up and logical 0 after the device initialization.

Note: The maximum time for resetting the connection memory is 250 µs.

Z Incomplete instruction; a three byte indirect instruction is not completed (Z = 1). Z is 0 after power up.

Note: Z is reset and the indirect access is cancelled by setting MOD:RI or resetting MOD:RC.

R Initialization **Request**. The connection memory has to be reset due to loss of data (R = 1). The R bit is set after power failure or inappropriate clocking and reset when the connection memory reset is finished. R is undefined after power up and logical 0 after the device initialization.

4.3 Indirect Access Register (IAR)

(Read or Write Operation with Address A0 = 1)

An indirect access is performed by reading/writing three consecutive bytes (first byte = control byte, second byte = data byte, third byte = address byte) to/from IAR. The structure is shown in **table 12**.

Table 12
The 3 Bytes of the Indirect Access

Bit 7							**Bit 0**	
0	0	K1	K0	0	0	C1	C0	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The control byte bits K1, K0, C1 and C0 together with the address byte determine the type of access being performed according to **table 13**.

Table 13
Encoding the Different Types of Indirect Accesses

K1	K0	C1	C0	Address Byte	Type of Access
0	0	D9	D8	CM Address	Read CM
1	0	D9	D8	CM Address	Write CM
0	1	D9	D8	CM Address	Write CM
1	1	0	0	FE_H	Write CFR
1	1	0	1	FE_H	Read CFR
1	1	0	0	FE_H	Write CSR
1	1	0	1	FE_H	Read CSR

Connection Memory Access

For a connection memory access the control byte bits C1 and C0 contain the data bits D9 and D8, respectively. D9 is the validity bit which together with D8 and the data byte D7 – D0 is written to the CM address IA7 – IA0.

The function of the validity bit is controlled by STA:TE. D8 – D0 and IA7 – IA0 contain the information for the logical line and time-slot numbers of the programmed connection, D8 – D0 for the inputs, IA7 – IA0 for the outputs. **Tables 14** through **18** show the programming of these bits for the different configurations and modes.

Standard Configuration

Table 14
Time-Slot and Line Programming for Standard Configuration

Standard configuration, all modes except space switch mode					
2-Mbit/s input lines	Bit	D3	to	D0	Logical line number
	Bit	D8	to	D4	Time-slot number
	Bit	D9			Validity bit
4-Mbit/s input lines	Bit	D2	to	D0	Logical line number
	Bit	D8	to	D3	Time-slot number
	Bit	D9			Validity bit
8-Mbit/s input lines	Bit	D1	to	D0	Logical line number
	Bit	D8	to	D2	Time-slot number
	Bit	D9			Validity bit
2-Mbit/s output lines	Bit	IA2	to	IA0	Line number
	Bit	IA7	to	IA0	Time-slot number
4-Mbit/s output lines	Bit	IA1	to	IA0	Line number
	Bit	IA7	to	IA2	Time-slot number
8-Mbit/s output lines	Bit	IA0			Line number
	Bit	IA7	to	IA1	Time-slot number

The pulse shape factor N may take any integer value from 0 to 255.

Space Switch Mode

Table 15
Time-Slot and Line Programming for Space Switch Mode

Space switch mode	(MI1 = 1, MI0 = 1; MO1 = 0, MO0 = 1)				
8-Mbit/s input lines	Bit	D0	to	D3	Logical line number
	Bit	D4	to	D8	The lower 5 bits of the time-slot number
	Bit	D9			Validity bit
8-Mbit/s output lines	Bit	IA0			Logical line number
	Bit	IA1	to	IA7	Time-slot number

N is fixed to 70. The selection of one specific input time-slot is possible by writing the connection memory (CM) as shown below.

Table 16
Programming Input and Output Lines and Time-Slots in Space Switch Mode

In CM address 00 – 3F:	D8 – D4 (SM addr.)	=	TS0 – TS3
In CM address 40 – 7F:	D8 – D4 (SM addr.)	=	TS32 – TS63
In CM address 80 – BF:	D8 – D4 (SM addr.)	=	TS6 – TS95
In CM address C0 – FF:	D8 – D4 (SM addr.)	=	TS96 – TS127

In space switch mode the leading edge of the SP pulse must be applied with the first bit of time-slot 125. The input and output time-slot number must match.

Primary Access Configuration

Table 17
Time-Slot and Line Programming for the Primary Access Configuration

2-Mbit/s input lines	Bit	D1	to	D0	Interface select in
	Bit	D3	to	D2	Line number
	Bit	D8	to	D4	Time-slot number
	Bit	D9			Validity bit
4-Mbit/s input lines	Bit	D1	to	D0	Fixed to 01 (system interface)
	Bit	D2			Line number
	Bit	D8	to	D3	Time-slot number
	Bit	D9			Validity bit
8-Mbit/s input lines	Bit	D1	to	D0	Fixed to 01 (system interface)
	Bit	D8	to	D2	Line number
	Bit	D9			Validity bit
2-Mbit/s output lines	Bit	IA0			Interface select out
	Bit	IA2	to	IA1	Line number
	Bit	IA7	to	IA3	Time-slot number
4-Mbit/s output lines	Bit	IA0			Fixed to 0 (system interface)
	Bit	IA1			Line number
	Bit	IA7	to	IA2	Time-slot number
8-Mbit/s output lines	Bit	IA0			Fixed to 0 (system interface)
	Bit	IA7	to	IA1	Time-slot number

The interface select bits have to be programmed as shown in the following table:

Table 18
Interface Selection Bits

	System Interface	Synchronous 2-MHz Interface
Input Lines	01	10
Output Lines	0	1

Configuration Register Access (CFR)

Access: Read or write indirect address FE_H

For a read access the bit 0 of the control byte must be set to logical 1 and for a write access to logical 0.

Value after power up or software reset: FF_H

DB 7							DB 0
1	1	1	1	1	1	CFS	CPS

CPS ... **Clock Period Select:** Device clock is set to 8192 kHz (logical 1) or 4096 kHz (logical 0).

CFS ... **Configuration Select:** The PEx 2045 works in either the primary access configuration (logical 0) or in standard configuration (logical 1). Setting this bit to logical 1 resets the CSR to 00_H.

Clock Shift Register Access (CSR)

Access: Read or write at indirect address FF_H.

For a read access the bit 0 of the control byte has to be set to logical 1 and for a write access to logical 0.

The value after power is 00_H.

DB 7							DB 0
RS2	RS1	RS0	RRE	XS2	XS1	XS0	XFE

RS2 ... RS0 ... **Receive** clock **Shift**, bits 2 – 0. The receive data stream is shifted in bit period steps as shown in **figure 21.**

RRE ... **Receive** with **Rising Edge**. The data is sampled with the falling (RRE = 0) or rising edge (RRE = 1) of the data equivalent clock (**see figure 21**).

XS0 ... XS2 ... **Transmit** clock **Shift**, bits 2 – 0. The transmitted data stream is shifted as shown in **figure 21**.

XFE ... **Transmit** with **Falling Edge**; data is transmitted with the rising (XFE = 0) or falling edge (XFE = 1) of the device clock.

Data stream manipulation according to these register entries only affects the system interface and only in the primary access configuration. The frame structure can be moved relative to the SP slope by up to 7 clock periods in half clock period steps. This register can hold non-zero values only for a CFR:CFS value of logical 0. **Figure 21** illustrates the clock shifting facility.

Identical non-zero entries for RS2 – RS0 and XS2 – XS0 as well as identical RRE and XFE generate an output time-slot structure which is 1 time-slot late relative to the input time-slot structure.

Identical 000 entries for RS2 – R0 and XS2 – XS0 as well as RRE and XFE being logical 0 cause the input and output frames to coincide in time.

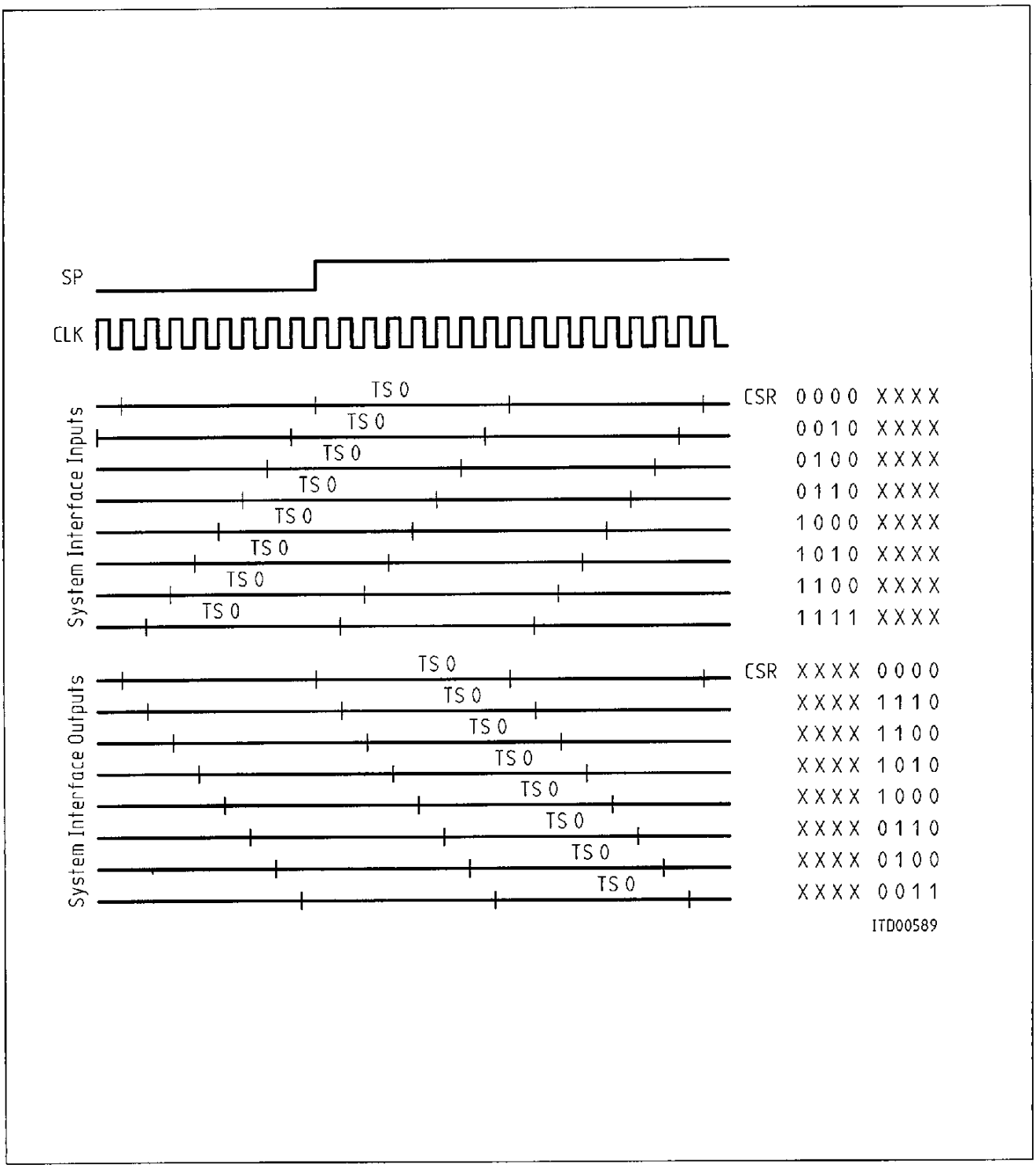


Figure 21
Clock Shifting

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEB 2045	T_A	0 to 70	°C
Storage temperature PEB 2045	T_{stg}	– 65 to 125	°C
Ambient temperature under bias PEF 2045	T_A	– 40 to 85	°C
Storage temperature PEF 2045	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V

DC Characteristics

Ambient temperature under bias range; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V.

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-input voltage	V_{IL}	– 0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} + 0.4	V	
L-output voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V V	I_{OH} = – 400 µA I_{OH} = – 100 µA
Operational power supply current	I_{CC}		10	mA	V_{DD} = 5 V, inputs at 0 V or V_{DD}, no output loads
Input leakage current Output leakage current	I_{LI} I_{LO}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

T_A = 25 °C, V_{DD} = 5 V ± 5 %, V_{SS} = 0 V.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
I/O capacitance	C_{IO}		20	pF
Output capacitance	C_{OUT}		15	pF

AC Characteristics

Ambient temperature under bias range, $V_{DD} = 5\ V \pm 5\ \%$.

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

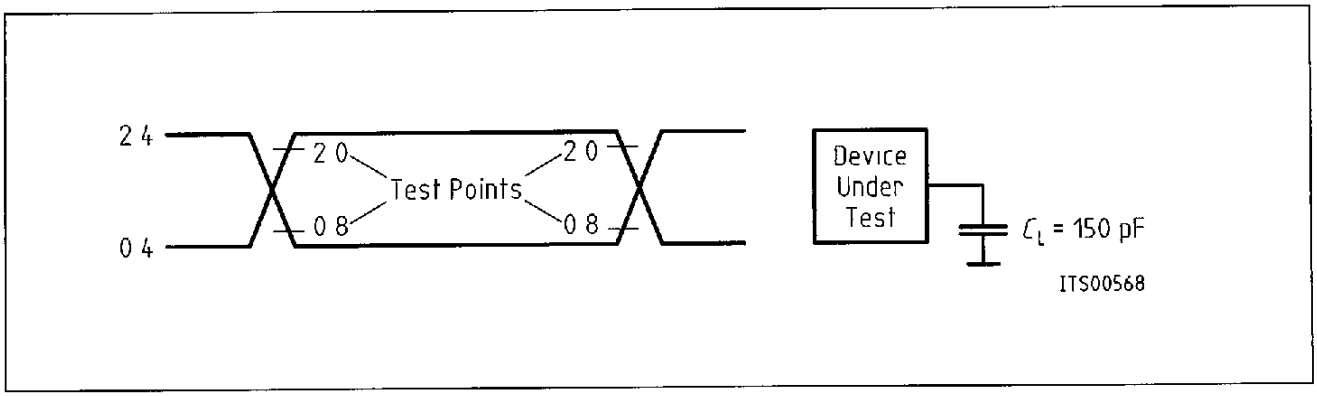


Figure 22
I/O Waveform for AC Tests

µP-Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address stable before $\overline{RD}$	t_{AR}	0		ns
Address hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ width	t_{RR}	90		ns
$\overline{RD}$ to data valid	t_{RD}		90	ns
Address stable to data valid	t_{AD}		90	ns
Data float after $\overline{RD}$	t_{DF}	5	25	ns
Read cycle time	t_{RCY}	160		ns
Address stable before $\overline{WR}$	t_{AW}	0		ns
Address hold time	t_{WA}	0		ns
$\overline{WR}$ width	t_{WW}	60		ns
Data setup time	t_{DW}	5		ns
Data hold time	t_{WD}	15		ns
Write cycle time	t_{WCY}	160		ns

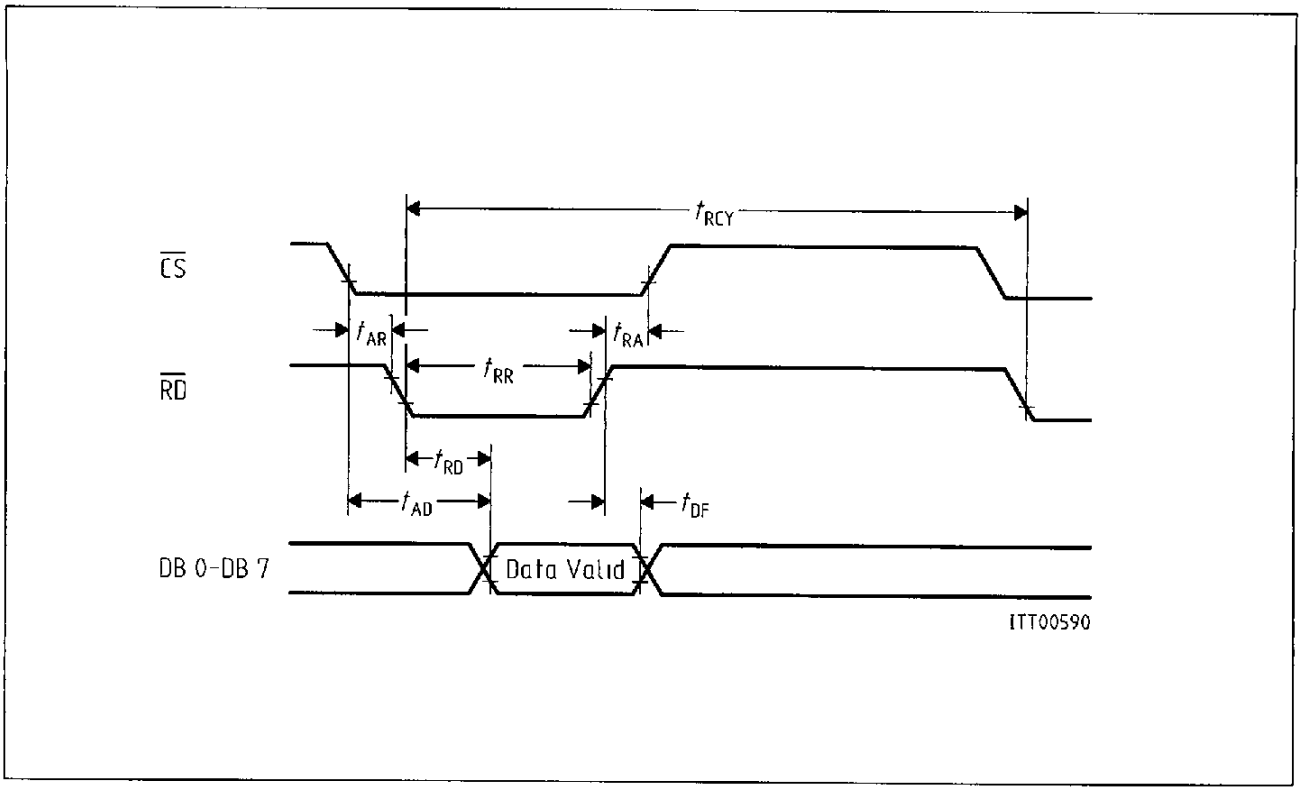


Figure 23
µP-Read Cycle

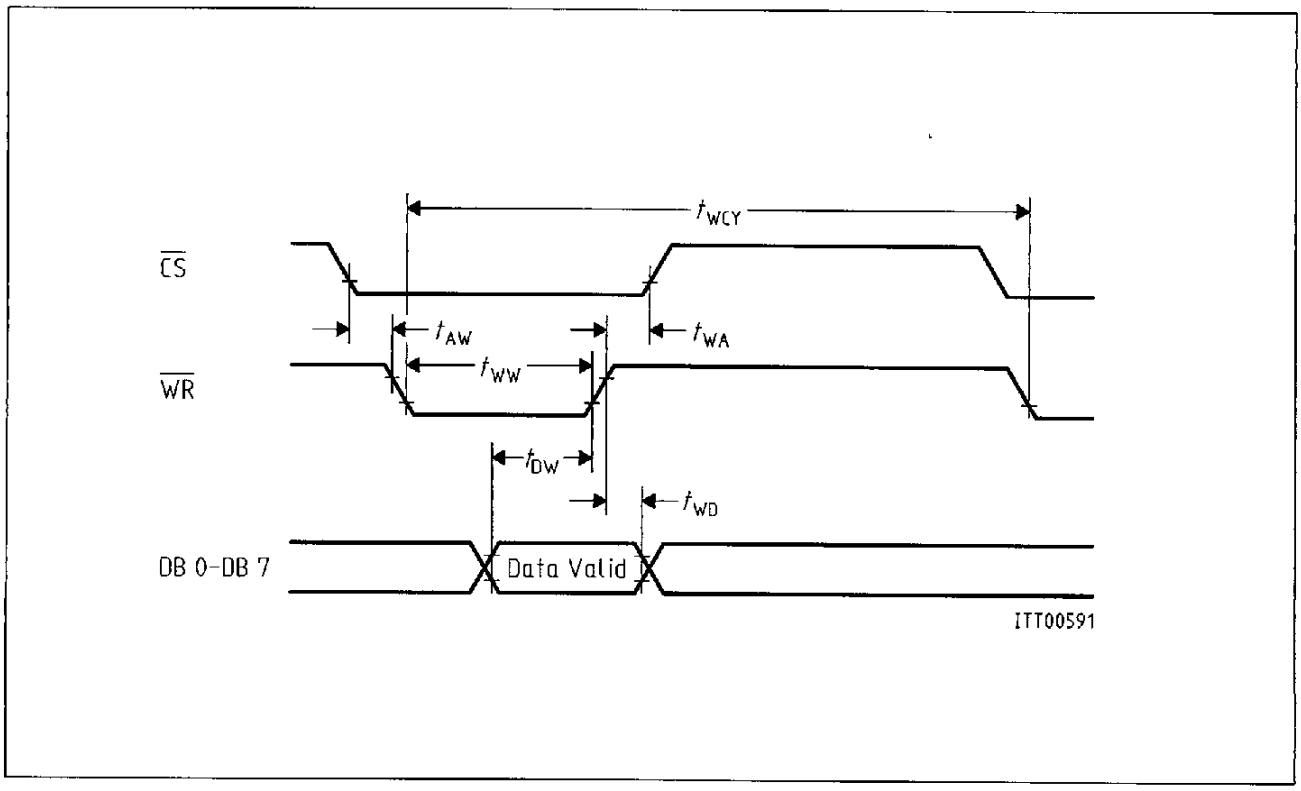


Figure 24
µP-Write Cycle

PCM-Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCM-input setup	t_S	0		ns
PCM-input hold	t_H	30		ns
PEB 2045 output delay	t_D		45	ns
PEF 2045 output delay	t_D		50	ns
PEB 2045 tristate delay	t_T		55	ns
PEF 2045 tristate delay	t_T		60	ns

Clock and Synchronization Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock period 8 MHz high	$t_{CP8\ H}$	40		ns
Clock period 8 MHz low	$t_{CP8\ L}$	48		ns
Clock period 8 MHz	t_{CP8}	120		ns
Synchronization pulse setup 8 MHz	t_{SS8}	10	$t_{CP8} - 20$	ns
Synchronization pulse delay 8 MHz	t_{SH8}	0	$t_{CP8} - 20$	ns
Clock period 4 MHz high	$t_{CP4\ H}$	90		ns
Clock period 4 MHz low	$t_{CP4\ L}$	90		ns
Clock period 4 MHz	t_{CP4}	240		ns
Synchronization pulse setup 4 MHz	t_{SS4}	10	$t_{CP4} - 30$	ns
Synchronization pulse delay 4 MHz	t_{SH4}	30	$t_{CP4} - 10$	ns
Data clock delay	t_{DCD}		100	ns

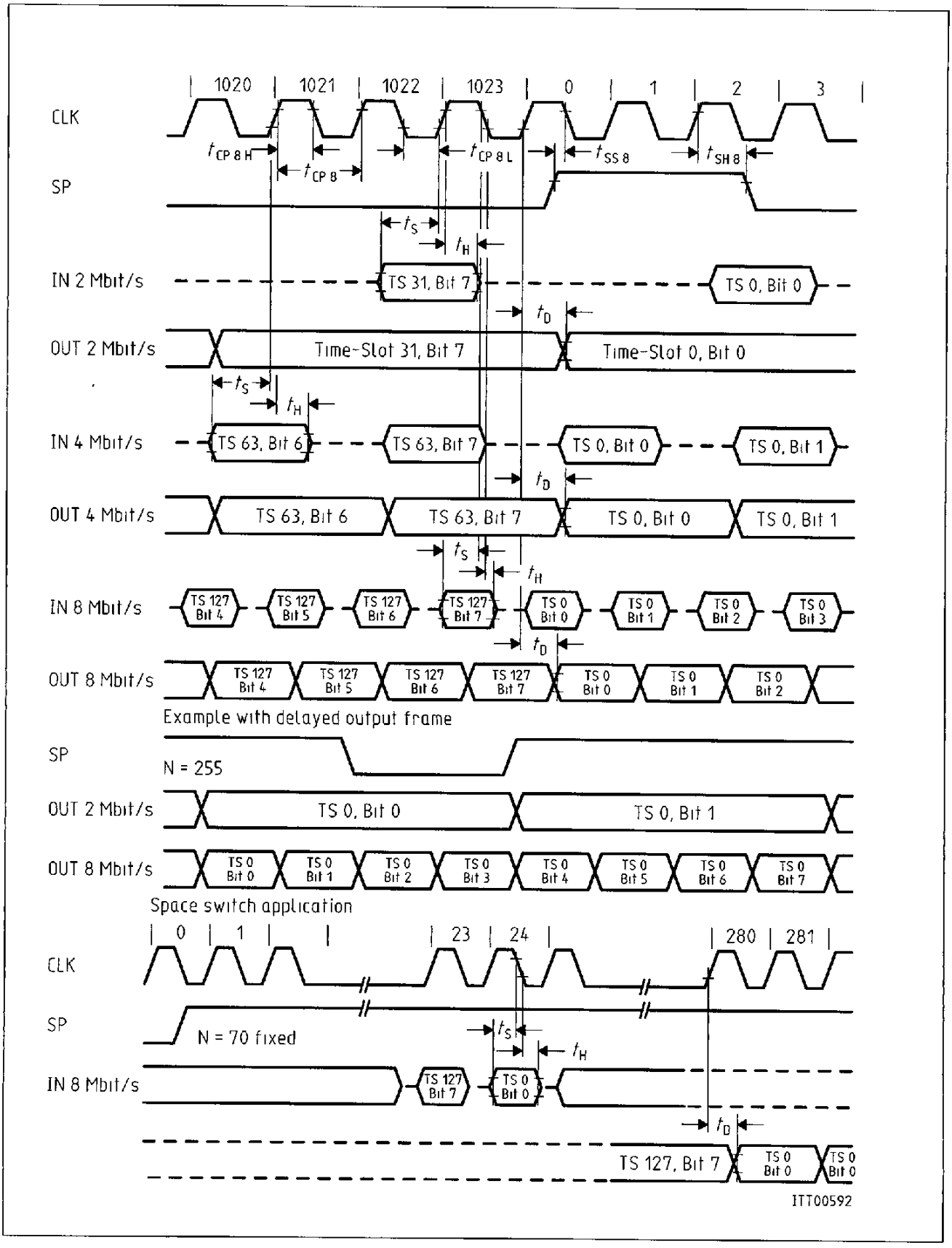


Figure 25
PCM-Line Timing in Standard Configuration with a 8-MHz Device Clock

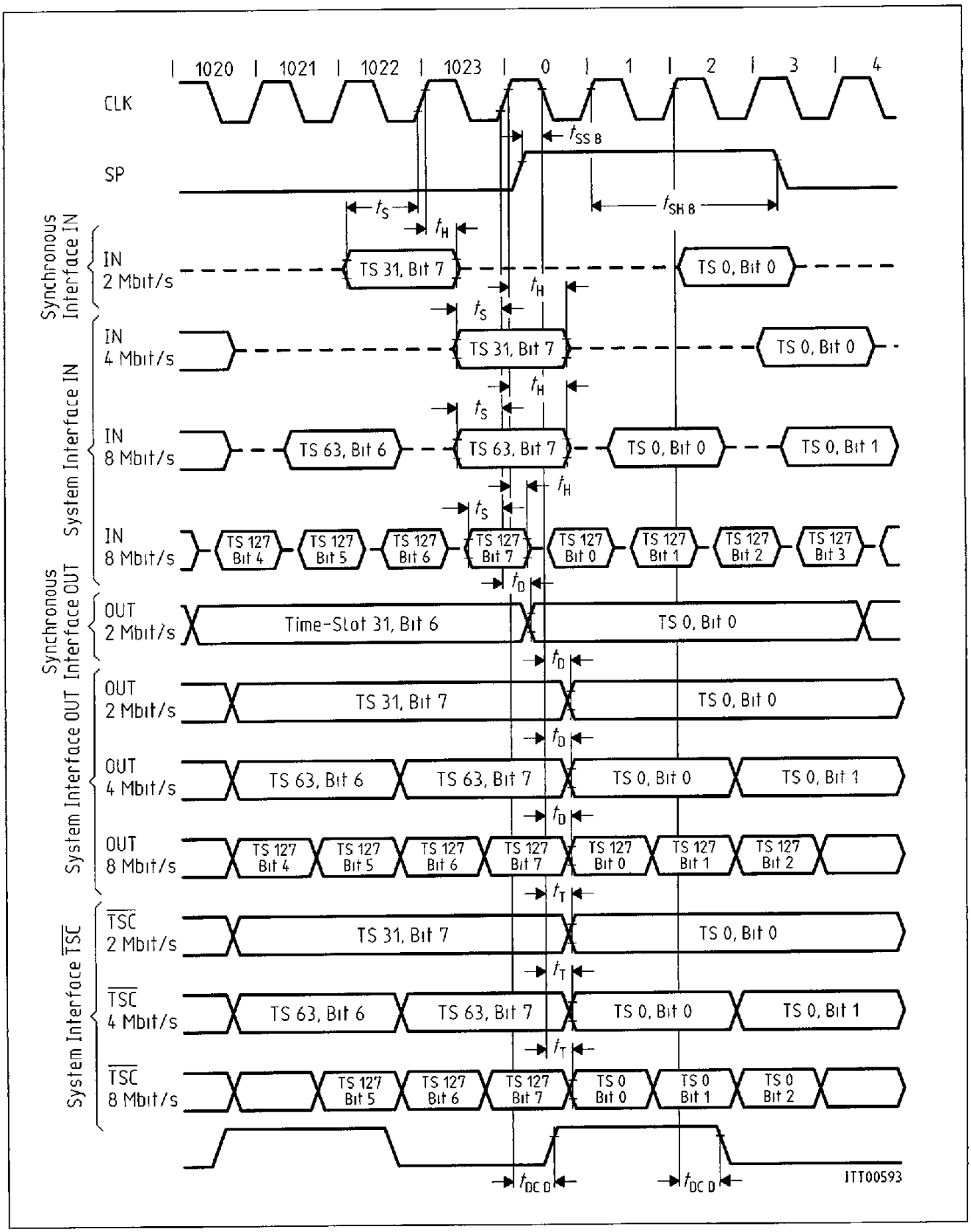


Figure 26
PCM-Line Timing in Primary Access Configuration with a 8 MHz-Device Clock and a CSR Entry (00010001)

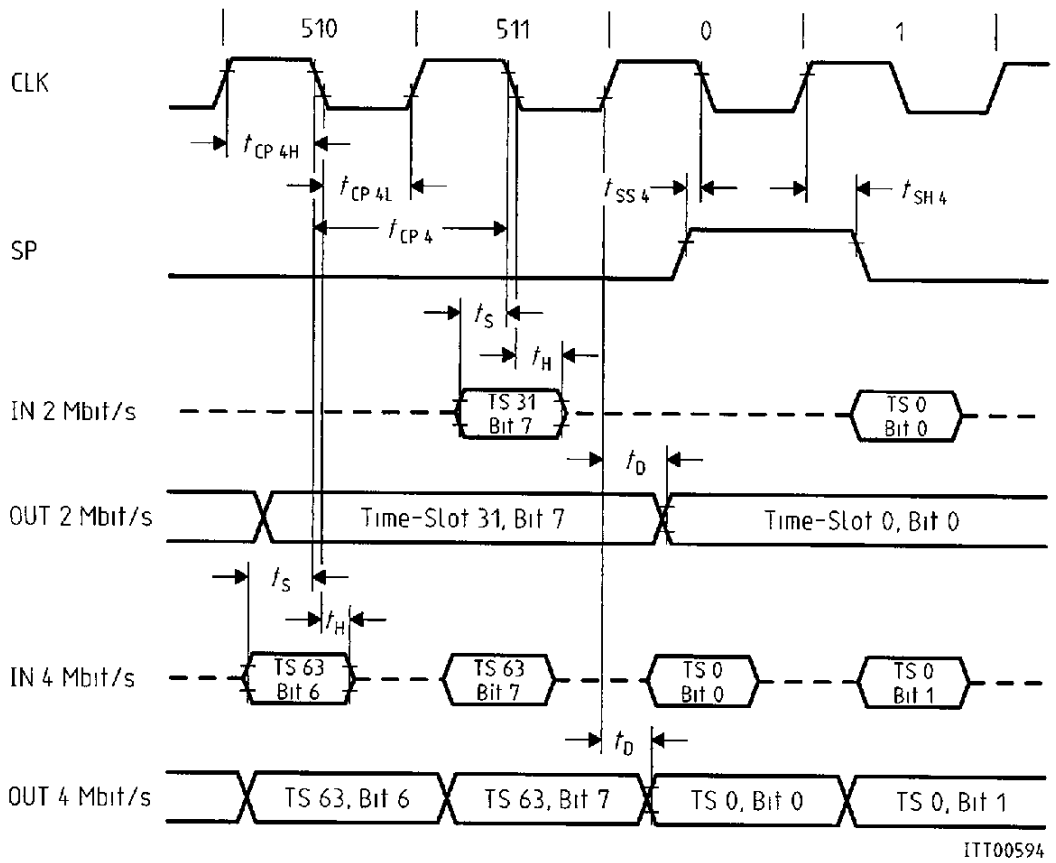


Figure 27
PCM-Line Timing in Standard Configuration with a 4-MHz Device Clock

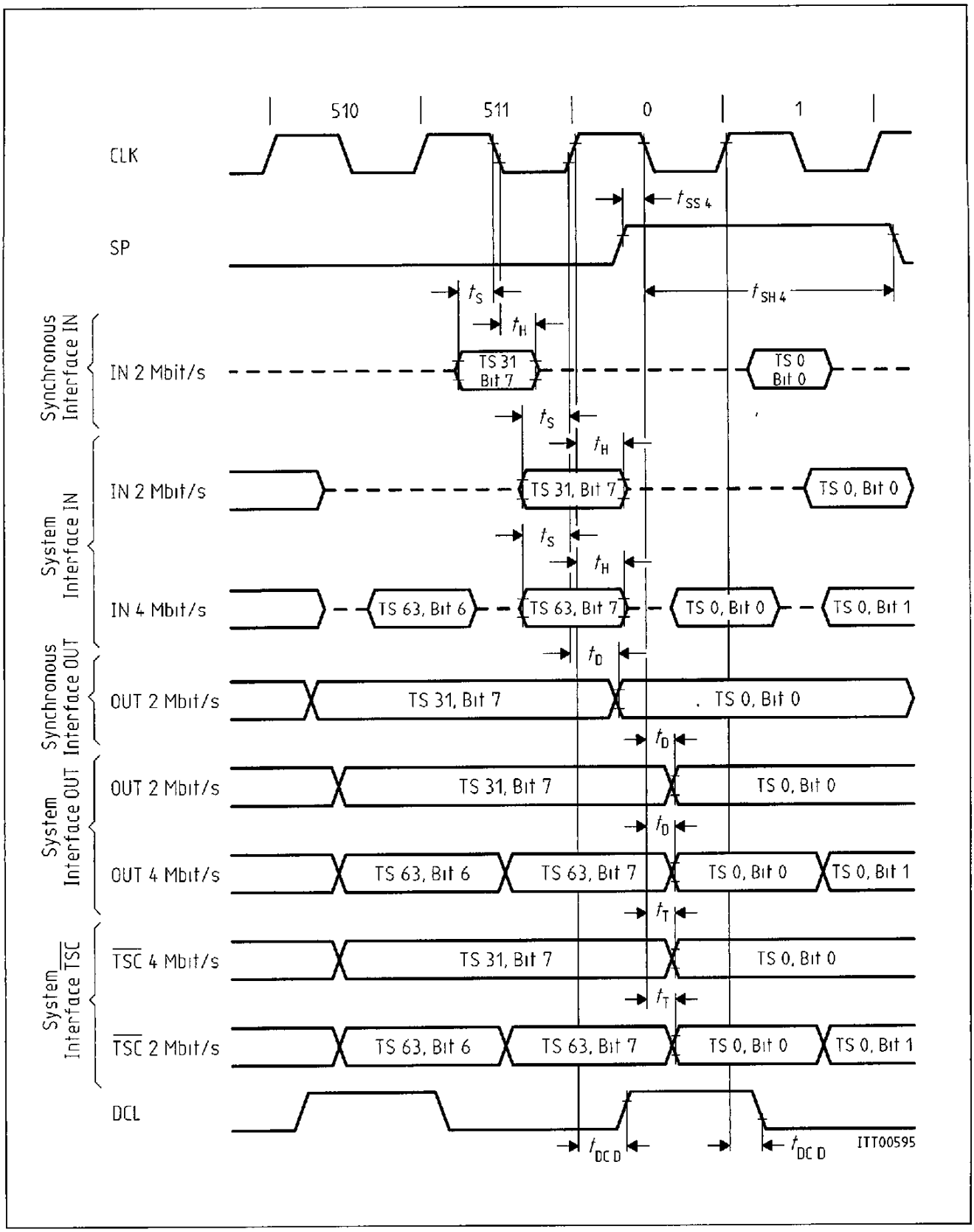


Figure 28
PCM-Line Timing in Primary Access Configuration with a 4-MHz Device Clock and a CSR Entry (00010001)

Busy Times

Operation	Max. Value	Unit
Indirect register access	900	ns
Connection memory reset	250	µs

6 Applications

Calculation of Switching Delay for PEB 2045

8-MHz Clock Cycle (t_{CL} = 122 ns)

Output Line / PCM Mode (Mbit/s)				Even Input Line	Odd Input Line
	2	4	8		
OUT	0			64 t_{CL}	80 t_{CL}
OUT	1			60 t_{CL}	76 t_{CL}
OUT	2			56 t_{CL}	72 t_{CL}
OUT	3			52 t_{CL}	68 t_{CL}
OUT	4	0		48 t_{CL}	64 t_{CL}
OUT	5	1		44 t_{CL}	60 t_{CL}
OUT	6	2	0	40 t_{CL}	56 t_{CL}
OUT	7	3	1	36 t_{CL}	52 t_{CL}
				Δ C min	Δ C min

Formula for determining the frame delay:

$$\text{Fdel} = \frac{\text{C del} - (\text{TS out} - \text{TS in}) \times \text{TS dur} + 1024}{1024}$$

Fdel = Frame delay (e.g. Fdel = 1.5 means 1 frame delay and Fdel = 0.8 means 0 frame delay)

Cdel = Component delay = Δ C min – (Δ SP – 2)

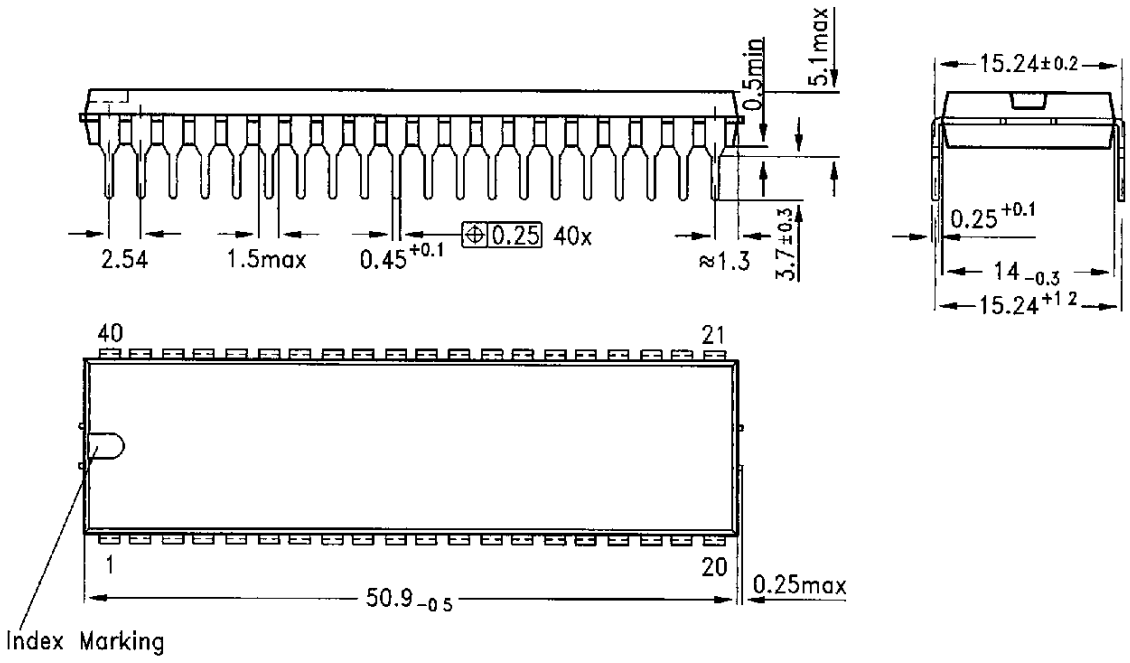
TSout = Time-slot number out clock cycles N = 0

TSin = Time-slot number in N = 2 → Δ SP = 10

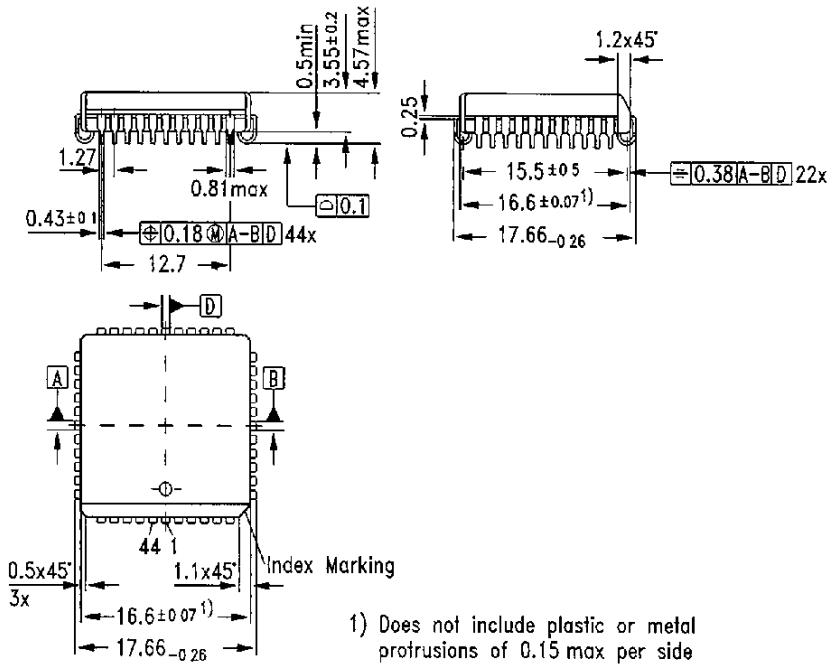
TSdur = Time-slot duration = 32 t_{CL} at 2 Mbit/s
= 16 t_{CL} at 4 Mbit/s
= 8 t_{CL} at 8 Mbit/s

With the above you should be able to calculate the frame delays for all switching possibilities.

Plastic Package, P-DIP-40
(Plastic Dual In-Line Package)



Plastic Package, P-LCC-44 (SMD)
(Plastic Leaded Chip Carrier)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm