

# PAL16L8AM, PAL16L8A-2M, PAL16R4AM, PAL16R4A-2M PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

- **Choice of Operating Speeds**  
High-Speed, A Devices . . . 25 MHz Min  
Half-Power, A-2 Devices . . . 16 MHz Min
- **Choice of Input/Output Configuration**
- **Package Options Include Both Ceramic DIP and Chip Carrier in Addition to Ceramic Flat Package**

| DEVICE  | I<br>INPUTS | 3-STATE<br>O OUTPUTS | REGISTERED<br>Q OUTPUTS | I/O<br>PORT<br>S |
|---------|-------------|----------------------|-------------------------|------------------|
| PAL16L8 | 10          | 2                    | 0                       | 6                |
| PAL16R4 | 8           | 0                    | 4 (3-state buffers)     | 4                |
| PAL16R6 | 8           | 0                    | 6 (3-state buffers)     | 2                |
| PAL16R8 | 8           | 0                    | 8 (3-state buffers)     | 0                |

## description

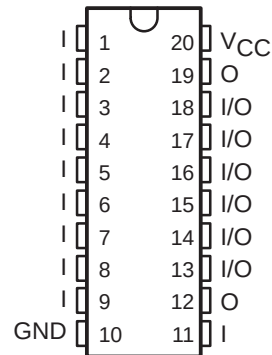
These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allow for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

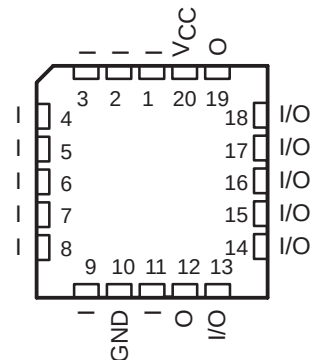
**PAL16L8'  
J OR W PACKAGE**

(TOP VIEW)



**PAL16L8'  
FK PACKAGE**

(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



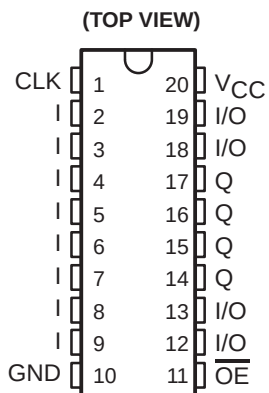
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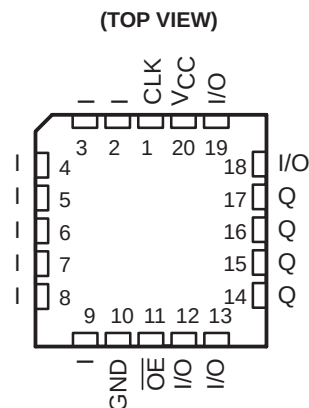
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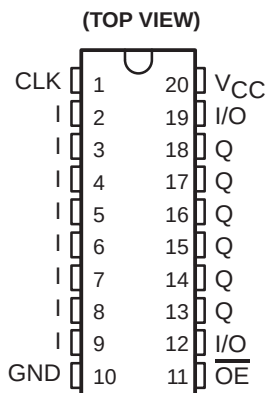
**PAL16R4'**  
J OR W PACKAGE



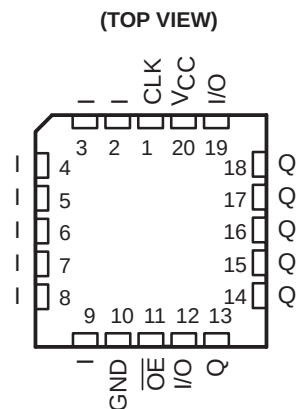
**PAL16R4'**  
FK PACKAGE



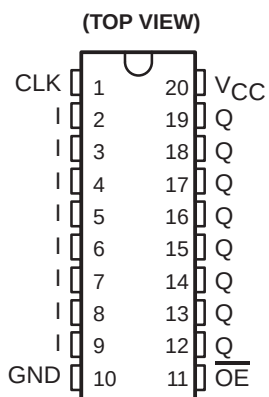
**PAL16R6'**  
J OR W PACKAGE



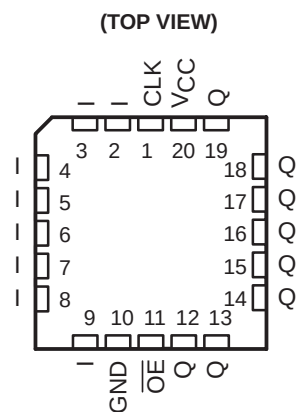
**PAL16R6'**  
FK PACKAGE



**PAL16R8'**  
J OR W PACKAGE



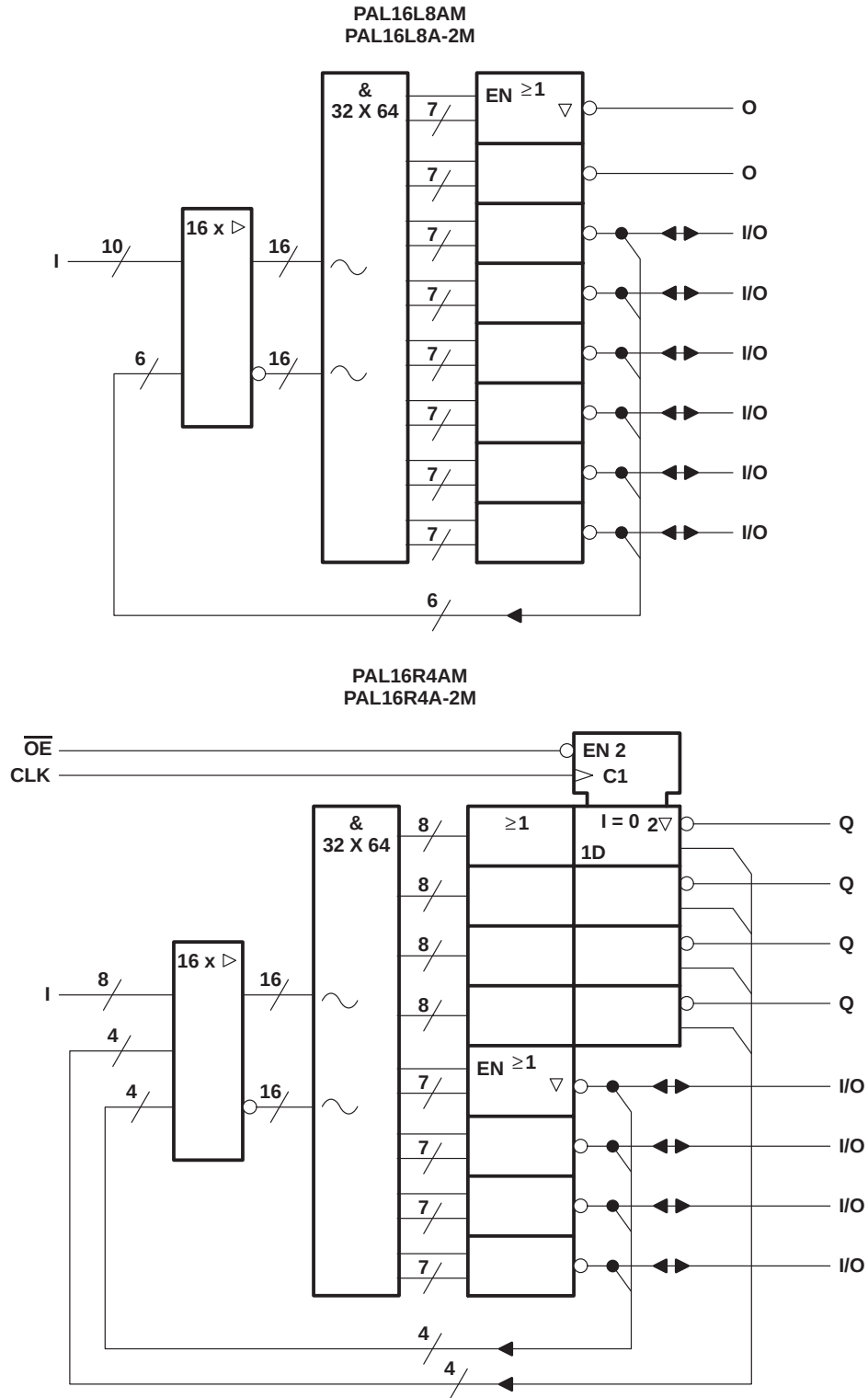
**PAL16R8'**  
FK PACKAGE



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## functional block diagrams (positive logic)

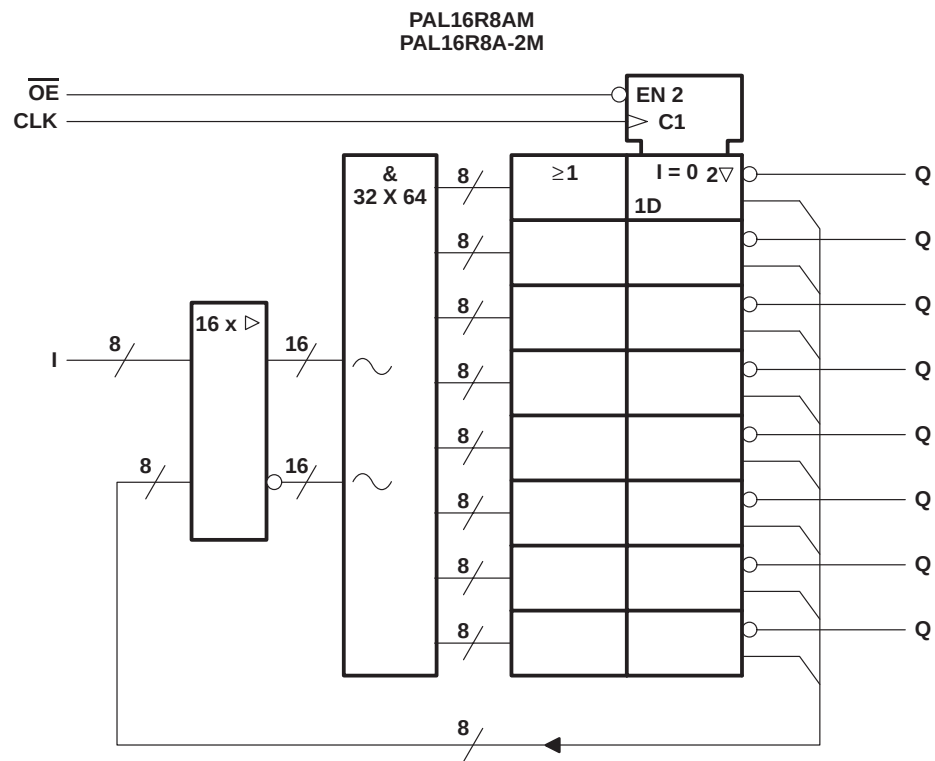
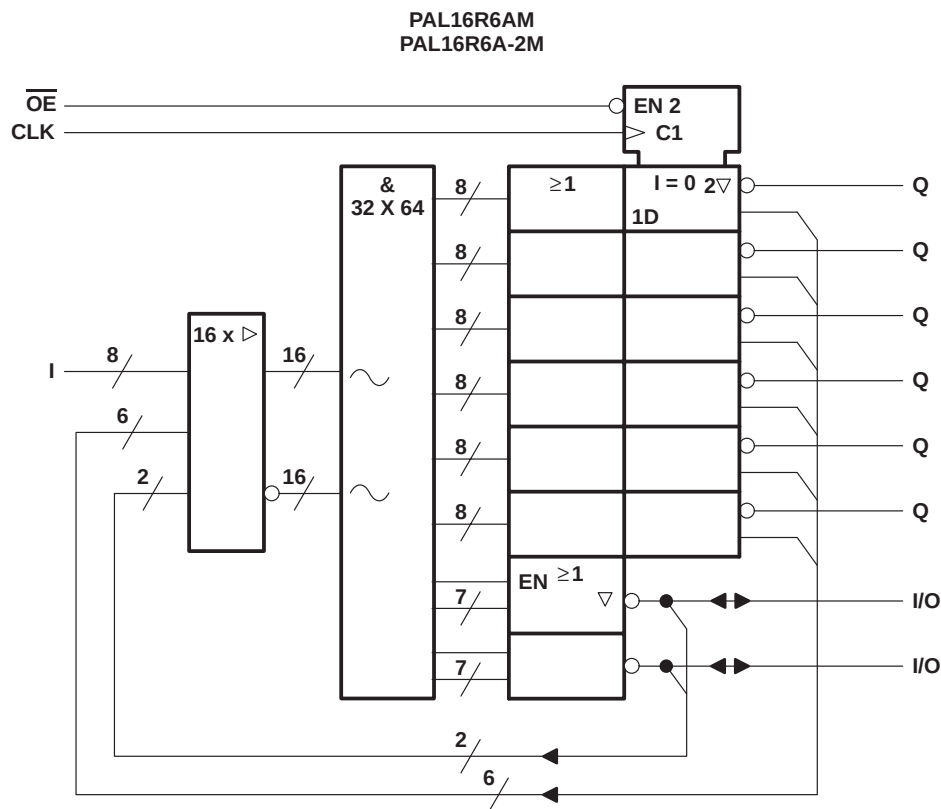


~ denotes fused inputs

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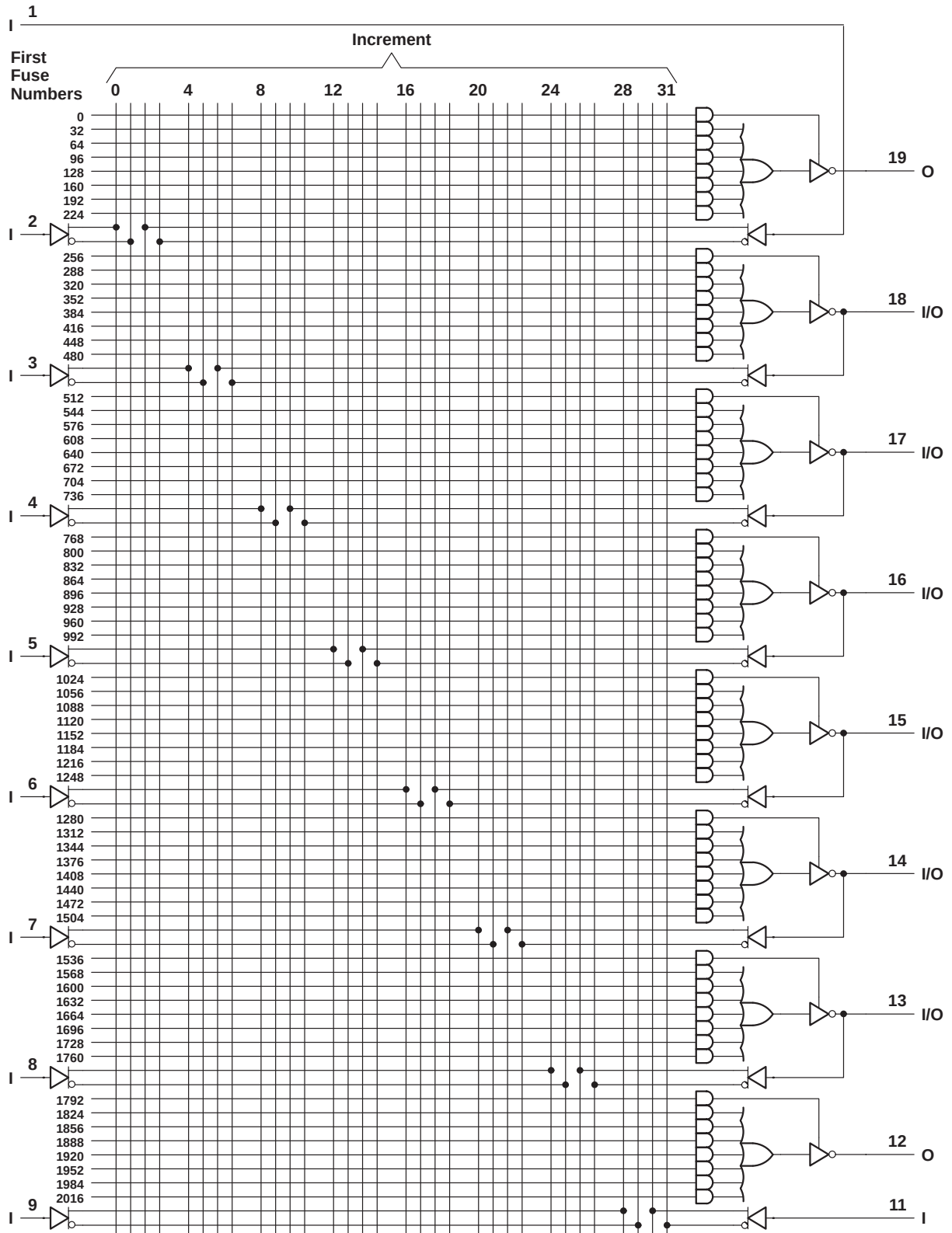
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## functional block diagrams (positive logic)



~ denotes fused inputs

logic diagram (positive logic)

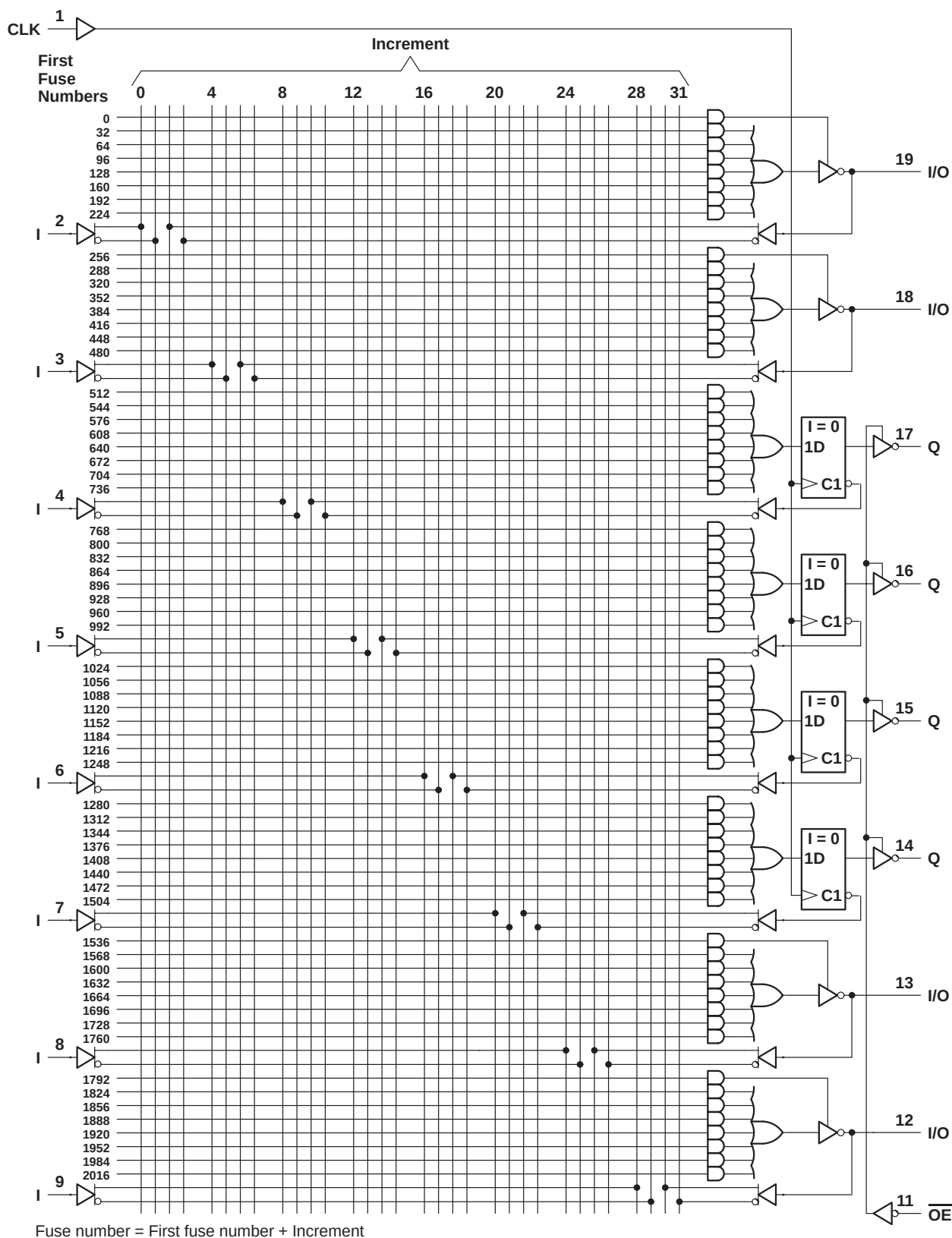


Fuse number = First fuse number + Increment

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## logic diagram (positive logic)



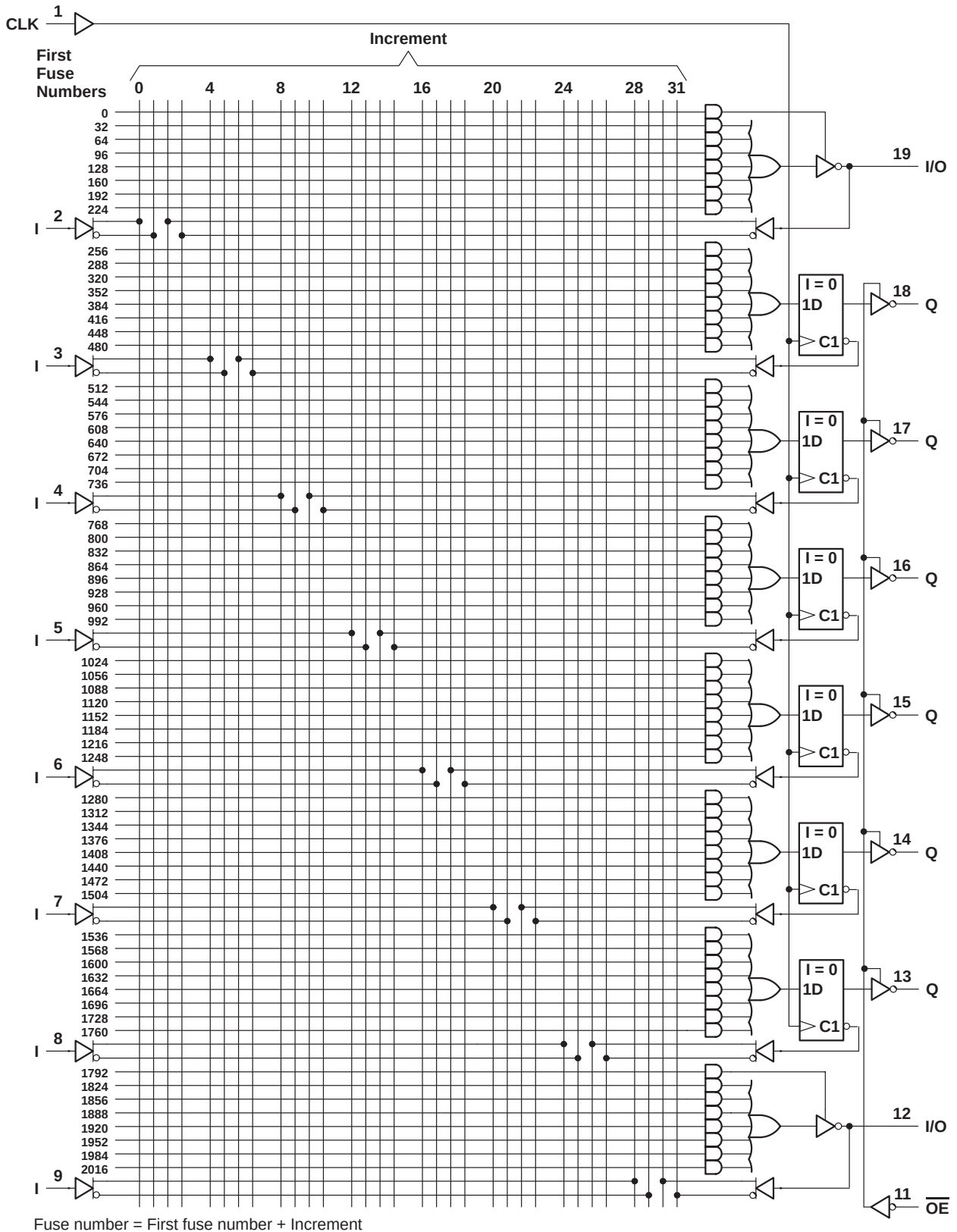
TEXAS  
INSTRUMENTS

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# PAL16R6AM, PAL16R6A-2M STANDARD HIGH-SPEED PAL® CIRCUITS

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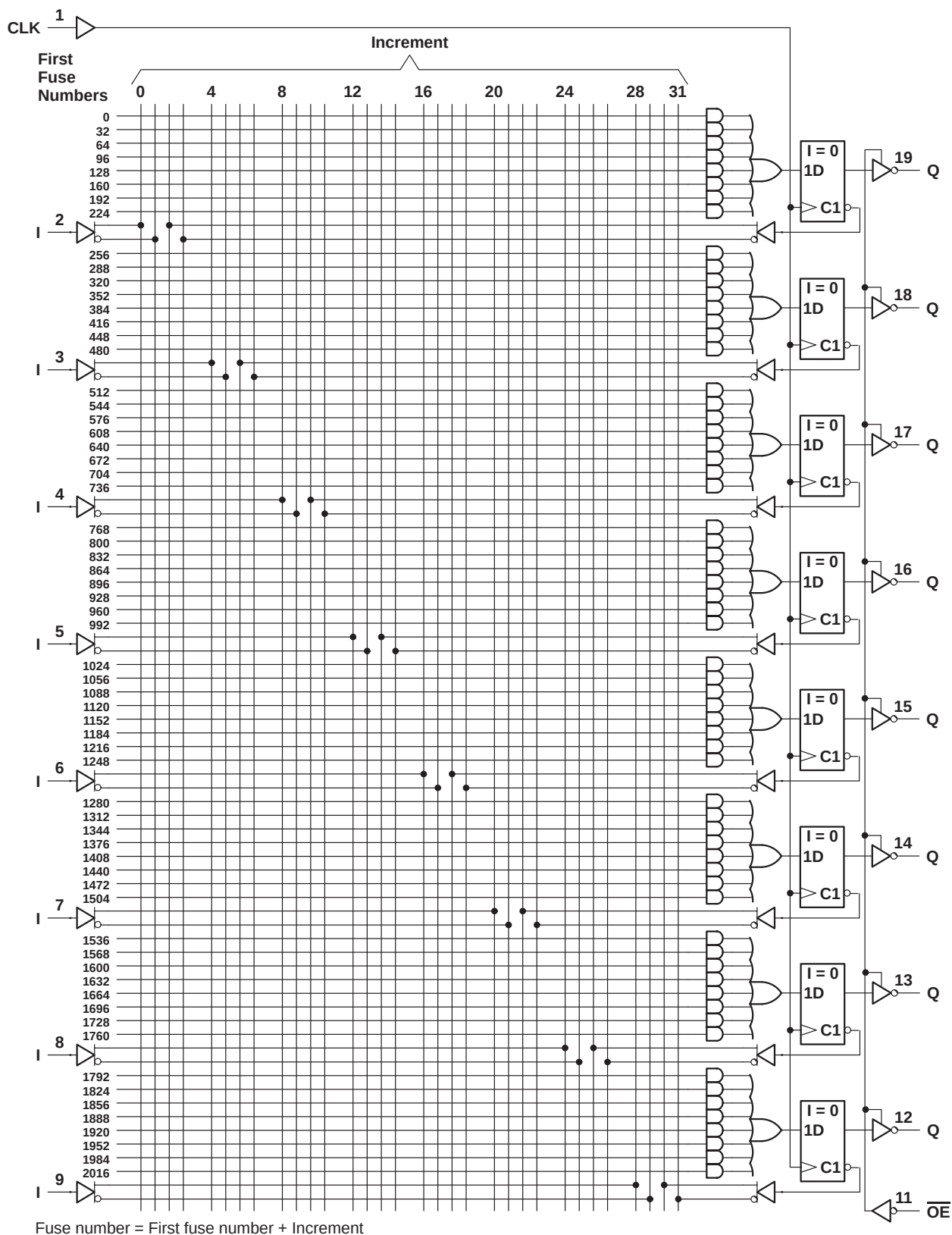
## logic diagram (positive logic)



# PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

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## logic diagram (positive logic)





## programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                                 |                |
|-------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)           | 7 V            |
| Input voltage (see Note 1)                      | 5.5 V          |
| Voltage applied to disabled output (see Note 1) | 5.5 V          |
| Operating free-air temperature range            | –55°C to 125°C |
| Storage temperature range                       | –65°C to 150°C |

NOTE 1: These ratings apply except for programming pins during a programming cycle.

## recommended operating conditions

|          |                                | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|-----|-----|-----|------|
| $V_{CC}$ | Supply voltage                 | 4.5 | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       | 2   |     | 5.5 | V    |
| $V_{IL}$ | Low-level input voltage        |     |     | 0.8 | V    |
| $I_{OH}$ | High-level output current      |     |     | –2  | mA   |
| $I_{OL}$ | Low-level output current       |     |     | 12  | mA   |
| $T_A$    | Operating free-air temperature | –55 | 25  | 125 | °C   |

# PAL16L8AM, PAL16R4AM, PAL16R6AM, PAL16R8AM STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

## electrical characteristics over recommended operating free-air temperature range

| PARAMETER           |                              | TEST CONDITIONS           |                             | MIN | TYP <sup>†</sup> | MAX  | UNIT          |
|---------------------|------------------------------|---------------------------|-----------------------------|-----|------------------|------|---------------|
| $V_{IK}$            |                              | $V_{CC} = 4.5\text{ V}$ , | $I_I = -18\text{ mA}$       |     |                  | -1.5 | V             |
| $V_{OH}$            |                              | $V_{CC} = 4.5\text{ V}$ , | $I_{OH} = -2\text{ mA}$     | 2.4 | 3.2              |      | V             |
| $V_{OL}$            |                              | $V_{CC} = 4.5\text{ V}$ , | $I_{OL} = 12\text{ mA}$     |     | 0.25             | 0.4  | V             |
| $I_{OZH}$           | Outputs                      | $V_{CC} = 5.5\text{ V}$ , | $V_O = 2.7\text{ V}$        |     |                  | 20   | $\mu\text{A}$ |
|                     | I/O ports                    |                           |                             |     |                  | 100  |               |
| $I_{OZL}$           | Outputs                      | $V_{CC} = 5.5\text{ V}$ , | $V_O = 0.4\text{ V}$        |     |                  | -20  | $\mu\text{A}$ |
|                     | I/O ports                    |                           |                             |     |                  | -100 |               |
| $I_I$               |                              | $V_{CC} = 5.5\text{ V}$ , | $V_I = 5.5\text{ V}$        |     |                  | 0.2  | mA            |
| $I_{IH}$            | I/O Ports                    | $V_{CC} = 5.5\text{ V}$ , | $V_I = 2.7\text{ V}$        |     |                  | 100  | $\mu\text{A}$ |
|                     | All others                   |                           |                             |     |                  | 25   |               |
| $I_{IL}$            | $\overline{\text{OE}}$ input | $V_{CC} = 5.5\text{ V}$ , | $V_I = 0.4\text{ V}$        |     |                  | -0.2 | mA            |
|                     | All others                   |                           |                             |     |                  | -0.1 |               |
| $I_{OS}^{\ddagger}$ |                              | $V_{CC} = 5.5\text{ V}$ , | $V_O = 0.5\text{ V}$        | -30 |                  | -250 | mA            |
| $I_{CC}$            |                              | $V_{CC} = 5.5\text{ V}$ , | $V_I = 0$ ,<br>Outputs open |     | 75               | 180  | mA            |

## timing requirements

|                    |                                                           |            | MIN | MAX | UNIT |
|--------------------|-----------------------------------------------------------|------------|-----|-----|------|
| $f_{\text{clock}}$ | Clock Frequency                                           |            | 0   | 25  | MHz  |
| $t_w$              | Pulse duration (see Note 2)                               | Clock high | 15  |     | ns   |
|                    |                                                           | Clock low  | 20  |     |      |
| $t_{\text{su}}$    | Setup time, input or feedback before $\text{CLK}\uparrow$ |            | 25  |     | ns   |
| $t_h$              | Hold time, input or feedback after $\text{CLK}\uparrow$   |            | 0   |     | ns   |

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency,  $f_{\text{clock}}$ . The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER        | FROM (INPUT)                     | TO (OUTPUT) | TEST CONDITION                                             | MIN | TYP <sup>†</sup> | MAX | UNIT |
|------------------|----------------------------------|-------------|------------------------------------------------------------|-----|------------------|-----|------|
| $f_{\text{max}}$ |                                  |             | R1 = 390 $\Omega$ ,<br>R2 = 750 $\Omega$ ,<br>See Figure 1 | 25  | 45               |     | MHz  |
| $t_{\text{pd}}$  | I, I/O                           | O, I/O      |                                                            |     | 15               | 30  | ns   |
| $t_{\text{pd}}$  | $\text{CLK}\uparrow$             | Q           |                                                            |     | 10               | 20  | ns   |
| $t_{\text{en}}$  | $\overline{\text{OE}}\downarrow$ | Q           |                                                            |     | 15               | 25  | ns   |
| $t_{\text{dis}}$ | $\overline{\text{OE}}\uparrow$   | Q           |                                                            |     | 10               | 25  | ns   |
| $t_{\text{en}}$  | I, I/O                           | O, I/O      |                                                            |     | 14               | 30  | ns   |
| $t_{\text{dis}}$ | I, I/O                           | O, I/O      |                                                            |     | 13               | 30  | ns   |

<sup>†</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set  $V_O$  at 0.5 V to avoid test equipment degradation.

# PAL16L8A-2M, PAL16R4A-2M, PAL16R6A-2M, PAL16R8A-2M STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

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## electrical characteristics over recommended operating free-air temperature range

| PARAMETER           |                       | TEST CONDITIONS           |                             | MIN | TYP <sup>†</sup> | MAX  | UNIT          |
|---------------------|-----------------------|---------------------------|-----------------------------|-----|------------------|------|---------------|
| $V_{IK}$            |                       | $V_{CC} = 4.5\text{ V}$ , | $I_I = -18\text{ mA}$       |     |                  | -1.5 | V             |
| $V_{OH}$            |                       | $V_{CC} = 4.5\text{ V}$ , | $I_{OH} = -2\text{ mA}$     | 2.4 | 3.2              |      | V             |
| $V_{OL}$            |                       | $V_{CC} = 4.5\text{ V}$ , | $I_{OL} = 12\text{ mA}$     |     | 0.25             | 0.4  | V             |
| $I_{OZH}$           | Outputs               | $V_{CC} = 5.5\text{ V}$ , | $V_O = 2.7\text{ V}$        |     |                  | 20   | $\mu\text{A}$ |
|                     | I/O ports             |                           |                             |     |                  | 100  |               |
| $I_{OZL}$           | Outputs               | $V_{CC} = 5.5\text{ V}$ , | $V_O = 0.4\text{ V}$        |     |                  | -20  | $\mu\text{A}$ |
|                     | I/O ports             |                           |                             |     |                  | -100 |               |
| $I_I$               |                       | $V_{CC} = 5.5\text{ V}$ , | $V_I = 5.5\text{ V}$        |     |                  | 0.2  | mA            |
| $I_{IH}$            | I/O Ports             | $V_{CC} = 5.5\text{ V}$ , | $V_I = 2.7\text{ V}$        |     |                  | 100  | $\mu\text{A}$ |
|                     | All others            |                           |                             |     |                  | 25   |               |
| $I_{IL}$            | $\overline{OE}$ input | $V_{CC} = 5.5\text{ V}$ , | $V_I = 0.4\text{ V}$        |     |                  | -0.2 | mA            |
|                     | All others            |                           |                             |     |                  | -0.1 |               |
| $I_{OS}^{\ddagger}$ |                       | $V_{CC} = 5.5\text{ V}$ , | $V_O = 0.5\text{ V}$        | -30 |                  | -250 | mA            |
| $I_{CC}$            |                       | $V_{CC} = 5.5\text{ V}$ , | $V_I = 0$ ,<br>Outputs open |     | 75               | 90   | mA            |

## timing requirements

|                    |                                                           |            | MIN | MAX | UNIT |
|--------------------|-----------------------------------------------------------|------------|-----|-----|------|
| $f_{\text{clock}}$ | Clock Frequency                                           |            | 0   | 16  | MHz  |
| $t_w$              | Pulse duration (see Note 2)                               | Clock high | 25  |     | ns   |
|                    |                                                           | Clock low  | 25  |     |      |
| $t_{\text{su}}$    | Setup time, input or feedback before $\text{CLK}\uparrow$ |            | 35  |     | ns   |
| $t_h$              | Hold time, input or feedback after $\text{CLK}\uparrow$   |            | 0   |     | ns   |

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency,  $f_{\text{clock}}$ . The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

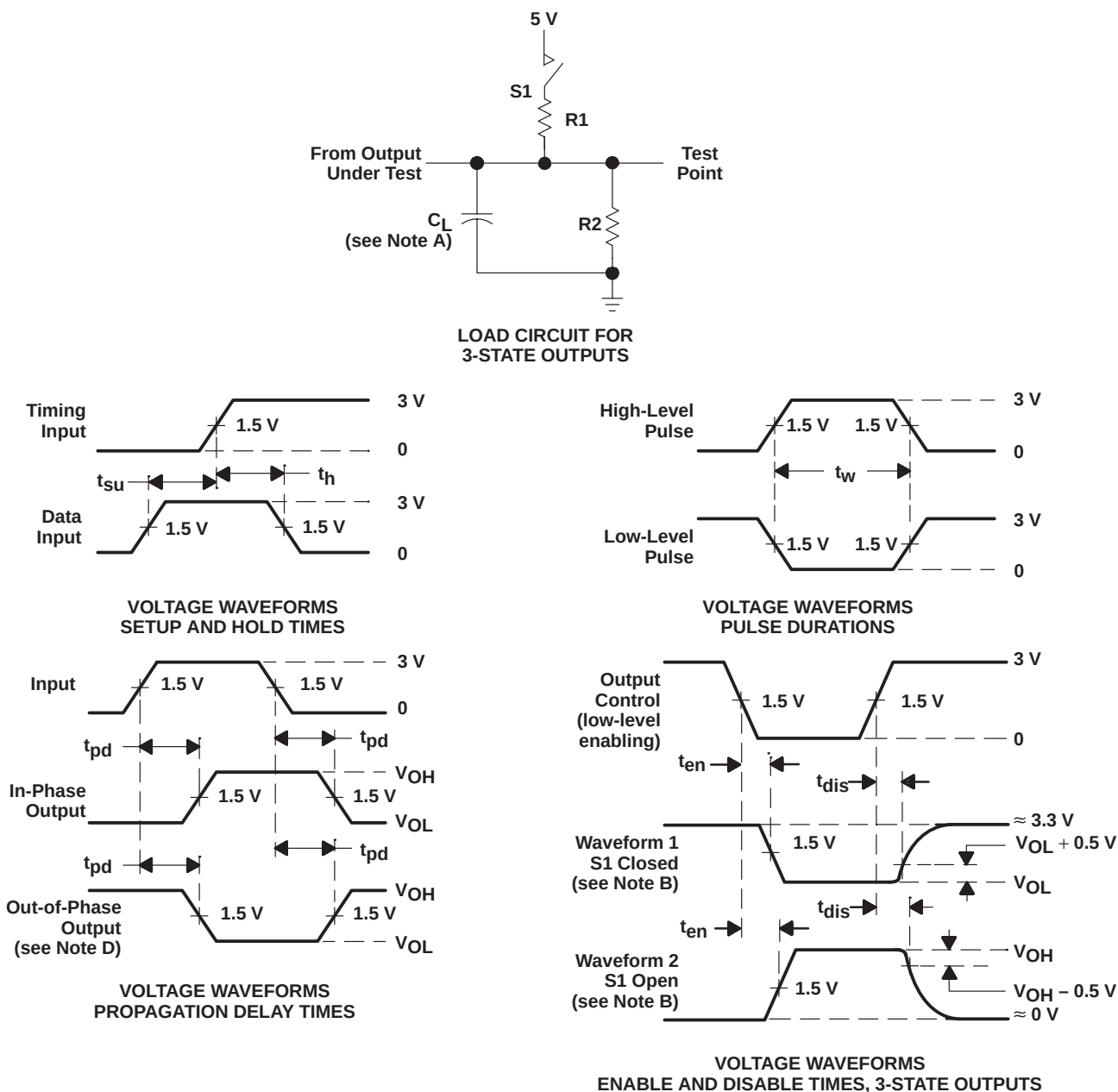
## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER        | FROM (INPUT)              | TO (OUTPUT) | TEST CONDITION                                             | MIN | TYP <sup>†</sup> | MAX | UNIT |
|------------------|---------------------------|-------------|------------------------------------------------------------|-----|------------------|-----|------|
| $f_{\text{max}}$ |                           |             | R1 = 390 $\Omega$ ,<br>R2 = 750 $\Omega$ ,<br>See Figure 1 | 16  | 25               |     | MHz  |
| $t_{\text{pd}}$  | I, I/O                    | O, I/O      |                                                            |     | 25               | 40  | ns   |
| $t_{\text{pd}}$  | $\text{CLK}\uparrow$      | Q           |                                                            |     | 11               | 25  | ns   |
| $t_{\text{en}}$  | $\overline{OE}\downarrow$ | Q           |                                                            |     | 20               | 25  | ns   |
| $t_{\text{dis}}$ | $\overline{OE}\uparrow$   | Q           |                                                            |     | 11               | 25  | ns   |
| $t_{\text{en}}$  | I, I/O                    | O, I/O      |                                                            |     | 25               | 40  | ns   |
| $t_{\text{dis}}$ | I, I/O                    | O, I/O      |                                                            |     | 25               | 35  | ns   |

<sup>†</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set  $V_O$  at 0.5 V to avoid test equipment degradation.

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance and is 50 pF for  $t_{pd}$  and  $t_{en}$ , 5 pF for  $t_{dis}$ .  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses have the following characteristics:  $PRR \leq 10$  MHz,  $t_r$  and  $t_f \leq 2$  ns, duty cycle = 50%  
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.  
 E. Equivalent loads may be used for testing.

Figure 1. Load Circuit and Voltage Waveforms

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