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PowerPC™

Advance Information

PowerPC 604e ™ RISC Microprocessor Family: PID9t-604e Hardware Specifications

The PID9t-604e microprocessor is an implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. In this document, the term "604e" and "PID9t-604e" are used as an abbreviation for the phrase "PowerPC 604e microprocessor." This document contains pertinent physical characteristics of the PID9t-604e.

This document contains the following topics:

1.0 General Parameters

Technology	0.35 µm CMOS 6S, five-layer metal
Die Size	96 mm^2
Transistor Count	5.5 Million
Packages	BGA, 255 ball array PGA, 288 pin array
Voltage	2.5 VDC ± 5% Processor Core (Vdd) 3.3 VDC ± 5% I/O (OVdd)
Maximum Power Dissipation	13.3 W @ 233 MHz
Typical Power Dissipation	7.2 W at 233MHz, 2.5V Core (Vdd) 0-1 W at 233 MHz, 3.3V I/O (OVdd)

1.1 DC Electrical and Thermal Characteristics

This section provides both the DC electrical specifications and thermal characteristics for the PID9t-604e. The following specifications are preliminary and subject to change without notice. They are based on preliminary characterization of early manufacturing process samples.

1.2 DC Electrical Characteristics

Table 1 and Table 2 provide the absolute maximum rating and thermal characteristics for the PID9t-604e.

Table 1. PowerPC PID9t-604e Microprocessor Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	-0.3 to 2.7	V
PLL supply voltage	AVdd	-0.3 to 2.7	V
I/O supply voltage	OVdd	-0.3 to 3.6	V
Input voltage	V_{in}	-0.3 to 5.5	V
Storage temperature range	T_{stg}	-55 to 150	°C

Notes:

1. Functional operating conditions are given in DC Electrical Specifications. Absolute maximum ratings are stress ratings only , and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{in} must not be greater than OVdd by more than 2.5 V at all times including during power-on reset.
3. **Caution:** Ovdd must not exceed Vdd/AVdd by more than 1.2 V at any time including during power-on reset.
4. **Caution:** Vdd/Avdd must not exceed OVdd by more than 0.4 V at any time including during power-on reset.

Table 2. . PowerPC PID9t-604e Microprocessor Thermal Characteristics

Characteristic	Symbol	Value	Rating
BGA package thermal resistance, junction-to-case	θ_{JC}	0.03	°C/W
PGA package thermal resistance, junction-to-case	θ_{JC}	1.073	°C/W

Notes:
1. For the BGA package, the θ_{JC} measurement is made from die junction to the back of the bare silicon die.
2. The junction temperature of the chip is a function of several parameters including θ_{JC}.
3. For the PGA package, the θ_{JC} value is an estimate based on mechanical and thermal properties as shown on drawings.

Table 3 provides the DC electrical characteristics for the PID9t-604e.

Table 3. DC Electrical Specifications

AVdd=Vdd = 2.5± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	V_{IH}	2.0	5.5	V	
Input low voltage (all inputs except SYSCLK)	V_{IL}	0	0.8	V	
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V	
SYSCLK input low voltage	CV_{IL}	0.0	0.4	V	
Input leakage current, V_{in} = 3.465 V	I_{in}	—	10	µA	1
V_{in} = 5.5 V	I_{in}	—	245	µA	1
Hi-Z (off state) leakage current, V_{in} = 3.465 V	I_{TSI}	—	10	µA	1
V_{in} = 0.0 V	I_{TSI}	-10		µA	1
V_{in} = 5.5 V	I_{TSI}	—	245	µA	1
Output high voltage, I_{OH} = –9 mA	V_{OH}	2.4	—	V	
Output low voltage, I_{OL} = 9 mA	V_{OL}	—	0.4	V	
Capacitance, V_{in} =0 V, f = 1 MHz (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	10	pF	2
Capacitance, V_{in} =0 V, f = 1 MHz (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	15	pF	2
Output Impedance Normal Mode Strong Mode Herculean Mode	Z_o	 25 20 15	 75 60 45	Ω	

Notes:
1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals.)
2. Capacitance is periodically sampled rather than 100% tested.

Table 4 provides the power dissipation numbers for the PID9t-604e.

Table 4. . PowerPC PID9t-604e Microprocessor Power Dissipation

	Processor Core Frequency			Unit	Notes
	200 MHz	225 MHz	233 MHz		
Full-On Mode					1
Typical	6.5	7.0	7.2	W	2
Maximum	12.1	13.0	13.3	W	3
Nap Mode					4
Maximum	0.78	0.79	0.80	W	4

Notes:
1. Power **measured** including Vdd and Ovdd at nominal levels.
2. Typical power is an average value measured at nominal voltages in a system executing typical applications and benchmark sequences.
3. Maximum power is measured using worst case benchmark sequences, applications and test patterns at nominal voltages This value should be used for system thermal design.
4. Nap Mode maximums are measured with full nap, and no bus activity.

1.3 AC Electrical Characteristics

This section provides the AC electrical characteristics for the PID9t-604e. These specifications are for parts that operate at processor core frequencies of 200, 225 and 233 MHz. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0–PLL_CFG3 pins. All timings are specified respective to the SYSCLK.

1.4 Clock AC Specifications

Table 5 provides the clock AC timing specifications as defined in 1.

Table 5. . PowerPC PID9t-604e Microprocessor Clock AC Timing Specifications

AVdd=Vdd = 2.5± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Num	Characteristic	200 MHz		225 MHz		233 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
	Frequency of operation	110	200	125	225	130	233	MHz	1
	Frequency of VCO	275	500	275	500	275	500	MHz	2
	SYSCLK frequency	33.3	66.67	33.3	66.67	33.3	66.67	MHz	3,4
1	SYSCLK cycle time	15.0	30.0	15.0	30.0	15.0	30.0	ns	
2,3	SYSCLK rise and fall time	1.0	2.0	1.0	2.0	1.0	2.0	ns	5

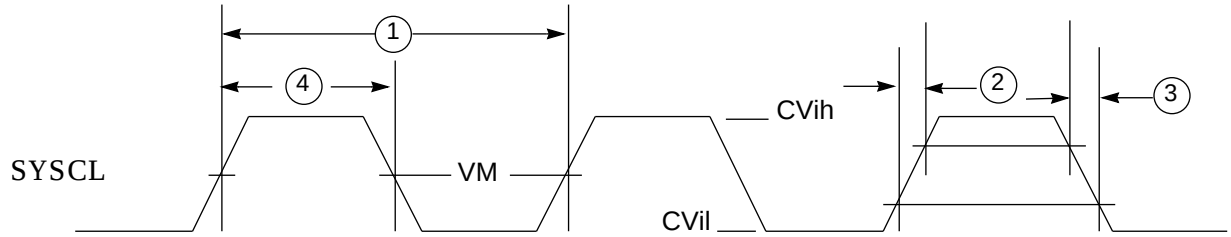
Table 5. . PowerPC PID9t-604e Microprocessor Clock AC Timing Specifications (Continued)

Num	Characteristic	200 MHz		225 MHz		233 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
4	SYSCLK duty cycle measured at 1.4 V	40	60	40	60	40	60	%	
	SYSCLK jitter	—	±150	—	±150	—	±150	ps	6
	Internal PLL relock time	—	100	—	100	—	100	µs	7, 8

Notes:

1. Times shown in specifications are only valid for the range of processor core frequencies specified.
2. **Caution**: The SYSCLK frequency and PLL_CFG0–PLL_CFG3 settings must be chosen such that the resulting CPU (core) frequency and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
3. AC timing specifications are tested up to the maximum SYSCLK (bus) frequency shown in Table 5.
   However, it is theoretically possible to attain higher SYSCLK frequencies if allowed for by system design.
4. These SYSCLK frequencies are applicable for PID9t-604e configured in the normal output mode. If configured for fast-out mode, SYSCLK can be programmed up to 150 MHz.
5. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
6. This number refers to cycle-to-cycle jitter.
7. PLL relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
8. Relock timing is guaranteed by design and is not tested.

Figure 1 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 1. . SYSCLK Input Timing Diagram

1.5 Input AC Specifications

Table 6 provides the input AC timing specifications for the PID9t-604e as defined in Figure 2.

Table 6. . PowerPC PID9t-604e Microprocessor Input AC Timing Specifications

Vdd = 2.5± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Num	Characteristic	200 MHz		225 or 233 MHz		Unit	Notes
		Min	Max	Min	Max		
7a	ARTRY, SHD, ABB, TS, XATS, AACK,BG, DRTRY, TA, DBG, DBB, TEA, DBDIS, and DBWO valid to SYSCLK (setup)	3.0	—	3.0	—	ns	
7b	All other inputs valid to SYSCLK (setup)	2.0	—	2.0	—	ns	1
8	SYSCLK to all inputs invalid (hold)	1.5	—	1.5	—	ns	
9	Mode select input valid to HRESET (input setup for DRTRY)	8 * t_{sysclk}	—	8 * t_{sysclk}	—	ns	2,3,4,5
10	HRESET to mode select input invalid (input hold for DRTRY)	0	—	0	—	ns	2,3,4,5

Notes:

1. All other input signals include the following signals—all inputs except ARTRY, SHD, ABB, TS, XATS, AACK, BG, DRTRY, TA, DBG, DBB, DBWO, DBDIS, TEA, and JTAG inputs.
2. The setup and hold time is with respect to the rising edge of HRESET (see 3).
3. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds.
4. These values are guaranteed by design, and are not tested.
5. Note this is for configuration of the fast-L2 mode and no-DRTRY mode.

Figure 2 provides the input timing diagram for the PID9t-604e.

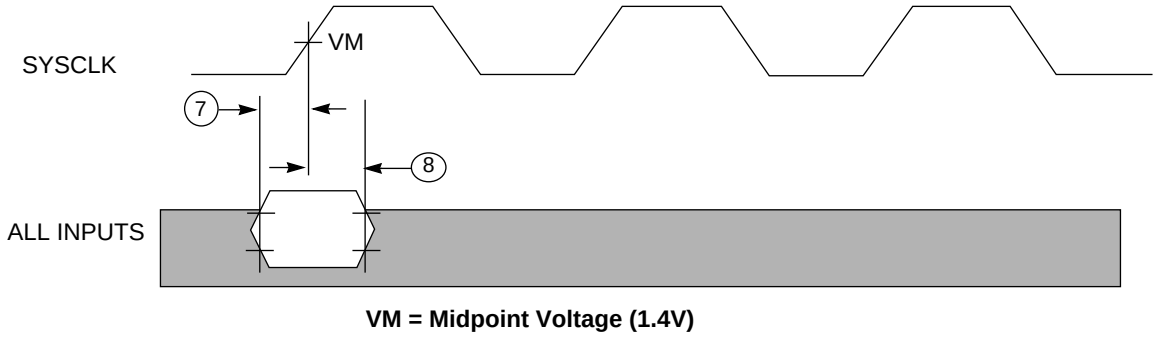


Figure 2. . PowerPC PID9t-604e Microprocessor Input Timing Diagram

Figure 3 provides the timing diagram for the fast-L2 mode/no-$\overline{\text{DRTRY}}$ mode select input.

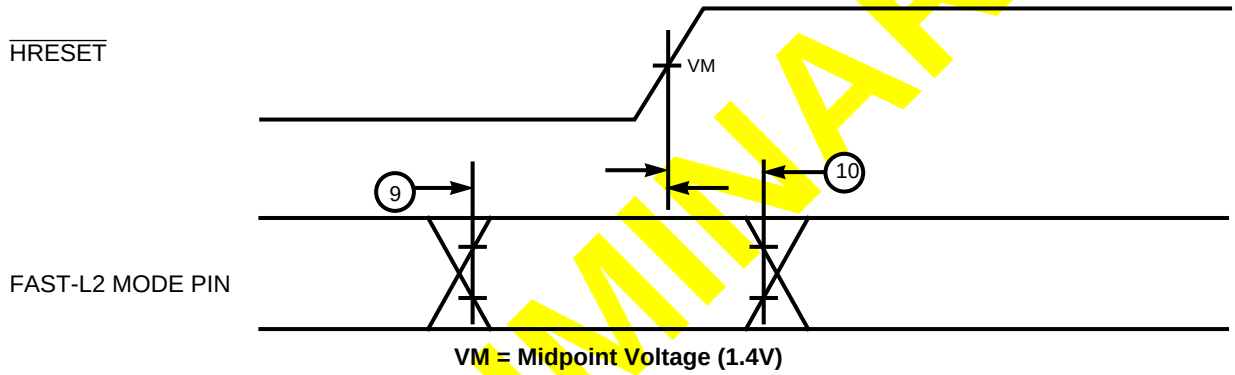


Figure 3. . Fast-L2 Mode/No-$\overline{\text{DRTRY}}$ Mode Select Input Timing Diagram

1.6 Output AC Specifications

Table 7 provides the output AC timing specifications for the PID9t-604e (timing diagram shown in figure 4). Note that the capacitive load (C_L) used for these values is equivalent to a lumped load of 5 pF. The test equipment used to characterize this device has a proprietary transmission line equivalent that has been shown to be comparable to a 5 pF lumped load. It is recommended that these values be used in conjunction with IBIS models to simulate system configurations during the system design phase.

Table 7. . PowerPC PID9t-604e Microprocessor Output AC Timing Specifications

AVdd=Vdd = 2.5± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 5 pF, 0 ≤ T_j ≤ 105 °C Drive Mode [11]

Num	Characteristic	200 MHz			225 or 233 MHz			Unit	Note
		Min	Max	Fast Out[6]	Min	Max	Fast Out[6]		
11	SYSCLK to output driven (output enable time)	0.75	—	—	0.75	—	—	ns	1
12a	SYSCLK to TS, XATS, ARTRY, SHD, ABB, and DBB output valid (for 5.5 V to 0.8 V)	—	6.0	5.5 Max	—	5.8	5.3 Max	ns	2
12b	SYSCLK to TS, XATS, ARTRY, SHD, ABB, and DBB output valid (for 3.6 V to 0.8 V)	—	5.5	5.0 Max	—	5.3	4.8 Max	ns	
13a	SYSCLK to all other signals output valid (for 5.5 V to 0.8 V)	—	6.8	6.3 Max	—	6.6	6.1 Max	ns	2
13b	SYSCLK to all other signals output valid (for 3.6 V to 0.8 V)	—	6.3	5.8 Max	—	6.1	5.6 Max	ns	
14	SYSCLK to output invalid (output hold)	0	—	—	0	—	—	ns	3
15	SYSCLK to output high impedance (all signals except ARTRY, SHD, ABB, DBB, TS, and XATS)	—	5.0	—	—	5.0	—	ns	
16	SYSCLK to output high impedance TS, XATS	—	5.0	—	—	5.0	—	ns	
17	SYSCLK to ABB and DBB high impedance after precharge	—	1.0* t_{sysclk}	—	—	1.0* t_{sysclk}	—	ns	4
18	SYSCLK to ARTRY and SHD high impedance before precharge	—	4.5	—	—	4.0	—	ns	
19	SYSCLK to ARTRY and SHD precharge enable	—	0.5* t_{sysclk} + 0.75	—	—	0.5* t_{sysclk} + 0.75	—	ns	4
20	Maximum delay to ARTRY and SHD precharge	—	1.5* t_{sysclk}	—	—	1.5* t_{sysclk}	—	ns	4

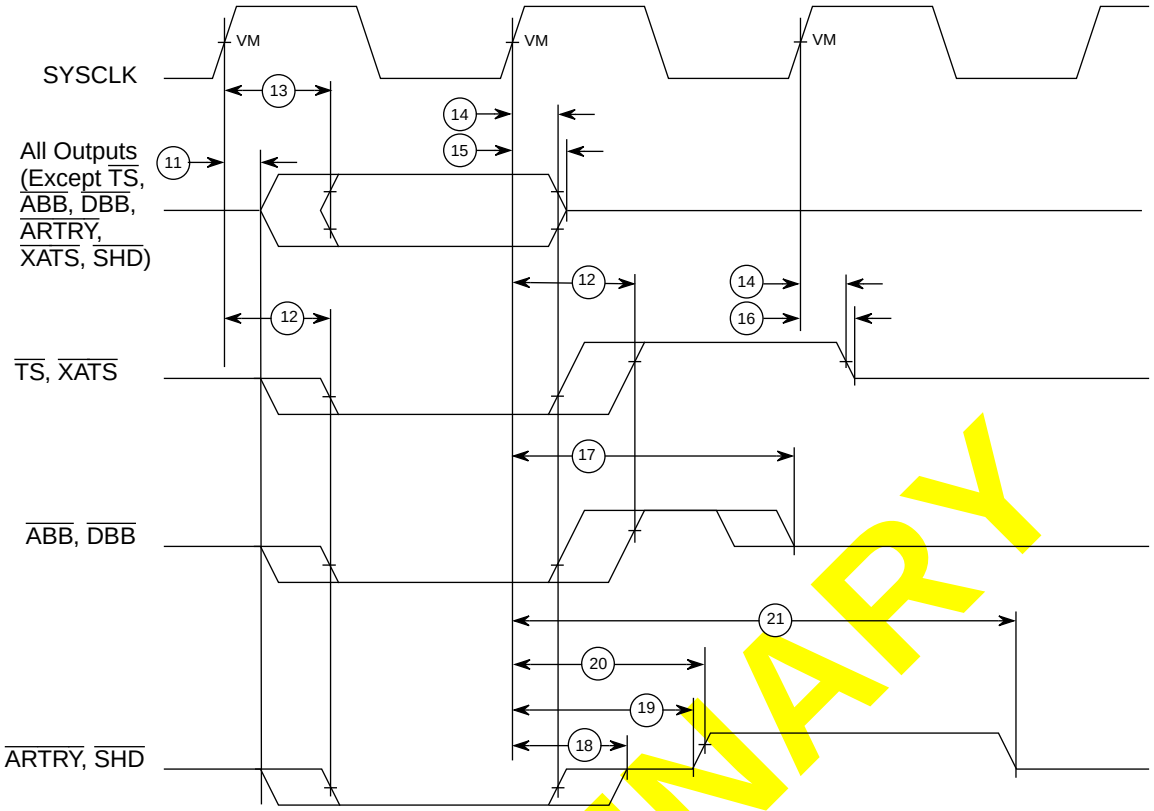
Table 7. . PowerPC PID9t-604e Microprocessor Output AC Timing Specifications (Continued)

Num	Characteristic	200 MHz			225 or 233 MHz			Unit	Note
		Min	Max	Fast Out[6]	Min	Max	Fast Out[6]		
21	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ high impedance after precharge	—	2.0* t_{sysclk}	—	—	2.0* t_{sysclk}	—	ns	4
	Rise time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		—	1.0		—	ns	5
	Rise time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		—	1.0		—	ns	5
	Fall time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		—	1.0		—	ns	5
	Fall time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		—	1.0		—	ns	5

Notes:

1. These values are guaranteed by design, and are not tested.
2. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from 3.6 V to 0.8 V (5-V CMOS levels instead of 3.3-V CMOS levels).
3. This minimum parameter assumes C_L=0pF
4. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{sysclk} the numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
5. These specifications are nominal values.
6. Fast Out mode only affects output valid timings. For all other timings, use the value indicated in the appropriate Min or Max column.

Figure 4 provides the output timing diagram for the PID9t-604e.



Notes: VM = Midpoint voltage (1.4 V)
All output specifications are measured from 0.8 V or 2.0 V of the signal in question to the 1.4 V of the rising edge of the input SYSCLK.

Figure 4. . PowerPC PID9t-604e Microprocessor Output Timing Diagram

1.7 Output Drive Strength information

The output drivers for PID9t-604e have three programmable output impedances. These outputs are selected at power on time based on the hard-wired setting of the DRVMOD(0..1) pins. In addition to the three operating output impedances, the output drivers can be disabled. Table 8 shows the settings for the DRVMOD(0..1) pins and their associated output impedance. Note that the output AC timing specifications shown in Table 7 are for the herculean mode setting.

Table 8. Output Drive Impedance Selection

DRVMOD(0..1)	Drive Description	Output Impedance, Ohms
00	Disabled	---
01	Normal	50
10	Strong	40
11	Herculean	30

1.8 Built-in Silicon Decoupling Capacitors

The PID9t-604e has built-in decoupling capacitors included in the device. On early versions of the PID9t-604e these decoupling capacitors could be enabled or disabled externally by tying the package appropriate pin to ground or OVdd. Late versions of the processor do not provide external control of the built-in decoupling capacitors. Table 9 below shows the pin assignments for pre- and post- DD2.3. Please refer to the Application Note AN-019 for complete description of this characteristic and revision dependent details..

Table 9: DCAP Pin Assignments

Package/ Pin	Signal Assignment	
	PID9t-604e Pre DD2.3	PID9t-604e Post DD2.3
BGA/D03	DCAP	NC
PGA/E05	DCAP	NC

Use of the built-in decoupling capacitors should not alter any system design plans for power plane decoupling. The built-in decoupling capacitors will only affect internal or core noise immunity. External decoupling will still be required for noise reduction.

1.9 JTAG AC Timing Specifications

Table 10 provides the JTAG AC timing specifications.

Table 10. JTAG AC Timing Specifications (Independent of SYSCLK)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.5 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	1
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary-scan input data setup time	0	—	ns	
7	Boundary-scan input data hold time	27	—	ns	
8	TCK to output data valid	4	25	ns	
9	TCK to output high impedance	3	24	ns	
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	35	—	ns	2
12	TCK to TDO data valid	4	24	ns	3
13	TCK to TDO high impedance	3	15	ns	3

Notes:

1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes.
2. Signal must be held to at least the next falling edge of the TCK. See Figure 8.
3. Load capacitance = 50 pF.

5 provides the JTAG clock input timing diagram.

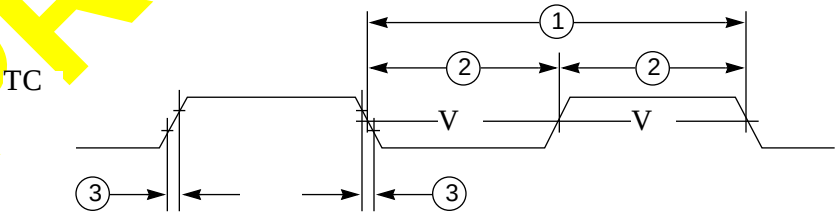


Figure 5. . Clock Input Timing Diagram

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.

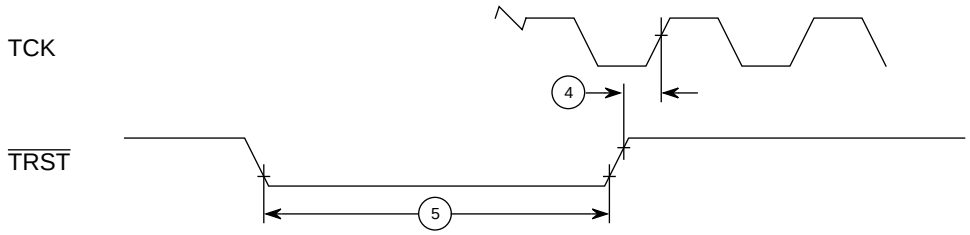


Figure 6. . $\overline{\text{TRST}}$ Timing Diagram

Figure 7 provides the boundary-scan timing diagram.

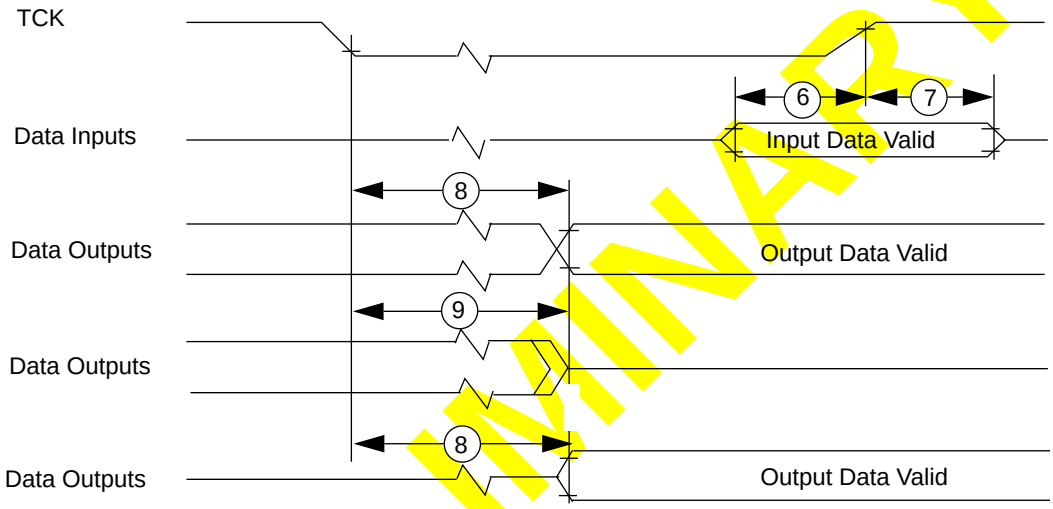


Figure 7. . Boundary-Scan Timing Diagram

Figure 8 provides the test access port timing diagram.

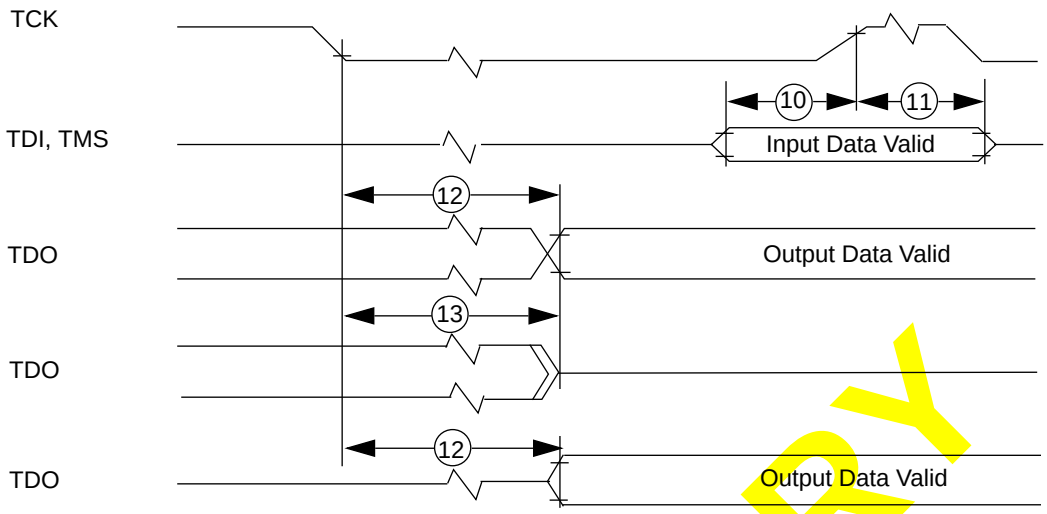


Figure 8. . Test Access Port Timing Diagram

1.10 PowerPC PID9t-604e Microprocessor Package Data

The following sections contain the pinout diagrams and mechanical package descriptions for the IBM BGA and PGA packages.

1.11 Package Description for the BGA Package

Shown below are the mechanical drawings and dimensions for the PID9t-604e BGA package.

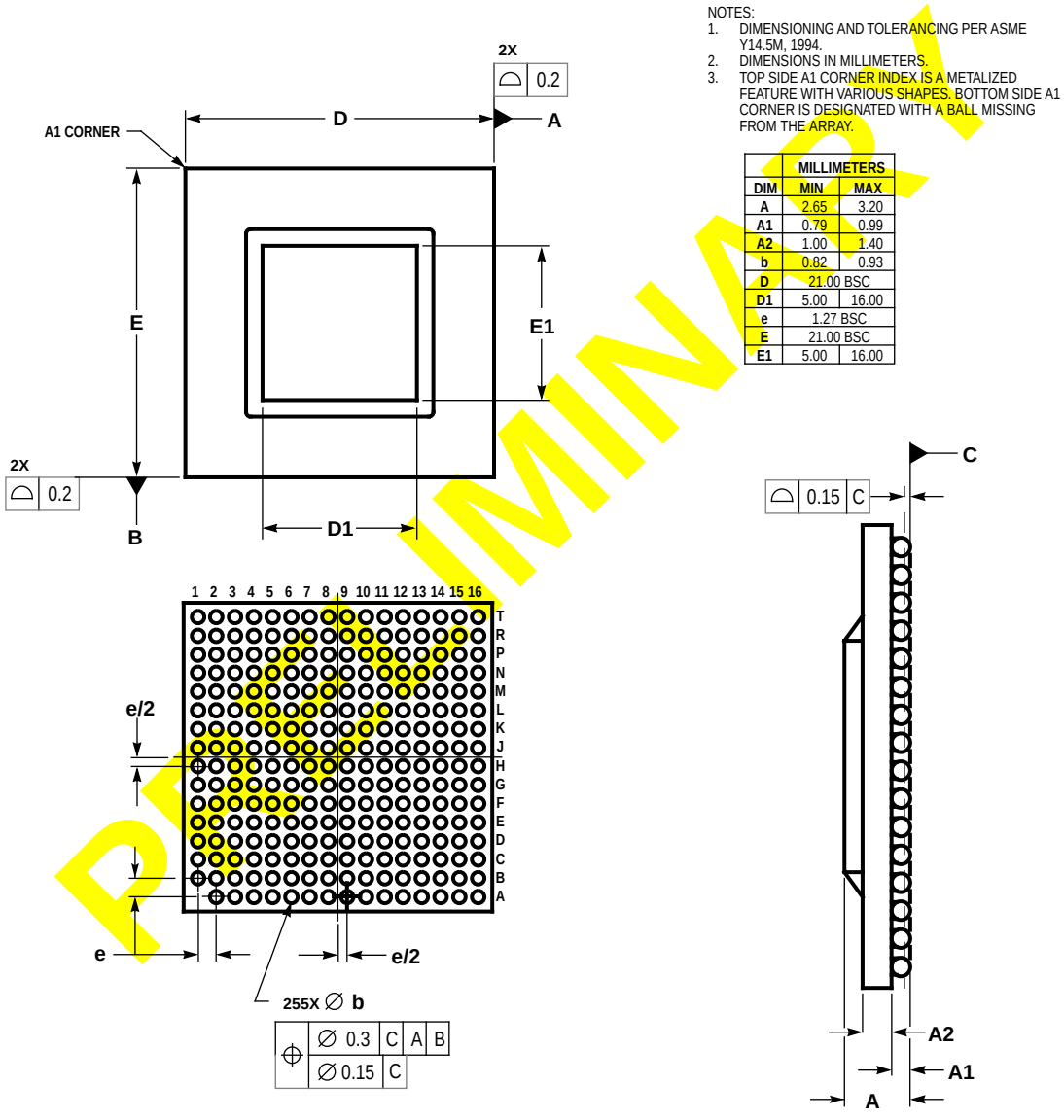


Figure 9. Drawings and Dimensions of the PID9t-604e BGA package

1.12 Package Description for the PGA Package

The following pages are the mechanical drawings and dimensions for the PID9t-604e PGA package.

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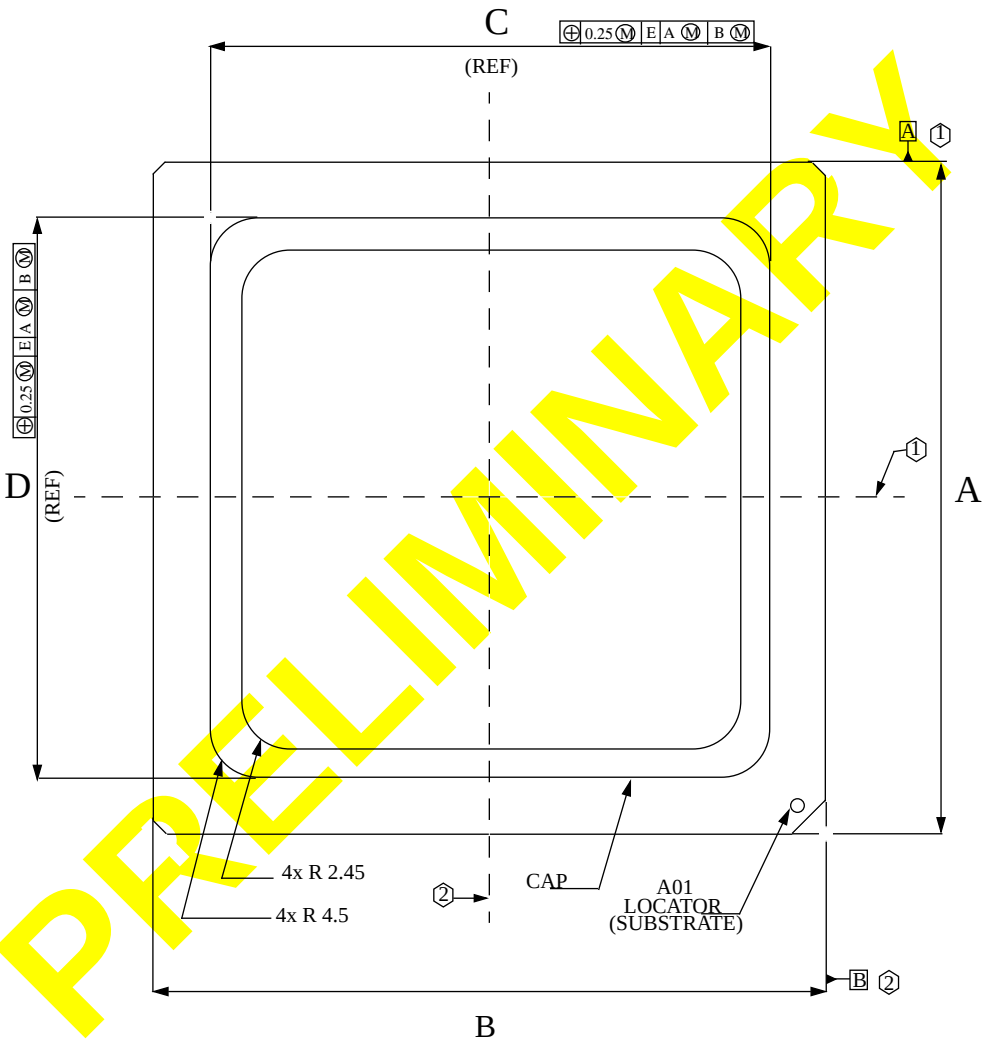
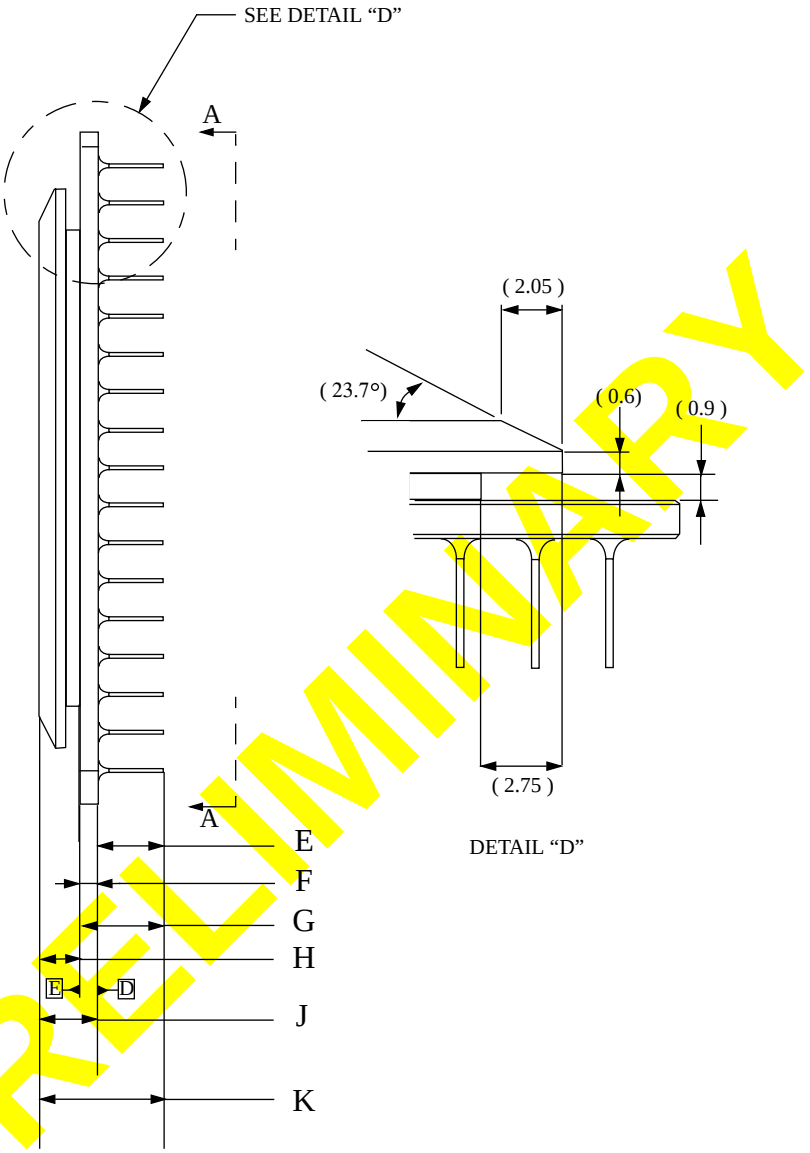


Dimensions shown are mm
Not to scale

Figure 10. Top View of the PID9t-604e PGA package

Figure 11. Side View and Detail of the PID9t-604e PGA package



Dimensions shown are mm
Not to scale

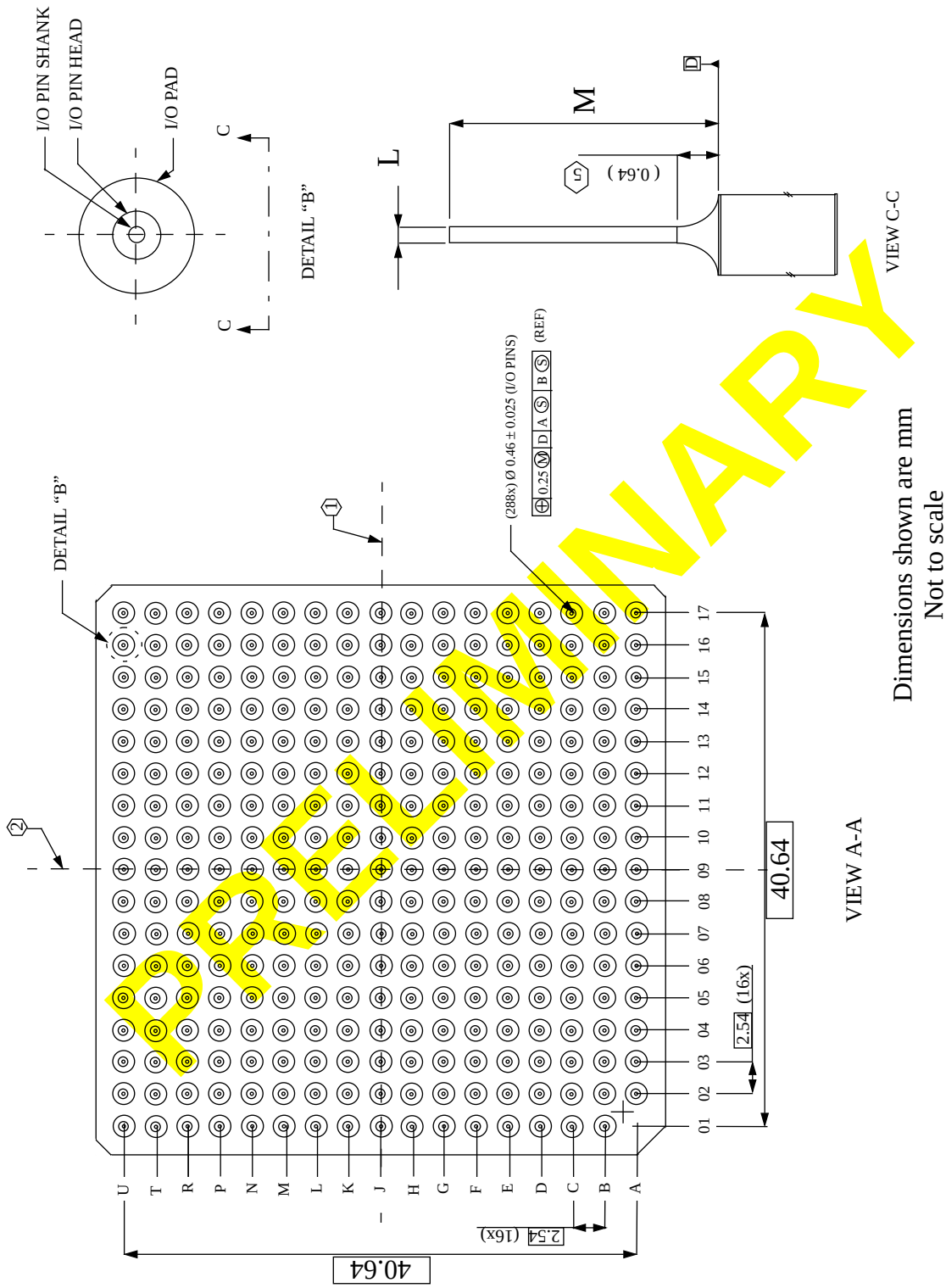


Figure 12. Bottom View and Pin Detail of the IBM 604 PGA package

Notes for PGA drawings:

1. Datum A is the center plane of feature labeled Datum A

2. Datum B is the center plane of feature labeled Datum B

3. Unless otherwise specified, part is symmetrical about centerlines defined by datum A&B

4. Where not otherwise defined, centerlines indicated are to be interpreted as a datum framework established by datums D, A, & B respectively

5. Braze climb during reflows not to increase pin shank dia. beyond a distance of 0.64mm or less from Datum D

6. Chamfer shown around the edge of this assembly may or may not be present

Table 11: 604 PGA Mechanical Dimension Values

Tag	mm		inches	
	Min	Max	Min	Max
A	44.2	44.7	1.740	1.759
B	44.2	44.7	1.740	1.759
C	37 0.08 (REF)		1.457 0.003 (REF)	
D	37 0.08 (REF)		1.457 0.003 (REF)	
E	4.06	4.32	0.16	0.17
F	1.05	1.35	0.041	0.053
G	5.17	5.61	0.203	0.221
H	2.3	2.5	0.09	0.098
J	3.35	3.85	0.132	0.152
K	7.47	8.11	0.294	0.319
L	0.435	0.485	0.017	0.019
M	4.06	4.32	0.16	0.17

1.13 PowerPC PID9t-604e Microprocessor Pinout Listings

1.14 PowerPC PID9t-604e BGA Pinout Listing

Table 12 is the pin listing for the PID9t-604e BGA.

Table 12. PowerPC PID9t-604e Microprocessor Pinout Listing, BGA Package

Signal Name	Pin Number	Active	I/O
A0-A31	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP0-AP3	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	A04	Low	Output
ARRAY_WR[1]	B07	Low	Input
$\overline{\text{ARTRY}}$	J04	Low	I/O
$\overline{\text{AVDD}}$[2]	A10	--	--
$\overline{\text{BG}}$	L01	Low	Input
$\overline{\text{BR}}$	B06	Low	Output
$\overline{\text{CI}}$	E01	Low	Output
$\overline{\text{CKSTP\_IN}}$	D08	Low	Input
$\overline{\text{CKSTP\_OUT}}$	A06	Low	Output
CLK_OUT	D07	--	Output
CSE0-CSE1	B01, B05	High	Output
$\overline{\text{DBB}}$	J14	Low	I/O
$\overline{\text{DBG}}$	N01	Low	Input
$\overline{\text{DBDIS}}$	H15	Low	Input
$\overline{\text{DBWO}}$	G04	Low	Input
DCAP [3]	D03	High	Input
DH0-DH31	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O

Table 12. PowerPC PID9t-604e Microprocessor Pinout Listing, BGA Package

Signal Name	Pin Number	Active	I/O
DL0-DL31	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP0-DP7	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{\text{DPE}}$	A05	Low	Output
$\overline{\text{DRTRY}}$	G16	Low	Input
DRVMOD(0-1)	D05, C03	High	Input
$\overline{\text{GBL}}$	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	--	--
HALTED	B08	High	Output
$\overline{\text{HRESET}}$	A07	Low	Input
$\overline{\text{INT}}$	B15	Low	Input
L1_TEST_CLK [1]	D11	Low	Input
L2_INT	D06	High	Input
L2_TEST_CLK [1]	D12	Low	Input
$\overline{\text{LSSD\_MODE}}$ [1]	B10	Low	Input
$\overline{\text{MCP}}$	C13	Low	Input
OVDD [3]	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	--	--
PLL_CFG(0-3)	A08, B09, A09, D09	High	Input
$\overline{\text{RSRV}}$	D01	Low	Output
RUN	C08	High	Input
$\overline{\text{SHD}}$	H04	Low	I/O
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	--	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input

Table 12. PowerPC PID9t-604e Microprocessor Pinout Listing, BGA Package

Signal Name	Pin Number	Active	I/O
$\overline{\text{TBST}}$	A14	Low	I/O
TC0-TC2	A02, A03, C06	High	Output
TCK	C11	High	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ0-TSIZ2	A13, D10, B12,	High	Output
TT0-TT4	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
VDD [4]	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11,	--	--
$\overline{\text{VOLT\_DET\_GND}}$[5]	F03	Low	--
$\overline{\text{XATS}}$	J16	Low	I/O

Notes:

1. These are test signals for factory use only and must be pulled up to OVDD for normal machine operation.
2. AVDD is powered by the same voltage as VDD. Please refer to the Section 1.18, “PLL Power Supply Filteringfor details on filter requirements for AVDD.
3. DCAP is tied high to enable on-chip decoupling capacitors. Please consult Application Engineering for more information.
4. VDD and OVDD must be tied to separate voltages in the PID9t-604e OVDD must be tied to 3.3 VDC, and VDD must be tied to 2.5 VDC for normal operation.
5. $\overline{\text{VOLT\_DET\_GND}}$ is tied to ground internally. Contact Application Engineering for more information.

1.15 PowerPC PID9t-604e PGA Pinout Listing

Table 13 is the pin listing for the PID9t-604e PGA

Table 13. PowerPC PID9t-604e Microprocessor Pinout Listing, PGA Package

Signal Name	Pin Number	Active	I/O
A0-A31	F13, E01, D17, F03, E16, F01, E17, G05, F15, G04, G13, G03, F17, G02, G14, G01, G15, H01, G16, H03, G17, J01, H13, H05, H15, J02, H17, J03, J13, L01, K13, M01	High	I/O
$\overline{\text{AACK}}$	K03	Low	Input
$\overline{\text{ABB}}$	L03	Low	I/O
AP0-AP3	E06, C04, C05, A04	High	I/O
$\overline{\text{APE}}$	C08	Low	Output
$\overline{\text{ARRAY\_WR}}$ [1]	A08	Low	Input
$\overline{\text{ARTRY}}$	K05	Low	I/O
$\overline{\text{AVDD}}$ [2]	A11	--	--
$\overline{\text{BG}}$	J05	Low	Input
$\overline{\text{BR}}$	E08	Low	Output
$\overline{\text{CI}}$	E02	Low	Output
$\overline{\text{CKSTP\_IN}}$	C09	Low	Input
$\overline{\text{CKSTP\_OUT}}$	E09	Low	Output
CLK_OUT	A06	--	Output
CSE0-CSE1	E07, B05	High	Output
$\overline{\text{DBB}}$	L17	Low	I/O
$\overline{\text{DBG}}$	K01	Low	Input
$\overline{\text{DBDIS}}$	J15	Low	Input
$\overline{\text{DBWO}}$	J04	Low	Input
DCAP [3]	E05	High	Input
DH0-DH31	P13, N12, T15, U15, R13, U14, N10, P11, T11, U11, R10, U10, U09, T09, N09, P09, R09, U08, R08, U07, N08, P07, T07, U06, R07, R06, N07, U05, T05, U04, R05, U03	High	I/O
DL0-DL31	L16, K15, M17, L14, N17, M15, N16, L13, M13, N15, P17, R17, N14, P15, R16, U16, R14, N11, T13, R12, U13, R11, U12, N03, P03, N04, R02, T01, T03, R04, P05, N06	High	I/O
DP0-DP7	L04, N01, M03, N02, P01, L05, R01, M05	High	I/O

Table 13. PowerPC PID9t-604e Microprocessor Pinout Listing, PGA Package

Signal Name	Pin Number	Active	I/O
$\overline{\text{DPE}}$	B07	Low	Output
$\overline{\text{DRTRY}}$	J17	Low	Input
DRVMOD(0-1)	E03, D03	High	Input
$\overline{\text{GBL}}$	F05	Low	I/O
GND	B04, B08, B10, B14, D02, D06, D12, D16, F04, F06, F08, F10, F12, F14, G07, G09, G11, H02, H06, H08, H10, H12, H16, J07, J09, J11, K02, K06, K08, K10, K12, K16, L07, L09, L11, M04, M06, M08, M10, M12, M14, P02, P06, P12, P16, T04, T08, T10, T14	--	--
HALTED	D09	High	Output
$\overline{\text{HRESET}}$	B09	Low	Input
$\overline{\text{INT}}$	E14	Low	Input
L1_TEST_CLK [1]	B11	Low	Input
L2_INT	A07	High	Input
L2_TEST_CLK [1]	E10	Low	Input
$\overline{\text{LSSD\_MODE}}$ [1]	D11	Low	Input
$\overline{\text{MCP}}$	D15	Low	Input
OVDD [6]	B02, B06, B12, B16, D04, D08, D10, D14, F02, F09, F16, H04, H14, J06, J12, K04, K14, M02, M09, M16, P04, P08, P10, P14, T02, T06, T12, T16	--	--
PLL_CFG(0-3)	A09, A10, A13, C11	High	Input
$\overline{\text{RSRV}}$	D05	Low	Output
RUN	D07	High	Input
$\overline{\text{SHD}}$	L02	Low	I/O
$\overline{\text{SMI}}$	B17	Low	Input
$\overline{\text{SRESET}}$	D13	Low	Input
SYSCLK	C10	--	Input
$\overline{\text{TA}}$	J16	Low	Input
TBEN	E04	High	Input
$\overline{\text{TBST}}$	E12	High	I/O
TC0-TC2	C06, A05, C07	High	Output
TCK	C12	High	Input

Table 13. PowerPC PID9t-604e Microprocessor Pinout Listing, PGA Package

Signal Name	Pin Number	Active	I/O
TDI	B13	High	Input
TDO	A14	High	Output
$\overline{\text{TEA}}$	J14	Low	Input
THERMISTOR [4]	A03, C01		
TMS	C13	High	Input
$\overline{\text{TRST}}$	A12	Low	Input
TS	L15	Low	I/O
TSIZ0-TSIZ2	E11, A15, B15	High	Output
TT0-TT4	A16, C14, C16, C17, E15	High	I/O
UPGRADE PRESENT [5]	C02		
$\overline{\text{WT}}$	D01	Low	Output
VDD [6]	F07, F11, G06, G08, G10, G12, H07, H09, H11, J08, J10, K07, K09, K11, L06, L08, L10, L12, M07, M11	--	--
$\overline{\text{VOLT\_DET\_GND}}$ [7]	C03	High	--
$\overline{\text{XATS}}$	K17	Low	I/O

Notes:

1. These are test signals for factory use only and must be pulled up to OVDD for normal machine operation.
2. AVDD is powered by the same voltage as VDD. Please refer to the Section 1.18, “PLL Power Supply Filtering for details on filter requirements for AVDD.
3. DCAP is tied high to enable internal decoupling capacitors on all pre-DD2.3 processors. Post DD2.3 processors have no DCAP pin, and no external control of internal decoupling capacitors. Please contact Application Engineering for more information.
4. Thermistor pins are reserved for an optional thermistor feature on the PGA package. It is available by special request for engineering parts only. Please contact Application Engineering for more information.
5. Upgrade Present is an internally grounded pin on PGA packages only. Please contact Application Engineering for more information.
6. VDD and OVDD must be tied to separate voltages in the PID9t-604e. OVDD must be tied to 3.3 VDC, and VDD must be tied to 2.5 VDC for normal operation.
7. $\overline{\text{VOLT\_DET\_GND}}$ is a pin that can be used to detect the core voltage requirement during system boot. On the PID9t-604e PGA, this pin is internally tied to OVdd, indicating that Vdd is 2.5 V and OVdd is 3.3V.

1.16 System Design Information

1.17 PLL Configuration

The following table shows the PLL_CFG implementation and the associated CPU and VCO ratios.

Note that the table is organized such that the minimum and maximum VCO frequency from Table 5 on page 4 dictate the ranges of SYSCLK and Core frequencies. PLL configurations must be made such that the core processor frequency and the VCO frequency are not exceeded on a given processor. Additionally, the table indicates some processor and bus frequencies that are outside those specified in Table 5 on page 4. Bus frequencies are system dependent and are not limited by the tester frequencies shown in Table 5 on page 4. Processor frequencies, however, are limited as indicated by the part number of the device. The PLL configuration table is for guideline purposes only and does not imply that all PID9t-604e devices would be capable of attaining all of the frequency limits indicated.

Table 14. PLL Configurations and SYSCLK and CORE Frequencies, DD1.x-DD2.x

PLL_CFG (0:3)		Processor to Bus Frequency Ratio	VCO divider	Frequency Range Supported by VCO having an example range of VCO_{min}=275 to VCO_{max}=500 (MHz)			
				SYSCLK		Core	
bin	dec	(r)	(d)	Min= VCO_{min}/(r*d)	Max= VCO_{max}/(r*d)	Min= VCO_{min}/d	Max= VCO_{max}/d
0000	0	1x	2	138	250	138	250
0001	1	1x	4	69	125	69	125
0010	2	1x	8	35	62	35	62
0011	3	PLL Bypass	n/a	n/a	n/a	n/a	n/a
0100	4	2x	2	69	125	138	250
0101	5	2x	4	35	62	69	125
0110	6	2.5x	2	55	100	138	250
0111	7	2.5x	4	28	50	69	125
1000	8	3x	2	46	84	138	250
1001	9	3x	4	23	42	69	125
1010	10	4x	2	35	62	138	250
1011	11	5x	2	28	50		
1100	12	1.5x	2	92	166		
1101	13	6x	2	23	42		
1110	14	3.5x	2	40	72		
1111	15	Off	n/a	n/a	n/a	n/a	n/a

1.18 PLL Power Supply Filtering

The AVdd power signal is provided on the 604e to provide power to the clock generation phase-lock-loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in . The circuit should be placed as close as possible the AVdd pin to ensure that it filters out as much noise as possible.

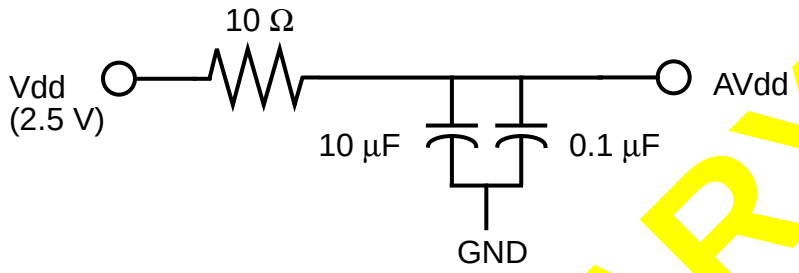


Figure 13. PLL Power Supply Filter Circuit

1.19 Decoupling Recommendations

Due to the PID9t-604e's large address and data buses and high operating frequencies, the processor can generate transient power surges and high frequency noise in its power supply. This is especially significant when driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the PID9t-604e itself requires a clean, tightly regulated source of power. Therefore it is strongly recommended that the system designer place at least one decoupling capacitor with a low ESR (effective series resistance) rating at each Vdd and OVdd pin of the PID9t-604e.

These capacitors should range in value from 220 pF to 10 µF to provide both high- and low- frequency filtering, and should be placed as close as possible to their associated VDD pin. Surface-mount tantalum or ceramic devices are preferred. It is also recommended that these decoupling capacitors receive their power from Vdd and Ground power planes in the PCB utilizing short traces and short or no via stubs to minimize the inductance in the traces. Power and ground connections must be made to all external Vdd and Ground pins of the PID9t-604e.

1.20 Connection Recommendations

To ensure reliable operation, it is recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be tied to Ground.

1.21 Thermal Management Information

The board designer can choose between several types of heat sinks to place on the PID9t-604e. There are several commercially available heat sinks designed especially for the PowerPC 604 family provided by the following vendors:

Thermalloy 214-243-4321
2021 W. Valley View Lane
P.O. Box 810839
Dallas, TX 75731

International Electronic Research Corporation(IERC)
135 W Magnolia Blvd. 818-842-7277
Burbank, CA 91502

Aavid Engineering 603-528-3400
One Kool Path
Laconic, NH 03247-0440

Wakefield Engineering 617-245-5900
60 Audubon Rd.
Wakefield, MA 01880

Ultimately, the final selection of an appropriate heat sink for the PID9t-604e system depends on many factors, including thermal performance at a given air velocity, spatial volume, attachment method, assembly, and cost. These vendors can provide assistance in system thermal solutions that lead to selection of appropriate heat sinks.

1.22 Ordering Information

This section provides the part numbering nomenclature for the PID9t-604e. In addition to processor frequency and bus divider, the part numbering scheme also consists of a part modifier and revision code. The modifier indicates enhancements in the device from the original production design. The revision codes refer to the die mask for identification purposes. Please contact your local IBM sales office for available combinations and assistance in selecting the correct part number.