PNX3000

Analog front end for digital video processors

Rev. 04 — 29 March 2005 Product data sheet

1. General description

The PNX3000 is an analog front end for digital video processors. It contains an IF circuit for both analog and digital broadcast signals, input selectors and Analog to Digital Converters (ADCs) for analog video and audio signals. The digital output signals are made available via three serial data links.

The IC has a supply voltage of 5 V. The supply voltage of the analog audio part can be 5 V or 8 V, depending on the maximum signal amplitudes that are required.

2. Features

- Multi-standard vision IF circuit with alignment-free PLL demodulator without external components
- Internal (switchable) time-constant for the IF-AGC circuit
- DTV IF circuit for gain control of digital broadcast TV signals
- Sound IF amplifier with separate AGC circuit for quasi-split sound
- IF circuit can also be used for intercarrier sound
- Analog demodulator for AM sound
- Integrated sound trap and group delay correction
- Video ident function detects the presence of a video signal
- Video source selector with four external CVBS or YC inputs and two analog CVBS outputs with independent source selection for each output
- Two linear inputs for $1f_H$ or $2f_H$ RGB signals with source selector; the RGB signals are converted to YUV before A to D conversion; both inputs can also be used as YPbPr input for DVD or set top box
- Integrated anti-alias filters for video ADCs
- Four 10-bit video ADCs for the conversion of CVBS, YC, YUV and down mixed sound IF signals
- Up to three different A to D converted video channels are available simultaneously (e.g. CVBS, YC and YUV)
- Audio source selector with five stereo inputs for analog audio and two microphone inputs
- Two microphone amplifiers with adjustable gain
- Three analog audio outputs for SCART and line out with independent source selection for each output
- Four 1-bit audio sigma delta ADCs for the conversion of audio and microphone signals

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- Three serial data link transmitters for interfacing with the digital video processor at a bit rate of 594 Mbit/s per data link
- Voltage to current converter for driving external east-west power amplifier
- I^2C-bus transceiver with selectable slave address and maskable interrupt output

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	main supply voltage			4.75	5.0	5.25	V
I_P	main supply current			-	285	320	mA
$V_{CC(1ASW)}$, $V_{CC(2ASW)}$	audio supply voltage		[1]	4.75	8.0	8.4	V
$I_{CC(ASW)}$	audio supply current		[1]	-	3.5	5.0	mA
Input signals							
$V_{i(VIF)(dif)(rms)}$	video IF amplifier sensitivity (RMS value)			-	75	150	µV
$V_{i(DTVIF)(dif)(rms)}$	DTV IF amplifier sensitivity (RMS value)	f_i between 30 MHz and 60 MHz		-	75	150	µV
$V_{i(SIF)(rms)}$	sound IF amplifier sensitivity (RMS value)	–3 dB		-	45	-	µV
$V_{i(CVBS/Y)(p-p)}$	external Y/CVBS input (peak-to-peak value)			-	1.0	1.76	V
$V_{i(RGB)(b-w)}$	RGB inputs (black-to-white value)		[2]	-	0.7	1.0	V
$V_{i(Y)(p-p)}$	luminance input signal (peak-to-peak value)	top sync-to-white	[2]	-	1.0	1.43	V
$V_{i(Pb)(p-p)}$	Pb input signal (peak-to-peak value)	100 % color bar	[2]	-	0.7	1.0	V
$V_{i(Pr)(p-p)}$	Pr input signal (peak-to-peak value)	100 % color bar	[2]	-	0.7	1.0	V
Video A to D converters							
$B_{v(-3dB)}$	–3 dB signal bandwidth	$1f_H$ mode		-	9	-	MHz
f_{sample}	sample frequency	$1f_H$ mode		-	27	-	MHz
RES	resolution			-	10	-	bit
Analog output signals							
$V_{o(CVBS)(p-p)}$	analog CVBS output signals (peak-to-peak value)	at input signal of 1.0 V (p-p)		-	2.0	-	V
$I_{o(TUNERAGC)}$	tuner AGC output current pin TUNERAGC			1	-	-	mA

[1] The supply voltage for the analog audio part of the IC can be 5 V or 8 V. For a supply voltage of 5 V the maximum signal amplitudes at in- and outputs are 1 V (RMS). For a supply voltage of 8 V the maximum amplitudes are 2 V (RMS).

[2] The RGB inputs can also be used as YPbPr input. The selection is made via the I^2C-bus. The YPbPr input sensitivity is in accordance with the DVD player specification.

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PNX3000HL/N3	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

5. Block diagram

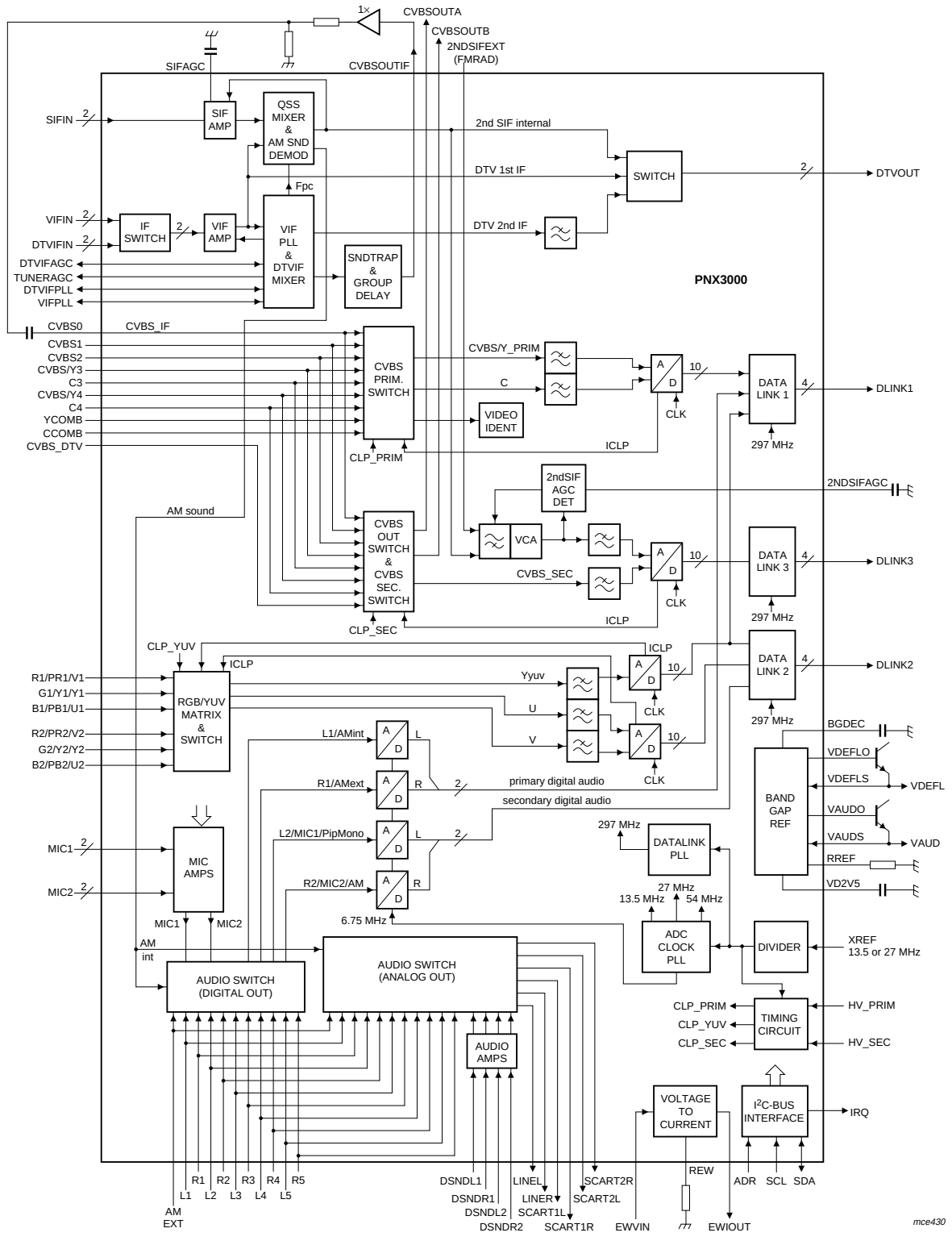


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

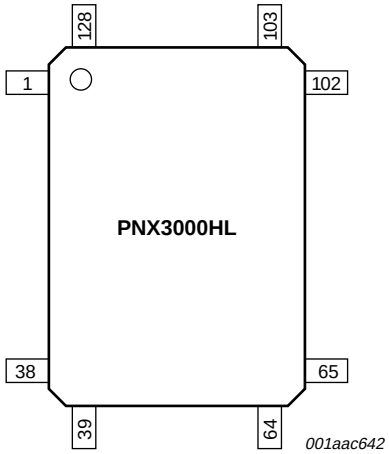


Fig 2. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
CVBS2	1	CVBS2 input
VAUDO	2	DC output voltage for supply of audio DACs in digital decoder
VAUDS	3	sense voltage input for audio DACs supply
CVBS/Y3	4	external CVBS/Y3 input
C3	5	external CHROMA3 input
GND(VSW)	6	ground video switch
BGDEC	7	band gap decoupling
CVBS/Y4	8	external CVBS/Y4 input
C4	9	external CHROMA4 input
FUSE	10	fused lead
GND(FILT)	11	ground filters
CVBS_DTV	12	input for CVBS encoded signal from DTV decoder
RREF	13	reference current input
$V_{CC(FILT)}$	14	supply voltage filters (5 V)
YCOMB	15	Y signal input from 3D comb filter
CCOMB	16	C signal input from 3D comb filter
AMEXT	17	external AM mono input
TESTPIN3	18	test pin 3; leave open
CVBSOUTA	19	CVBS or Y+CHROMA output A
VDEFLO	20	DC output voltage for supply of deflection DACs in digital decoder
VDEFLS	21	sense voltage for deflection DACs supply

Table 3: Pin description *...continued*

Symbol	Pin	Description
CVBSOUTB	22	CVBS or Y+CHROMA output B
FUSE	23	fused lead
TESTPIN2	24	test pin 2; connect to ground
R1/PR1/V1	25	R input 1 of RGB signal, Pr input 1 of YPbPr signal or V input 1 of YUV signal
G1/Y1/Y1	26	G input 1 of RGB signal, Y input 1 of YPbPr signal or Y input 1 of YUV signal
B1/PB1/U1	27	B input 1 of RGB signal, Pb input 1 of YPbPr signal or U input 1 of YUV signal
$V_{CC(RGB)}$	28	supply voltage RGB matrix (5 V)
GND(RGB)	29	ground RGB matrix
R2/PR2/V2	30	R input 2 of RGB signal, Pr input 2 of YPbPr signal or V input 2 of YUV signal
G2/Y2/Y2	31	G input 2 of RGB signal, Y input 2 of YPbPr signal or Y input 2 of YUV signal
B2/PB2/U2	32	B input 2 of RGB signal, Pb input 2 of YPbPr signal or U input 2 of YUV signal
FUSE	33	fused lead
GND(VADC)	34	ground video ADCs
$V_{CC(VADC)}$	35	supply voltage video ADCs (5 V)
EWVIN	36	east-west input voltage
EWIOUT	37	east-west output current
REW	38	east-west voltage to current conversion resistor
ADR	39	I^2C-bus address selection
XREF	40	XTAL reference frequency input
FUSE	41	fused lead
IRQ	42	interrupt request output
SDA	43	I^2C-bus serial data input and output
SCL	44	I^2C-bus serial clock input
HV_SEC	45	horizontal and vertical sync input for secondary video channel
HV_PRIM	46	horizontal and vertical sync input for primary video channel
VD2V5	47	decoupling of internal digital supply voltage
GND(DIG)	48	digital ground
$V_{CC(DIG)}$	49	digital supply voltage (5 V)
STROBE3N	50	strobe negative data link 3
STROBE3P	51	strobe positive data link 3
DATA3N	52	data negative data link 3
DATA3P	53	data positive data link 3
FUSE	54	fused lead
STROBE2N	55	strobe negative data link 2
STROBE2P	56	strobe positive data link 2
DATA2N	57	data negative data link 2

Table 3: Pin description *...continued*

Symbol	Pin	Description
DATA2P	58	data positive data link 2
GND(I2D)	59	ground data links
STROBE1N	60	strobe negative data link 1
STROBE1P	61	strobe positive data link 1
DATA1N	62	data negative data link 1
DATA1P	63	data positive data link 1
$V_{CC(I2D)}$	64	supply voltage data links (5 V)
SCART2R	65	audio output for SCART 2 right
SCART2L	66	audio output for SCART 2 left
LINER	67	audio line output right
LINEL	68	audio line output left
SCART1R	69	audio output for SCART1 right
SCART1L	70	audio output for SCART1 left
FUSE	71	fused lead
DSNDR2	72	audio signal from digital decoder right 2
DSNDL2	73	audio signal from digital decoder left 2
DSNDR1	74	audio signal from digital decoder right 1
DSNDL1	75	audio signal from digital decoder left 1
GND(AADC)	76	ground audio ADCs
$V_{CC(AADC)}$	77	supply voltage audio ADCs (5 V)
FUSE	78	fused lead
R4	79	right input audio 4
L4	80	left input audio 4
R3	81	right input audio 3
L3	82	left input audio 3
R2	83	right input audio 2
L2	84	left input audio 2
R1	85	right input audio 1
L1	86	left input audio 1
GND(2ASW)	87	ground 2 audio switch
$V_{CC(2ASW)}$	88	supply voltage 2 audio switch (audio output buffers; 5 V or 8 V)
VAADCREF	89	decoupling of reference voltage for audio ADCs
VAADCN	90	0 V reference voltage for audio ADCs (GND)
VAADCP	91	full scale reference voltage for audio ADCs (5 V)
MIC2N	92	microphone input 2 negative
MIC2P	93	microphone input 2 positive
MIC1N	94	microphone input 1 negative
MIC1P	95	microphone input 1 positive
FUSE	96	fused lead
GND(1ASW)	97	ground 1 audio switch
$V_{CC(1ASW)}$	98	supply voltage 1 audio switch (audio input buffers; 5 V or 8 V)

Table 3: Pin description *...continued*

Symbol	Pin	Description
SIFINP	99	sound IF input positive
SIFINN	100	sound IF input negative
SIFAGC	101	control voltage for sound IF AGC
DTVIFAGC	102	control voltage for DTV IF AGC
DTVIFINP	103	DTV IF input positive
DTVIFINN	104	DTV IF input negative
TUNERAGC	105	tuner AGC output
FUSE	106	fused lead
VIFINP	107	vision IF input positive
VIFINN	108	vision IF input negative
DTVIFPLL	109	output loop filter DTVIF PLL demodulator
$V_{CC(IF)}$	110	supply voltage IF circuit (5 V)
VIFPLL	111	output loop filter VIF PLL demodulator
GND(1IF)	112	ground 1 IF circuit
2NDSIFEXT	113	second sound IF input
2NDSIFAGC	114	second sound IF AGC capacitor
GND(2IF)	115	ground 2 IF circuit
DTVOUTP	116	DTV output positive
DTVOUTN	117	DTV output negative
$V_{CC(SUP)}$	118	supply voltage of supply circuit (5 V)
FUSE	119	fused lead
CVBSOUTIF	120	CVBS output of IF circuit
GND(SUP)	121	ground of supply circuit
$V_{CC(1VSW)}$	122	supply voltage 1 of video switch (5 V)
CVBS0	123	CVBS0 input for CVBS from IF part
TESTPIN1	124	test pin 1; connect to ground
$V_{CC(2VSW)}$	125	supply voltage 2 of video switch (5 V)
CVBS1	126	CVBS1 input
R5	127	right input audio 5
L5	128	left input audio 5

7. Functional description

7.1 Vision IF

The IF amplifier contains 3 AC-coupled control stages which have a total gain control range of more than 66 dB.

The video signal is demodulated by means of an alignment-free PLL carrier regenerator with an internal VCO. This VCO is calibrated by means of a digital control circuit which uses the external crystal frequency as a reference. The frequency setting for the various

standards (33.4 MHz, 33.9 MHz, 38 MHz, 38.9 MHz, 45.75 MHz and 58.75 MHz) is realized via the I^2C-bus. To improve performance for phase modulated carrier signals the control speed of the PLL can be increased by setting bit FFI.

The AFC output is generated by the digital control circuit of the IF PLL demodulator and can be read via the I^2C-bus. For fast search tuning systems the window of the AFC can be increased with a factor of three with bus bit AFW.

The AGC-detector operates on top sync or top white level. The demodulation polarity is switched via the I^2C-bus. The AGC detector capacitor is integrated. The time-constant can be chosen via I^2C-bus bits AGC1 and AGC0. The AGC has also an external mode which is activated by bit AGCM. In this mode the IF gain is determined by an external voltage on pin DTVIFAGC.

The IC has an integrated sound trap filter. The filter is constructed as a cascade of three separate traps, to realize sufficient suppression of the first and second sound carriers. The trap frequencies are selected via the I^2C-bus.

The IC has an integrated group delay correction filter. The filter can be switched between the PAL BG curve and a flat group delay response characteristic. This has the advantage that in multi-standard receivers the video SAW filter does not need to be switchable.

7.2 DTV IF

Apart from processing analog TV signals, the IF circuit can also be used to preprocess digital TV signals before they are sent to a DTV channel decoder. For this application the two modes of operation are DTV 1st IF and DTV 2nd IF. For both operating modes the IF PLL must be set to synthesizer mode.

In DTV 1st IF mode only the AGC function of the IF circuit is used, so the DTV channel decoder must be able to handle the 1st IF frequency. Because the AGC detector operates on the down-mixed 2nd IF signal, it is still important to program a valid frequency for the IF VCO. It is recommended to set the frequency of the VCO to a value that is approximately 4 MHz higher than the incoming 1st IF center frequency.

In DTV 2nd IF mode the 2nd IF signal is obtained by down-mixing the incoming DTV IF signal with the IF VCO signal. The low-pass filtered DTV 2nd IF signal is available as a differential signal at the DTV output. This signal may have a maximum bandwidth of 10 MHz. The VCO frequency is programmed via the I^2C-bus in steps of 250 kHz.

In DTV mode the AGC time constant is determined by a capacitor on pin DTVIFAGC. There are two AGC modes: internal and external. In the internal AGC mode the gain is controlled by an internal AGC detector. The external AGC mode is activated by bit AGCM. In this mode the appropriate AGC pin is used as input, so that the IF gain can be controlled by the DTV channel decoder.

The IF PLL has two pins for connection of the PLL loop filters, one for analog TV and one for DTV. This allows each loop filter to be optimized for its application.

7.3 Sound IF

The PNX3000 has a separate sound IF input to enable quasi-split sound applications. The sound IF amplifier is similar to the vision IF amplifier and has a gain control range of about 55 dB. The AGC detector measures the average level of the AM or FM SIF carrier and ensures a constant signal amplitude for the AM demodulator and Quasi-Split Sound (QSS) mixer.

The single reference QSS mixer is realized by a multiplier. In this multiplier the SIF signal is converted to the intercarrier frequency by mixing it with the regenerated picture carrier from the video IF VCO. With this system a high performance stereo sound processing can be achieved.

For applications without a SIF SAW filter the IC can also be used in intercarrier mode. In this mode the composite video signal from the VIF amplifier is fed to the QSS mixer and converted to the intercarrier frequency.

AM sound demodulation is realized in the analog domain by the QSS mixer. The modulated SIF signal is multiplied in phase with the limited SIF signal. The demodulator output signal is low-pass filtered for suppression of the carrier harmonics. The demodulated AM signal can be digitized by one of the audio ADCs.

The QSS mixer can also be used for down-mixing an FM radio IF signal to an intercarrier frequency, so that it can be demodulated by the digital decoder. The IF PLL must be set to synthesizer mode in this case. The preferred solution is to supply the FM radio signal via a separate SAW or ceramic filter to the DTV input of the PNX3000. The reason is that the selectivity of a SAW filter for TV sound is not sufficient for FM radio and, if the SIF input is used, no tuner AGC information is available.

For high performance FM radio it is recommended that a 10.7 MHz FM radio IF signal is supplied to the external 2nd SIF input. In this case the IF signal must be filtered by an external bandpass filter, that also functions as an anti-alias filter. The low-pass filter before the 2nd SIF ADC must be bypassed by setting bus bit SLPM.

The IC includes a separate AGC circuit for the 2nd SIF signal. This AGC is needed for intercarrier sound applications and when an external sound IF signal is supplied to the 2nd SIF input. The AGC amplifier is preceded by a second order high-pass filter for suppression of video signal components. The AGC time constant is determined by an external capacitor.

7.4 CVBS/YC source selector

The video input selector consists of four independent source selectors, that can select between the CVBS signal coming from the IF part and four external CVBS signals. Two of the external CVBS inputs can also be used as YC input. One selector is used to select the signal for of the primary video channel. A second selector selects the CVBS or YC signal for the secondary channel. The third and fourth selectors are used to select analog outputs CVBS A and B, which can be used for SCART or line output.

The primary channel can be a CVBS or YC signal. If a YC signal is selected for the secondary channel or for the external CVBS outputs A or B, the luminance and chrominance signals are added to obtain a CVBS signal.

The IC has an extra YC input for connection of a 3D comb filter. The comb signal can only be selected for the primary video channel. The input pin CVBS_DTV allows an analog CVBS signal derived from a digital broadcast (MPEG) signal to be recorded with an analog VCR. This signal cannot be selected for the primary video channel.

The video identification circuit detects the presence of a video signal on the CVBS_IF input (pin CVBS0). The identification output is normally used to detect transmitters during search tuning and can be read via the I^2C-bus. The circuit can also be used to monitor the selected primary CVBS or YC signal. Either mode is selected by bit VIM.

7.5 RGB/YPbPr source selector

The IC has two RGB inputs. Both inputs can also be used as YPbPr input for connecting video sources with an YPbPr output like a DVD player. The RGB inputs can also be used for fast insertion of RGB signals (for instance on screen display menus) in the primary CVBS signal. The fast insertion switch is located in the digital video processor.

The RGB signals are converted to YUV before further processing. The YUV output signal is digitized by two ADCs. The U and V components have half the bandwidth of the Y signal, therefore the U and V signals are multiplexed and digitized by one ADC.

7.6 Video A to D converters and anti-alias filters

The PNX3000 contains four video ADCs for analog and digital video broadcast signals. The clock frequency for the ADCs is either 27 MHz or 54 MHz. Two analog signals can be multiplexed at the input of one ADC. Then the clock frequency of the ADC is 54 MHz and the sample frequency of each channel is 27 MHz.

The video ADCs are 10-bit folding ADCs. The sample frequency for standard $1f_H$ video signals is 27 MHz. For the YUV channel the sample frequency of the U and V components is half the sample frequency of the Y signal.

For $2f_H$ YPbPr or RGB input signals (for instance 480p or 1080i ATSC signals), the frequency that is used to sample the YUV signals is twice as high as for $1f_H$ signals. The sample frequency is 54 MHz for Y and 27 MHz for U and V. The high sample frequency requires two data links to transport the video data to the digital video processor.

The anti-alias filters before the ADCs limit the signal bandwidth to prevent aliasing effects. The filters for YUV can be bypassed by means of two separate bits: bit BPY for the Y filter and bit BPUV for the U and V filters. This enables the use of external anti-alias filters with increased bandwidth for $2f_H$, RGB or YPbPr input signals.

Table 4 shows the signal bandwidths and sample rates for the various types of video signals. Table 5 shows which video signals are sent to the digital video processor for both data link modes.

Table 4: Overview of anti-alias filter bandwidths and video signal sample rates

Signal type	Signal component	Signal band –1.0 dB (MHz)	Signal band –3.0 dB (MHz)	Sample frequency (MHz)
CVBS	-	8	9	27
YC	Y	8	9	27
	C	8	9	27
YUV $1f_H$	Y	8	9	27
	U	4	4.5	13.5
	V	4	4.5	13.5
YUV $2f_H$	Y	16	18	54
	U	8	9	27
	V	8	9	27
DTV	-	10	12	-
2nd SIF	-	8	9	27

7.7 Audio source selectors and A to D converters

The PNX3000 contains two different audio source selectors. The first selector selects which audio signals are routed to the audio ADCs for further processing in the digital domain. The two microphone inputs are also connected to this selector. The selector has two outputs, a primary channel and a secondary channel. The primary audio channel is used for one stereo signal. The secondary audio channel can carry a second stereo signal, or two microphone signals, or one mono signal and one microphone signal or one mono signal and one AM sound signal.

The second selector selects which audio signals are fed to the analog audio outputs for SCART and line out. This selector also has two stereo inputs for demodulated sound signals coming from the digital video processor.

The gain from an external audio input to an analog output is 1. A supply voltage of 5 V allows input and output amplitudes of 1 V (RMS) full scale. The PNX3000 has separate supply voltage pins for the audio selector circuit. To allow for input and output amplitudes of 2 V (RMS) full scale, as required for compliance with the SCART specification, an audio supply voltage of 8 V must be used.

The audio ADCs are 1-bit sigma-delta converters that operate at a clock frequency of 6.75 MHz. The audio A to D clock is synchronous with the video A to D clock, so that audio and video data can be sent over the same data links. The effective audio sample rate is $\frac{f_{clk}}{128} = 52.7$ ksample/s.

7.8 Microphone inputs

The IC has two microphone inputs. One microphone input can be used for voice control of the TV set with the help of an intelligent voice command decoder. The second input can be used for connection of a microphone for Karaoke.

To allow the use of microphones with different sensitivities the gain of each microphone amplifier is switchable between two values via the I^2C-bus.

7.9 Clock generation, timing circuitry and black level clamping

The IC contains two PLL circuits that derive the sample clock for the ADCs and the bit and word clocks for the data links from an external reference frequency. The reference frequency must be a stable frequency of either 13.5 MHz or 27 MHz from a crystal oscillator. The internal reference frequency is always 13.5 MHz. If the external frequency is 27 MHz a prescaler must be activated by bus bit FXT.

One PLL is used to multiply the 13.5 MHz reference frequency to the 27 MHz and 54 MHz clock frequencies that are needed for the video ADCs. A second PLL is used to obtain the 297 MHz bit clock for the data link transmitters.

A special timing circuit is used to generate the horizontal and vertical timing pulses that are needed in the IF part, and also for clamping the black level of the selected video signals to a defined value at the output of the video ADCs. The horizontal and vertical timing information of the primary and secondary video channels must be supplied by the digital video processor on pins HV_PRIM and HV_SEC. The signal on these pins must consist of a horizontal timing pulse that starts just before and ends just after the horizontal sync pulse of the selected video signal. To enable detection of the vertical blanking period, the horizontal pulses must be wider during a number of lines in the vertical blanking interval.

The clamp signal inside the IC is generated with the help of the external horizontal timing pulse and the 13.5 MHz clock. The vertical timing information is used to disable the black level clamp, so that the black level is not disturbed by the vertical sync pulse on the video signal. The clamp pulse for the YUV channel can be derived from the primary or the secondary HV pulse, and is selected by bus bit CLPS.

To avoid signal disturbance, it is possible to disable the black clamps when the horizontal PLL in the digital video processor is not locked to the selected video signal. This is done by bus bit CMP for the primary CVBS channel and bus bit CMS for the secondary CVBS channel.

Special attention is required when the same CVBS input is selected for primary and secondary CVBS channels. In this case the black level clamp loop is only closed for the primary CVBS input. Due to internal offsets this will normally result in a deviation on the black level of the digitized secondary CVBS output.

7.10 Data link transmitters

Three serial data links are used for transportation of the digital video and audio data coming from the ADCs in the PNX3000 to the digital video processor. The use of serial data connections results in a considerable reduction in pin count and the number of connection wires that are needed between both ICs.

The communication between data link transmitter and data link receiver consists of two signals, a data signal and a strobe signal. The two signals together contain the data, bit-sync and word-sync information. For optimal EMC performance both data and strobe are low voltage differential signals. The voltage swing on each wire is 300 mV.

Each data word sent over a data link consists of 44 bits: 4 video samples of 10 bits each, 2 audio bits and 2 word-sync bits. The word clock is 13.5 MHz. The data rate on each of the three data links is 594 Mbit/s. Table 5 shows which video signals are sent to the digital

video processor for both data link modes. In the standard mode up to three video channels plus one sound IF signal are digitized and transferred simultaneously over the data links.

The distance between both ICs that are connected via the data link must not be larger than about 10 centimeters. The two wires for each differential signal should be paired in the layout of the printed-circuit board.

7.11 I²C-bus transceiver

The slave address of the I²C-bus transceiver in the PNX3000 has two possible values, selected via the ADR pin. The maximum bus clock frequency is 400 kHz, and the voltage swing of SCL and SDA can be 3.3 V or 5 V. The I²C-bus transceiver also has a hardwired IRQ output (open drain and LOW-active) for interruption of the microprocessor when the value of an important status bit in status byte 0 changes. The IRQ signal is maskable with register 0Fh.

7.12 Power supply circuit

An internal band gap circuit generates a stable voltage of 1.25 V. This voltage is multiplied to a reference voltage of 2.3 V, and a digital supply voltage of 2.5 V. These two voltages must be decoupled by external capacitors. A $\frac{1}{2}V_P$ reference voltage for the audio ADCs also requires an external decoupling capacitor. The PNX3000 contains two voltage regulators to supply the SDACs that are used in the digital video processor. Each regulator requires a few external components (one transistor, two resistors and a decoupling capacitor). The output voltage is adjustable between 1.25 V and 3.3 V by selection of external resistors values.

7.13 East-west interface

The PNX3000 contains a voltage to current converter that serves as the interface between the voltage output of the digital video processor and the current input of the east-west stage of the vertical deflection amplifier (TDA8358). The transconductance is determined by the value of an external resistor.

Table 5: Overview of data link modes

Mode	Application	Data link 1				Data link 2				Data link 3			
		Video1		Audio1		Video2		Audio2		Video3		Test	
0	standard	$CVBS/Y_{prim}$	C	L1	R1	Y_{yuv}	U,V	L2	R2	$CVBS_{sec}$	2nd SIF	HV_P	HV_S
1	YUV $2f_H$ input	Y_{yuv}		L1	R1	U	V	L2	R2	$CVBS_{sec}$	2nd SIF	HV_P	HV_S

8. I²C-bus specification

The slave addresses of the IC are given in Table 6. The circuit operates at clock frequencies of up to 400 kHz.

Table 6: Slave addresses (9Ah or 9Eh)

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	1	1	A1	1	1/0

Bit A1 is controlled via the ADR pin, when the pin is connected to ground it is a 0 and when connected to the positive supply line it is a 1. When this pin is left open it is connected to ground via an internal resistor.

8.1 Input control bits

Table 7: Input control registers

Valid subaddresses: 00h to 0Fh; auto-increment mode available for subaddresses.

Function	Sub addr (hex)	Data byte								POR value (hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
Vision IF 0	00	AFN	AFW	IFS	AGCM	FFI	PMOD	AGC1	AGC0	00
Vision IF 1	01	IFON	DSIF	DFIF	DTV	IFLH	SYNT	SSIF	QSS	00
IF PLL offset	02	IFGT	VAI	IFO5	IFO4	IFO3	IFO2	IFO1	IFO0	20
IF tuner take-over	03	VA1	VA0	TTO5	TTO4	TTO3	TTO2	TTO1	TTO0	20
IF PLL frequency	04	FXT	IFA	IFB	IFC	0	0	0	0	80
IF synthesizer frequency	05	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0	00
Filters	06	BPUV	BPY	BPP	GD	SLPM	BPS	ST1	ST0	00
Data link mode	07	DRND	0	0	HDTV	0	0	0	DM	00
Video switches 0	08	SEC3	SEC2	SEC1	SEC0	PRI3	PRI2	PRI1	PRI0	00
Video switches 1	09	VIM	VSW	CMS	CMP	CVA3	CVA2	CVA1	CVA0	36
Video switches 2 and audio mute	0A	0	MA2	MA1	MA0	CVB3	CVB2	CVB1	CVB0	76
RGB switches	0B	0	RSEL	MAT	DVD	0	0	CMR	CLPS	02
Audio switches ADC	0C	MONO	SEA2	SEA1	SEA0	MNM1	PRA2	PRA1	PRA0	00
Audio switches 0	0D	DSG	A1S2	A1S1	A1S0	MNM0	A0S2	A0S1	A0S0	00
Audio switches 1	0E	0	M2G	AMX	M1G	MICON	A2S2	A2S1	A2S0	00
IRQ mask status byte 0	0F	1 [1]	IM6	IM5	IM4	IM3	IM2	IM1	IM0	80

[1] The value of this bit cannot be changed.

Table 8: AFC switch

AFN	Mode
0	normal operation
1	AFC not active

Table 9: AFC window

AFW	AFC window
0	normal
1	enlarged

Table 10: IF sensitivity

IFS	IF sensitivity
0	normal
1	reduced

Table 11: Internal or external AGC mode

AGCM	Mode
0	internal
1	external

Table 12: Fast filter IF-PLL

FFI	Condition
0	normal time constant
1	increased time constant

Table 13: Video modulation standard

PMOD	Condition
0	negative modulation (FM sound)
1	positive modulation (AM sound)

Table 14: IF AGC speed

AGC1	AGC0	AGC speed
0	0	0.7 × norm
0	1	norm
1	0	3 × norm
1	1	6 × norm

Table 15: IF amplifier on/off

IFON	Mode
0	IF amplifier not active
1	normal operation

Table 16: Selection of signal on analog DTV output

DSIF	DFIF	Mode	LPF active
0	0	DTV second IF	Y
0	1	DTV first IF	N
1	0	2nd SIF internal	N
1	1	spare	N/A

Table 17: Vision IF input select

DTV	Mode
0	VIF input
1	DTVIF input

Table 18: Calibration of IF PLL demodulator

IFLH	Mode
0	calibration system active
1	calibration system not active

Table 19: IF PLL mode

SYNT	Mode
0	normal mode
1	synthesizer mode

Table 20: Second sound IF input

SSIF	Mode
0	internal input
1	external input

Table 21: Sound operation

QSS	Mode
0	intercarrier sound
1	quasi split sound

Table 22: IF AGC operation mode

IFGT	Mode
0	non gated operation
1	gated operation [1]

[1] Gated operation gives improved weak signal performance. Gated operation is automatically disabled if CVBS_IF is not selected as primary or secondary video signal. In this situation bit IFLH should be set to 1 to avoid recalibration of the IF VCO for white video patterns.

Table 23: CVBS IF output signal amplitude correction for system I

VAI	Output signal amplitude	
	PMOD = 0	PMOD = 1
0	no correction	no correction
1	amplitude +8 %	amplitude –8 %

Table 24: IF PLL offset adjustment

IFO5 to IFO0 (hex)	Control
00	negative correction
20	no correction
3F	positive correction

Table 25: CVBS IF output signal amplitude

VA1	VA0	Output signal amplitude	
		Negative modulation, PMOD = 0	Positive modulation, PMOD = 1
0	0	no correction	no correction
0	1	spare	spare
1	0	amplitude –5 %	amplitude +5 %
1	1	amplitude +5 %	amplitude –5 %

Table 26: IF AGC tuner take over

TTO5 to TTO0 (hex)	Control
3F	tuner take over at IF input signal of 0.4 mV
00	tuner take over at IF input signal of 80 mV

Table 27: External reference frequency

FXT	Condition
0	13.5 MHz
1	27 MHz

Table 28: PLL demodulator frequency setting

IFA	IFB	IFC	IF frequency
0	0	0	58.75 MHz
0	0	1	45.75 MHz
0	1	0	38.90 MHz
0	1	1	38.00 MHz
1	0	0	33.40 MHz
1	1	0	33.90 MHz

Table 29: IF VCO synthesizer frequency (SF7 to SF0) [1]

SF7 to SF0 (Decimal number)	Frequency
95	f = 24 MHz
255	f = 64 MHz

[1] $f_{synth} = (N + 1) \times 250$ kHz; where $95 \leq N \leq 255$.

Table 30: Bypass UV anti-alias filters

BPUV	Mode
0	normal operation
1	UV anti-alias filters bypass

Table 31: Bypass Y_{yuv} anti-alias filter

BPY	Mode
0	normal operation
1	Y_{yuv} anti-alias filter bypass

Table 32: Bypass anti-alias filters of primary CVBS

BPP	Mode
0	normal operation
1	primary CVBS anti-alias filters bypass

Table 33: Group delay correction

GD	Mode
0	group delay correction bypass
1	group delay correction active

Table 34: 2nd SIF LPF mode

SLPM	Mode
0	2nd SIF LPF active
1	2nd SIF LPF bypass (for FM radio 10.7)

Table 35: Bypass anti-alias filters of secondary CVBS

BPS	Mode
0	normal operation
1	secondary CVBS anti-alias filters bypass

Table 36: Sound trap frequency

ST1	ST0	Frequency
0	0	5.5 MHz
0	1	4.5 MHz
1	0	6.0 MHz
1	1	6.5 MHz

Table 37: Data link transmitter test mode

DRND	Mode
0	normal operation
1	pseudo random test mode [1]

[1] The pseudo random mode can be used for in-circuit testing of the data link connections between data link transmitter in the analog front end IC and data link receiver in the digital video processor IC.

Table 38: YUV $2f_H$ clamp pulse timing

HDTV	mode
0	normal timing (480p signal)
1	HDTV timing (1080i signal)

Table 39: Data link modes [1]

DM	Application	Mode
0	Normal	0
1	YUV $2f_H$	1

[1] See Table 5 in Section 7.1.

Table 40: Selection of secondary video signal

SEC3	SEC2	SEC1	SEC0	Selected signal
0	0	0	0	CVBS_IF
0	0	0	1	CVBS1
0	0	1	0	CVBS2
0	0	1	1	CVBS3
1	0	1	1	Y + C3
0	1	0	0	CVBS4
1	1	0	0	Y + C4
0	1	0	1	CVBS_DTV
other				CVBS_IF

Table 41: Selection of primary video channel

PRI3	PRI2	PRI1	PRI0	Selected signal
0	0	0	0	CVBS_IF
0	0	0	1	CVBS1
0	0	1	0	CVBS2
0	0	1	1	CVBS3
1	0	1	1	Y + C3
0	1	0	0	CVBS4
1	1	0	0	Y + C4
1	1	1	0	YC_COMB
other				CVBS_IF

Table 42: Video ident mode

VIM	Mode
0	ident coupled to CVBS_IF
1	ident coupled to selected primary CVBS signal

Table 43: IF video mute

VSW	Mode
0	normal operation
1	CVBSOUTIF muted

Table 44: Clamp mode primary CVBS channel

CMS	Mode
0	top sync clamping mode
1	black level clamping mode

Table 45: Clamp mode primary CVBS channel

CMP	Mode
0	top sync clamping mode
1	black level clamping mode

Table 46: Selection of CVBS output A

CVA3	CVA2	CVA1	CVA0	Selected signal
0	0	0	0	CVBS_IF
0	0	0	1	CVBS1
0	0	1	0	CVBS2
0	0	1	1	CVBS3
1	0	1	1	Y + C3
0	1	0	0	CVBS4
1	1	0	0	Y + C4
0	1	0	1	CVBS_DTV
other				output muted

Table 47: Mute SCART2 audio output

MA2	Mode
0	normal operation
1	SCART2 audio output muted

Table 48: Mute SCART1 audio output

MA1	Mode
0	normal operation
1	SCART1 audio output muted

Table 49: Mute LINE audio output

MA0	Mode
0	normal operation
1	LINE audio output muted

Table 50: Selection of CVBS output B

CVB3	CVB2	CVB1	CVB0	Selected signal
0	0	0	0	CVBS_IF
0	0	0	1	CVBS1
0	0	1	0	CVBS2
0	0	1	1	CVBS3
1	0	1	1	Y + C3
0	1	0	0	CVBS4
1	1	0	0	Y + C4
0	1	0	1	CVBS_DTV
other				output muted

Table 51: Selection of RGB/YUV input

RSEL	Selected Signal
0	RGB1 input
1	RGB2 input

Table 52: RGB/YUV input mode

MAT	DVD	Mode
0	0	YUV input [1]
0	1	YPbPr input [2]
1	0	RGB input [3]
1	1	spare

[1] YUV input is an Y, –(B–Y) and –(R–Y) input with the specification:
a) Y = 1.43 V (p-p); U = 1.33 V (p-p); V = 1.05 V (p-p)
b) These signal amplitudes are based on a color bar signal with 75 % saturation

[2] YPbPr input with the specification:
a) Y = 1.0 V (p-p); Pb = 0.7 V (p-p); Pr = 0.7 V (p-p)
b) These signal amplitudes are based on a color bar signal with 100 % saturation

[3] RGB input with the specification:
a) $R = 0.7 \times V_{B-W}$; $G = 0.7 \times V_{B-W}$; $B = 0.7 \times V_{B-W}$
b) These signal amplitudes are based on a color bar signal with 100 % saturation

Table 53: Clamp mode for RGB and YUV signals

CMR	Mode
0	top sync clamp mode
1	black level clamp mode

Table 54: Clamp pulse selection for RGB and YUV signals

CLPS	Mode
0	clamp pulse of primary channel
1	clamp pulse of secondary channel

Table 55: Selection of secondary audio channel

SEA2	SEA1	SEA0	Selected signal
0	0	0	AMint (L) and AMext (R) [1]
0	0	1	L1 and R1
0	1	0	L2 and R2
0	1	1	L3 and R3
1	0	0	L4 and R4
1	0	1	L5 and R5
1	1	0	MIC1 (L) and MIC2 (R)
1	1	1	AMext (L) and AMint (R) [1]

[1] Selection between AMint and AMext must be done by digital video processor.

Table 56: Secondary audio channel mode

Mono	MNM1	MNM0	Mode
0	-	-	stereo; see Table 55
1	0	0	mono (L) and AMint (R) [1]
1	0	1	mono (L) and AMext (R) [1]
1	1	0	mono (L) and MIC1 (R) [1]
1	1	1	mono (L) and MIC2 (R) [1]

[1] Mono is (L + R)/2; when AM is selected in Table 55, mono is AMint for SEA[2:0] = 000 and AMext for SEA[2:0] = 111. A more comprehensive table can be found in the application note.

Table 57: Selection of primary audio channel

PRA2	PRA1	PRA0	Selected signal
0	0	0	AMint (L) and AMext (R) [1]
0	0	1	L1 and R1
0	1	0	L2 and R2
0	1	1	L3 and R3
1	0	0	L4 and R4
1	0	1	L5 and R5
1	1	1	AMext (L) and AMint (R) [1]

[1] Selection between AMint and AMext must be done by digital video processor.

Table 58: Gain from DSND inputs to SCART outputs

DSG	Gain
0	0 dB; to be used with 5 V audio supply
1	6 dB; to be used with 8 V audio supply

Table 59: Selection of SCART1 audio output

AMX	A1S2	A1S1	A1S0	Selected signal
0	0	0	0	AMint
0	0	0	1	LR1
0	0	1	0	LR2
0	0	1	1	LR3
0	1	0	0	LR4
0	1	0	1	LR5
0	1	1	0	DSND1
0	1	1	1	DSND2
1	0	0	0	AMext

Table 60: Selection of LINE audio output

AMX	A0S2	A0S1	A0S0	Selected signal
0	0	0	0	AMint
0	0	0	1	LR1
0	0	1	0	LR2
0	0	1	1	LR3
0	1	0	0	LR4
0	1	0	1	LR5
0	1	1	0	DSND1
0	1	1	1	DSND2
1	0	0	0	AMext

Table 61: Microphone input 2 gain

M2G	Gain
0	low
1	high

Table 62: Microphone input 1 gain

M1G	Gain
0	low
1	high

Table 63: Microphone amplifiers on/off

MICON	Mode
0	microphone amplifiers not active
1	normal operation

Table 64: Selection of SCART2 audio output

AMX	A2S2	A2S1	A2S0	Selected signal
0	0	0	0	AMint
0	0	0	1	LR1
0	0	1	0	LR2
0	0	1	1	LR3
0	1	0	0	LR4
0	1	0	1	LR5
0	1	1	0	DSND1
0	1	1	1	DSND2
1	0	0	0	AMext

Table 65: IRQ mask bits for status byte 0

IM6 to IM0	IRQ output
0	IRQ output not activated
1	IRQ output is activated when the corresponding status bit changes value

[1] The IRQ output is always activated if status bit POR = 1.

8.2 Output status bits

Table 66: Output status registers

Subaddresses must not be sent, they are automatically incremented.

Function	Sub addr	Data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte 0	00	POR	MSUP	ASUP	ROK	LOCK	VID	AFA	AFB
Status byte 1	01	0	0	0	0	0	DCF	0	AGC
Reserved	02	0	0	0	0	0	0	0	0
Status byte 3	03	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Table 67: Power-on reset

POR	Condition
0	normal
1	power-down

Table 68: Main supply

MSUP	Condition
0	main supply not OK
1	main supply OK

Table 69: Audio supply

ASUP	Condition
0	audio supply not OK
1	audio supply OK

Table 70: Reference frequency

ROK	Condition
0	reference frequency not present
1	reference frequency present

Table 71: IF-PLL lock indication

LOCK	Indication
0	IF PLL not locked
1	IF PLL locked

Table 72: Video identification

VID	Indication
0	no video signal detected
1	video signal detected

Table 73: AFC output

AFA	AFB	Condition
0	0	outside window; too low
0	1	outside window; too high
1	0	in window; below reference
1	1	in window; above reference

Table 74: Data link current test

DCF	indication
0	data link current test OK
1	data link current test FAIL

Table 75: Tuner AGC output

AGC	Indication
0	tuner gain reduction active
1	no gain reduction of tuner

Table 76: Mask version indication

ID7	ID6	ID5	ID4	ID3	Mask version
0	0	0	0	0	N1A or N1B version
0	0	0	0	1	-
0	0	0	1	0	N1C version
0	0	0	1	1	N1D version
0	0	1	0	0	N1E or N1F version
0	0	1	0	1	N2B version
0	0	1	1	0	N3B version

9. Limiting values

Table 77: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	main supply voltage		-	6.0	V
$V_{CC(1ASW)}$, $V_{CC(2ASW)}$	audio supply voltage		-	9.0	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_{sol}	soldering temperature	for 5 s	-	260	°C
T_j	operating junction temperature		-	150	°C

Table 77: Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{esd}	electrostatic discharge voltage	human body model; C = 100 pF; R = 1.5 kΩ			
		pin SDA		±1500	V
		all other pins		±2000	V
		machine model; C = 200 pF; R = 0 Ω			
		pin SDA		±150	V
		all other pins		±200	V

10. Thermal characteristics

Table 78: Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	30	K/W

[1] The value given for the thermal resistance from junction to ambient should only be considered as an indication. Most of the dissipated heat is conveyed to the ambient air through the Printed-Circuit Board (PCB) on which the IC is mounted. The actual value of the thermal resistance depends on the number of metal layers, size and layout of the PCB, and also on the dissipation of other components on the PCB.

11. Characteristics

Table 79: Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
Power supplies							
V_P	main supply voltage			4.75	5.0	5.25	V
I_P	main supply current			-	285	320	mA
$V_{CC(1ASW)}$, $V_{CC(2ASW)}$	audio supply voltage		[1]	4.75	8.0	8.4	V
$I_{CC(ASW)}$	audio supply current		[1]	-	3.5	5.0	mA
$V_{CC(SUP)}$	minimum required voltage to set status bit MSUP			-	4.0	-	V
$V_{CC(ASW1)}$	minimum required voltage to set status bit ASUP			-	4.0	-	V
P_{tot}	total power dissipation			-	1.45	1.70	W
Reference voltages							
V_{BGDEC}	band gap decoupling voltage on pin BGDEC			2.20	2.30	2.40	V
V_{RREF}	voltage on pin RREF			2.19	2.30	2.41	V
V_{VD2V5}	digital supply decoupling voltage at pin VD2V5			2.35	2.50	2.65	V
V_{POR}	Power-On Reset (POR) level on pin VD2V5			1.8	2.0	2.2	V

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Voltage regulators							
V_{AUDO}, V_{DEFLO}	output voltage range		[2]	1.25	-	3.30	V
V_{AUDS}, V_{DEFLS}	voltage at feedback pin			1.24	1.27	1.31	V
Video IF circuit							
Video IF amplifier inputs							
$V_{i(dif)(rms)}$	input sensitivity (differential; RMS value)	AGC set					
		f_i = 38.9 MHZ		-	75	150	µV
		f_i = 45.75 MHz		-	75	150	µV
		f_i = 58.75 MHz		-	75	150	µV
$R_{i(dif)}$	input resistance (differential)		[3]	-	2	-	kΩ
$C_{i(dif)}$	input capacitance (differential)		[3]	-	3	-	pF
ΔG_v	gain control range			64	-	-	dB
$V_{i(max)(dif)(rms)}$	maximum input signal (differential; RMS value)			150	-	-	mV
PLL demodulator [4] [5]							
Δf_{VCO}	free-running frequency offset of VCO	PLL not locked; deviation from nominal setting		–500	-	0	kHz
$f_{cr(PLL)}$	catching range PLL	without SAW filter; referred to selected IF system frequency		±1	-	-	MHz
$t_{d(ident)}$	delay time of identification	bit LOCK = 1		-	-	20	ms
Video amplifier output: pin CVBSOUTIF [6]							
$V_{o(z)}$	zero signal output level	negative modulation	[7]	-	3.5	-	V
		positive modulation; note	[7]	-	1.1	-	V
$V_{o(ts)}$	top sync level	negative modulation		1.3	1.4	1.5	V
$V_{o(w)}$	white level	positive modulation		-	3.4	-	V
$V_{o(dem)(p-p)}$	demodulated CVBS output signal (peak-to-peak value)	recommended settings for bits VA1 and VA0	[8]	1.8	2.0	2.2	V
ΔV_o	difference in amplitude between negative and positive modulation	recommended settings for bits VA1 and VA0	[8]	-	0	15	%
$Z_{o(v)}$	video output impedance			-	150	250	Ω
$I_{bias(int)}$	internal bias current of NPN emitter follower output transistor			-	0.9	-	mA
$I_{source(max)}$	maximum source current			-	-	1	mA
$B_{v(-3dB)}$	bandwidth of demodulated video output signal	at –3 dB; before sound trap		6	9	-	MHz
G_{dif}	differential gain	negative modulation	[9]	-	2	5	%
		positive modulation	[9]	-	3	5	%

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
φ_{dif}	differential phase		[9] [10]	-	-	5	deg
NL_{vid}	video non-linearity		[11]	-	-	5	%
V_{clamp}	white spot clamp level			-	3.8	-	V
N_{clamp}	noise inverter clamping level		[12]	-	0.9	-	V
N_{ins}	noise inverter insertion level		[12]	-	2.3	-	V
d_{blue}	intermodulation at 'blue'		[10] [13]				
		V_o at 0.92 MHz or 1.1 MHz		60	66	-	dB
		V_o at 2.66 MHz or 3.3 MHz		60	66	-	dB
d_{yellow}	intermodulation at 'yellow'		[10] [13]				
		V_o at 0.92 MHz or 1.1 MHz		56	62	-	dB
		V_o at 2.66 MHz or 3.3 MHz		60	66	-	dB
S/N	signal-to-noise ratio		[10] [14]				
		weighted		56	60	-	dB
		unweighted		49	53	-	dB
ΔV_{rc}	residual carrier signal		[10]	-	5.5	-	mV
$\Delta V_{rc(2H)}$	residual 2nd harmonic of carrier signal		[10]	-	2.5	-	mV
IF and tuner AGC [15]							
Timing of IF AGC							
MVI	modulated video interference	30 % AM for 1 V to 100 mV; 0 Hz to 200 Hz (B/G standard)		-	-	10	%
t_{res}	response time	IF input signal amplitude increase of 52 dB; positive and negative modulation; IF AGC time constant set to normal		-	2	-	ms
		IF input signal amplitude decrease of 52 dB					
		negative modulation		-	50	-	ms
		positive modulation		-	100	-	ms
Tuner take over adjustment (via I^2C-bus)							
$V_{start(min)(rms)}$	minimum starting level for tuner take over (RMS value)			-	0.4	0.8	mV
$V_{start(max)(rms)}$	maximum starting level for tuner take over (RMS value)			100	150	-	mV
Tuner control output							
$V_{o(max)}$	maximum tuner AGC output voltage	maximum tuner gain	[3]	-	-	5	V
$V_{o(sat)}$	output saturation voltage	minimum tuner gain; I_o = 1 mA		-	-	300	mV
$I_{o(TUNERAGC)}$	tuner AGC output current pin TUNERAGC			1	-	-	mA
I_L	leakage current RF AGC			-	-	1	µA

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔV_i	input signal variation for complete tuner control			0.5	2	4	dB
AFC output (via I²C-bus) [16]							
f_{AFC}	AFC resolution			-	2	-	bit
Δf_w	window sensitivity			-	125	-	kHz
Δf_{lw}	window sensitivity in large window mode			-	275	-	kHz
DTV IF circuit							
DTV IF amplifier input							
$V_{i(dif)(rms)}$	input sensitivity (differential; RMS value)	f_i between 30 MHz and 60 MHz		-	75	150	µV
$R_{i(dif)}$	input resistance (differential)		[3]	-	2	-	kΩ
$C_{i(dif)}$	input capacitance (differential)		[3]	-	3	-	pF
ΔG_v	gain control range			64	-	-	dB
$V_{i(max)(dif)(rms)}$	maximum input signal (differential; RMS value)			150	-	-	mV
DTV IF mixer							
f_{osc}	oscillator frequency	step size 250 kHz		24	-	64	MHz
$N_{\varphi(osc)}$	oscillator phase noise	carrier to noise ratio in dBc/Hz		-	–92	-	dB
PB_{ll}	lower limit pass-band			-	-	1.0	MHz
PB_{ul}	upper limit pass-band			10.0	-	-	MHz
PBR	pass-band ripple			-	-	0.5	dB
B_{sb}	stop band			-	44	-	MHz
α_{sb}	stop band attenuation			40	-	-	dB
External AGC control							
ΔV_i	voltage range for full control of the amplifier			1	-	3	V
Z_i	input impedance			1	-	-	MΩ
DTV output (down-mixed output signal)							
$V_{o(dif)(p-p)}$	differential output signal (peak-to-peak value)	internal AGC mode; no modulation					
		DTV 1st IF mode; f = 40 MHz		-	0.68	-	V
		DTV 2nd IF mode; f = 4 MHz		-	1.20	-	V
$V_{o(dif)(p-p)(max)}$	maximum allowed differential output signal (peak-to-peak value)	external AGC mode	[17]				
		DTV 1st IF mode; f = 40 MHz		-	0.95	-	V
		DTV 2nd IF mode; f = 4 MHz		-	1.68	-	V
$Z_{o(dif)}$	output impedance (differential)			-	150	-	Ω
V_O	DC output level	DTV 1st IF mode		-	1.15	-	V
		DTV 2nd IF mode		-	3.0	-	V

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{bias(int)}$	internal bias current of emitter followers			-	2	-	mA
$I_{source(max)}$	maximum allowed source current			-	-	2	mA
Sound IF circuit							
Sound IF amplifier							
$V_{i(rms)}$	input sensitivity (RMS value)	–3 dB		-	45	-	dBµV
$V_{i(max)(rms)}$	maximum input signal (RMS value)			100	-	-	dBµV
$R_{i(dif)}$	input resistance (differential)		[3]	-	2	-	kΩ
$C_{i(dif)}$	input capacitance (differential)		[3]	-	3	-	pF
ΔG_v	gain control range			-	55	-	dB
$\alpha_{ct(SIF-VIF)}$	crosstalk attenuation between SIF and VIF input			50	-	-	dB
Sound IF intercarrier output on DTV output, FM modulation [18]							
$V_{o(dif)(rms)}$	differential output signal amplitude (RMS value)	SC1; sound carrier 2 off		75	100	125	mV
B_{-3dB}	bandwidth (–3 dB)			7.5	8.5	-	MHz
$\Delta V_{r(SC)(rms)}$	residual IF sound carrier (RMS value)			-	2	-	mV
$Z_{o(dif)}$	output impedance (differential)			-	150	-	Ω
V_O	DC output voltage			-	1.3	-	V
$I_{bias(int)}$	internal bias current of emitter followers			-	2	-	mA
$I_{source(max)}$	maximum allowed source current			-	2	-	mA
S/N_W	weighted signal-to-noise ratio (SC1/SC2)	ratio of PC/SC1 at vision IF input of 40 dB or higher	[19]				
		black picture		53/48	58/55	-	dB
		white picture		52/47	55/53	-	dB
		6 kHz sinewave (black-to-white modulation)		44/42	48/46	-	dB
		250 kHz sine wave (black-to-white modulation)		44/25	48/30	-	dB
		sound carrier subharmonics (f = 2.75 MHz ± 3 kHz)		45/44	51/50	-	dB
		sound carrier subharmonics (f = 2.87 MHz ± 3 kHz)		46/45	52/51	-	dB
AM sound output [20]							
$V_{o(rms)}$	AF output signal amplitude (RMS value)	54 % modulation		400	500	600	mV

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD	total harmonic distortion	54 % modulation		-	0.5	1.0	%
		80 % modulation		-	-	5.0	%
B_{-3dB}	–3 dB AF bandwidth			100	125	-	kHz
S/N_W	weighted signal-to-noise ratio	54 % modulation		47	53	-	dB
PSRR	power supply ripple rejection ratio	5 V main supply		-	17	-	dB
2nd sound IF AGC circuit							
2nd Sound IF external input							
$\Delta V_{i(rms)}$	input voltage range (RMS value)			18	-	320	mV
Δf_i	input frequency range		[21]	4	-	10.7	MHz
R_i	input resistance		[3]	-	25	-	kΩ
C_i	input capacitance		[3]	-	3	-	pF
2nd Sound IF AGC							
ΔG	gain control range			-	25	-	dB
$I_{ch(AGC)}$	charge current AGC pin	FM mode		-	-	12.5	µA
		AM mode		-	-	2.5	µA
$I_{dch(AGC)}$	discharge current AGC pin	FM mode		-	-	50	µA
		AM mode		-	-	2.5	µA
		overload		-	1	-	mA
Digital output							
$n_{d(p-p)}$	decimal digital output level (peak-to-peak value)	FM mode		-	716	-	
		AM mode; no modulation		-	358	-	
Sound trap and group delay correction filter							
Sound trap							
$B_{v(-3dB)}$	–3 dB video bandwidth (sound trap + group delay)	f_{SC1} = 4.5 MHz		3.90	4.00	-	MHz
		f_{SC1} = 5.5 MHz		4.80	4.90	-	MHz
		f_{SC1} = 6.0 MHz		5.25	5.35	-	MHz
		f_{SC1} = 6.5 MHz		5.70	5.80	-	MHz
$\Delta V_{chrom(p)}$	peaking at chroma subcarrier frequency			-	1.0	2.0	dB
α_{SC1}	attenuation at first sound carrier f_{SC1}	all trap frequencies		28	33	-	dB
α_{SC2}	attenuation at second sound carrier f_{SC2}	f = 4.726 MHz; f_{SC1} = 4.5 MHz		21	27	-	dB
		f = 5.742 MHz; f_{SC1} = 5.5 MHz		21	27	-	dB
		f = 6.55 MHz; f_{SC1} = 6.0 MHz		12	18	-	dB
		f = 6.742 MHz; f_{SC1} = 6.5 MHz		18	24	-	dB

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Group delay correction; Figure 6 and Figure 7 [22]							
$t_{d(g)}$	group delay	f = 4.43 MHz; sound trap frequency 5.5 MHz; sound trap only		-	180	-	ns
		f = 4.43 MHz; sound trap frequency 5.5 MHz; sound trap plus group delay correction filter		-	170	-	ns
Video switches							
CVBS and YC switches							
$V_{i(CVBS/Y)(p-p)}$	CVBS or Y input voltage (peak-to-peak value)			-	1.0	1.76	V
$V_{i(CVBS/Y)(clip)}$	CVBS or Y clipping level	black-to-peak video		-	1.33	-	V
$I_{i(CVBS/Y)}$	CVBS or Y input current	outside clamp pulse		-	0	-	µA
		during clamp pulse		–10	-	+10	µA
$\alpha_{sup(CVBSn)}$	suppression of non-selected CVBS input signal		[10]	50	-	-	dB
$V_{i(C)(p-p)}$	chrominance input voltage (peak-to-peak value)	100 % color bar	[3]	-	885	1264	mV
$Z_{i(C)}$	chrominance input impedance			-	50	-	kΩ
Video ident function							
$V_{sync(min)}$	minimum sync pulse amplitude			70	100	140	mV
$t_{d(ident)}$	delay time of identification	I^2C-bus status bit VID = 1; after the Video IF AGC has stabilized on a new transmitter		-	-	10	ms
Analog CVBS outputs: pins CVBSOUTA and CVBSOUTB							
Z_o	output impedance			-	-	250	Ω
$V_{o(p-p)}$	output signal amplitude (peak-to-peak value)	at input signal of 1.0 V (p-p)		-	2.0	-	V
V_O	DC output level	top sync		-	0.4	-	V
		output muted		-	0.5	-	V
Digital outputs							
CVBS/Y signal							
$n_{d(black)}$	decimal digital output level for black	black clamp mode		-	240	-	
$n_{d(white)}$	decimal digital output level for white	nominal input signal		-	652	-	
C signal							
$n_{d(black)}$	decimal digital output level for black			480	512	544	
$n_{d(p-p)}$	decimal digital output amplitude (peak-to-peak value)	nominal input level; 100 % color bar		-	520	-	

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RGB, YPbPr and YUV inputs							
Analog inputs							
General							
I_i	input current	outside clamp pulse		-	0	-	µA
		during clamp pulse		–10	-	+10	µA
RGB mode							
$V_{i(b-w)}$	input signal amplitude (black-to-white value)			-	0.7	1.0	V
YPbPr mode							
$V_{i(Y)(p-p)}$	Y input signal amplitude (peak-to-peak value)	top sync-to-white		-	1.0	1.43	V
$V_{i(Pb)(p-p)}$	Pb input signal amplitude (peak-to-peak value)	100 % color bar		-	0.7	1.0	V
$V_{i(Pr)(p-p)}$	Pr input signal amplitude (peak-to-peak value)	100 % color bar		-	0.7	1.0	V
YUV mode							
$V_{i(Y)}$	Y input signal amplitude	top sync-to-white		-	1.43	2.04	V
$V_{i(U)(p-p)}$	U input signal amplitude (peak-to-peak value)	100 % color bar		-	1.77	2.53	V
$V_{i(V)(p-p)}$	V input signal amplitude (peak-to-peak value)	100 % color bar		-	1.40	2.00	V
Digital outputs							
General							
Δt_d	delay difference for the three channels		[10]	-	0	20	ns
Y signal							
$n_{d(black)}$	decimal digital output level for black	black clamp mode		-	240	-	
$n_{d(white)}$	decimal digital output level for white	nominal input level		-	788	-	
U and V signals [23]							
$n_{d(black)}$	decimal digital output level for black	black clamp mode		-	512	-	
$n_{d(p-p)}$	decimal digital output amplitude (peak-to-peak value)	nominal input level; 100 % color bar		-	716	-	
Video anti-alias filters							
CVBS, Y_{yc}, C and 2nd SIF filters							
$f_{pb(-1dB)}$	–1.0 dB pass-band frequency			-	8.0	-	MHz
$f_{pb(-3dB)}$	–3.0 dB pass-band frequency			-	9.0	-	MHz
$f_{sb(-35dB)}$	–35 dB stop band frequency			-	20	-	MHz

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(g)}$	group delay	at 1.0 MHz		-	36	-	ns
		at 5.0 MHz		-	42	-	ns
$E_{\Delta G}$	differential gain error		[9]	-	2	5	%
$E_{\Delta\varphi}$	differential phase error		[9] [10]	-	-	5	deg
S/N	signal-to-noise ratio	B = 5 MHz	[24]	60	-	-	dB
Y_{yuv} filters							
$f_{pb(-1dB)}$	–1.0 dB pass-band frequency	$1f_H$ mode		-	8.0	-	MHz
		$2f_H$ mode		-	16	-	MHz
$f_{pb(-3dB)}$	–3.0 dB pass-band frequency	$1f_H$ mode		-	9.0	-	MHz
		$2f_H$ mode		-	18	-	MHz
$f_{sb(-35dB)}$	–35 dB stop band frequency	$1f_H$ mode		-	20	-	MHz
		$2f_H$ mode		-	40	-	MHz
$t_{d(g)}$	group delay	at 1 MHz; $1f_H$ mode		-	36	-	ns
		at 1 MHz; $2f_H$ mode		-	18	-	ns
		at 5 MHz; $1f_H$ mode		-	42	-	ns
		at 10 MHz; $2f_H$ mode		-	21	-	ns
S/N	signal-to-noise ratio	$1f_H$ mode: B = 5 MHz $2f_H$ mode: B = 10 MHz	[24]	60	-	-	dB
U and V filters							
$f_{pb(-1dB)}$	–1.0 dB pass-band frequency	$1f_H$ mode		-	4.0	-	MHz
		$2f_H$ mode		-	8.0	-	MHz
$f_{pb(-3dB)}$	–3.0 dB pass-band frequency	$1f_H$ mode		-	4.5	-	MHz
		$2f_H$ mode		-	9.0	-	MHz
$f_{sb(-35dB)}$	–35 dB stop band frequency	$1f_H$ mode		-	10	-	MHz
		$2f_H$ mode		-	20	-	MHz
$t_{d(g)}$	group delay	at 1 MHz; $1f_H$ mode		-	72	-	ns
		at 1 MHz; $2f_H$ mode		-	36	-	ns
		at 5 MHz; $1f_H$ mode		-	84	-	ns
		at 10 MHz; $2f_H$ mode		-	42	-	ns
S/N	signal-to-noise ratio	$1f_H$ mode: B = 5 MHz $2f_H$ mode: B = 10 MHz	[24]	60	-	-	dB
Filter for DTV 2nd 2nd IF signal							
$f_{pb(-1dB)}$	–1.0 dB pass-band frequency			-	10	-	MHz
$f_{pb(-3dB)}$	–3.0 dB pass-band frequency			-	12	-	MHz
$f_{sb(-35dB)}$	–35 dB stop band frequency			-	44	-	MHz
$t_{d(g)}$	group delay			-	22	-	ns
				-	32	-	ns
S/N	signal-to-noise ratio	B = 10 MHz	[25]	60	-	-	dB

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Video analog-to-digital converters						
General [26]						
$B_{V(-3dB)}$	–3dB signal bandwidth		-	9	-	MHz
f_{sample}	sample frequency		-	27	-	MHz
RES	resolution		-	10	-	bit
Static measurements						
DNL	differential non-linearity	f_{clk} = 54 MHz; f_{signal} = 10 MHz	-	0.7	-	LSB
INL	integral non-linearity	f_{clk} = 54 MHz; f_{signal} = 10 MHz	-	1	-	LSB
Dynamic measurements						
THD	total harmonic distortion	f_{clk} = 27 MHz; f_{signal} = 5 MHz	-	–63	-	dB
		f_{clk} = 54 MHz; f_{signal} = 10 MHz	-	–63	-	dB
S/N	signal-to-noise ratio	f_{clk} = 27 MHz; B = 5 MHz	-	58	-	dB
		f_{clk} = 54 MHz; B = 10 MHz	-	58	-	dB
ENOB	effective number of bits	f_{clk} = 54 MHz; f_{signal} = 10 MHz	-	9.0	-	bit
Audio selectors						
LR inputs						
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	5 V audio supply	1.0	-	-	V
		8 V audio supply	2.0	-	-	V
R_i	input resistance		24	32	-	kΩ
G	gain from LR inputs to analog outputs	outputs unloaded	–0.4	0	+0.3	dB
$\alpha_{(LRn)}$	crosstalk attenuation from non-selected inputs	f = 10 kHz	70	80	-	dB
DSND inputs for audio signals coming from digital video processor						
$V_{i(max)(rms)}$	maximum input signal amplitude (RMS value)		1.0	-	-	V
R_i	input resistance		24	32	-	kΩ
G	gain from DSND inputs to analog outputs	5 V audio supply; DSG = 0; outputs unloaded	–0.4	0	+0.3	dB
		8 V audio supply; DSG = 1; outputs unloaded	5.6	6.0	6.3	dB
$\alpha_{(DSNDn)}$	crosstalk attenuation from non-selected inputs		70	80	-	dB
Microphone amplifiers [27]						
R_i	input resistance		-	20	-	kΩ
G_{low}	low gain	bits M1G = M2G = 0	-	17	-	dB
G_{high}	high gain	bits M1G = M2G = 1	-	35	-	dB
Δf	frequency range		50	-	20000	Hz
THD + N	total harmonic distortion plus noise	1 kHz input signal at 0.9 V (RMS) output level	–74	–80	-	dB

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S/N	signal-to-noise ratio	referred to 16 mV (RMS) input level				
		low gain	70	76	-	dB
		high gain	74	80	-	dB
Analog outputs						
$V_{o(max)(rms)}$	maximum output signal amplitude (RMS value)	5 V audio supply	1.0	-	-	V
		8 V audio supply	2.0	-	-	V
Z_o	output impedance			500	650	Ω
THD + N	total harmonic distortion plus noise	1 kHz input signal				
		+6 dBV output level	–80	–88	-	dB
		–54 dBV output level; A-weighted	–36	–40	-	dB
S/N	signal-to-noise ratio	referred to 0 dBV output level; A-weighted	90	96	-	dB
Δf	frequency range		20	-	20000	Hz
PSRR	power supply ripple rejection ratio	1 kHz ripple frequency				
		ripple on 5 V main supply	-	43	-	dB
		ripple on 8 V audio supply	-	45	-	dB
Audio analog-to-digital converters						
Digital audio outputs [28]						
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	5 V audio supply	1.0	-	-	V
		8 V audio supply	2.0	-	-	V
THD + N	total harmonic distortion plus noise	1 kHz input signal				
		+0 dBV output level	-	–78	-	dB
		–54 dBV output level; A-weighted	-	–30	-	dB
S/N	signal-to-noise ratio	referred to 0 dBV input level; A-weighted	-	86	-	dB
α_{cs}	channel separation	0 kHz to 20 kHz	-	80	-	dB
V_o	digital output level	at 2 V (RMS) input level	-	–4.3	-	dBFS
PSRR	power supply ripple rejection ratio	8 V audio supply voltage; 1 kHz ripple frequency				
		ripple on 5 V main supply	-	54	-	dB
		ripple on 8 V audio supply	-	55	-	dB
		5 V audio supply voltage; 1 kHz ripple frequency	-	18	-	dB
Timing circuit						
HV input signals: pins HV_PRIM and HV_SEC [29] [30]						
Timing specification for HV pulses coming from digital video processor; see Figure 8						
$t_{(HV\text{-}sync)}$	time between start HV pulse and start of horizontal sync pulse on CVBS/Y signal	$1f_H$ TV mode	-	0.6	-	µs
		$2f_H$ mode; HDTV = 0	-	0.3	-	µs
		$2f_H$ mode; HDTV = 1	-	0.3	-	µs

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{W(HV)}$	width of HV pulses	$1f_H$ TV mode				
		normal lines	-	72	-	ck
		clamp disable lines	-	128	-	ck
		vsync lines	-	288	-	ck
		$2f_H$ mode HDTV = 0				
		normal lines	-	36	-	ck
		clamp disable lines	-	64	-	ck
		vsync lines	-	144	-	ck
		$2f_H$ mode; HDTV = 1				
		normal lines	-	20	-	ck
		clamp disable lines	-	44	-	ck
		vsync lines	-	144	-	ck
Detection of clamp disable lines						
$t_{det(clamp)(dis)}$	clamp disable detection	$1f_H$ TV mode	-	80	-	ck
		$2f_H$ mode; HDTV = 0	-	40	-	ck
		$2f_H$ mode; HDTV = 1	-	24	-	ck
Detection of vsync lines						
$t_{det(vsync)}$	vsync detection	$1f_H$ TV mode	-	255	-	ck
		$2f_H$ mode; HDTV = 0	-	136	-	ck
		$2f_H$ mode; HDTV = 1	-	136	-	ck
Internal clamp pulses						
$t_{d(HV-clamp)}$	delay between start of HV pulse and start of clamp pulse	$1f_H$ TV mode	-	80	-	ck
		$2f_H$ mode; HDTV = 0	-	40	-	ck
		$2f_H$ mode; HDTV = 1	-	24	-	ck
$t_{W(clamp)}$	width of clamp pulse	$1f_H$ TV mode	-	44	-	ck
		$2f_H$ mode; HDTV = 0	-	22	-	ck
		$2f_H$ mode; HDTV = 1	-	17	-	ck
Crystal reference frequency input: pin XREF						
R_i	input resistance		25	35	45	kΩ
C_i	input capacitance		-	3	-	pF
$V_{i(p-p)}$	input signal amplitude (peak-to-peak value)		1	-	3.5	V
Data link transmitters						
General						
$f_{word(CLK)}$	word clock frequency		-	13.5	-	MHz
WL	word length		-	44	-	bit
f_D	data rate		-	594	-	Mbit/s
$f_{bit(CLK)}$	bit clock frequency	individual data and strobe signals	-	297	-	MHz
Output drivers for data and strobe signals						
$\Delta V_{o(p-p)}$	voltage swing (peak-to-peak value)	individual pins; output loaded with 100 Ω	-	0.3	-	V

Table 79: Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{o(dif)(p-p)}$	differential output voltage (peak-to-peak value)	output loaded with 100 Ω		-	0.6	-	V
R_o	output resistance			-	-	50	Ω
R_L	load resistance	connected between positive terminal and negative terminal		-	100	-	Ω
East-west drive circuit: pins EWVIN, EWIOUT and REW							
R_i	input resistance			-	40	-	kΩ
ΔV_i	input voltage range			0	-	3.5	V
R_{ew}	external conversion resistor		[31]	-	750	-	Ω
ΔV_o	output voltage range		[31]	1.0	-	V_{CC}	V
ΔI_o	output current range			0	-	1.2	mA
I^2C-bus control inputs and outputs							
SDA/SCL inputs and outputs	[32]						
V_i	input voltage level			0	-	5.5	V
V_{IL}	LOW-level input voltage			-	-	$0.2 \times V_{CC}$	V
V_{IH}	HIGH-level input voltage			$0.5 \times V_{CC}$	-	-	V
I_{IL}	LOW-level input current	V_i = 0 V		-	0	-	µA
I_{IH}	HIGH-level input current	V_i = 5.5 V		-	0	-	µA
V_{OL}	LOW-level output voltage	SDA pin; I_L = 3 mA		-	-	0.4	V
C_i	input capacitance			-	5	10	pF
IRQ output	[33]						
V_{OL}	LOW-level output voltage	IRQ pin; I_L = 1.5 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	open drain		-	-	5.5	V

[1] The supply voltage for the analog audio part may have a value between 5 V and 8 V. For a supply voltage of 5 V the maximum amplitude of in- and output signals is 1 V (RMS). For a supply voltage of 8 V the maximum amplitude of in- and output signals is 2 V (RMS).

[2] The value of the regulated voltage is determined by the external resistive voltage divider. The voltage range mentioned relates to the voltage at the emitter of the external transistor. The stability of the voltage regulator loop depends on the value of the decoupling capacitor on the emitter of the external transistor. Recommended value is $C_{dec} = 1.5 \times \frac{I_o}{V_o}$ µF, with I_o in mA.

[3] This parameter is not tested during production and is just given as application information for the designer of the television receiver.

[4] Loop bandwidth B_L = 60 kHz (natural frequency f_N = 15 kHz; damping factor d = 2; calculated with top sync level as FPLL input signal level).

[5] The IF-PLL demodulator uses an internal VCO (no external LC-circuit required) which is calibrated by means of a digital control circuit which uses the clock frequency of the microcontroller/teletext decoder as a reference. The required IF frequency for the various standards is set via the I^2C-bus. When the system is locked the resulting IF frequency is very accurate with a deviation from the nominal value of less than 25 kHz.

[6] Measured at pin CVBSOUTIF pin with 10 mV (RMS) top sync input signal at VIF input.

[7] So called projected zero point, i.e. with switched demodulator.

[8] The signal amplitude at the CVBSOUTIF output depends on the settings of bits VA1 and VA0. The recommended settings for negative modulation (bit PMOD = 0), is VA1 = VA0 = 1. For positive modulation (bit PMOD = 1), the setting VA1 = 1 and VA0 = 0. is recommended. The $V_{0(dem)(p-p)}$ and ΔV_o values specified are valid if the recommended settings are used.

[9] Measured in accordance with the test line given in Figure 3. For the differential phase test the peak white setting is reduced to 87 %:

a) The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.

b) The phase difference is defined as the difference in degrees between the largest and smallest phase angle.

[10] This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.

[11] This figure is valid for the complete video signal amplitude (peak white-to-black), see Figure 4.

[12] The noise inverter is only active in the strong signal mode (no noise detected in the incoming signal).

[13] The test set-up and input conditions are given in Figure 5. Measurement is done with an input signal of 10 mV (RMS).

[14] Measured at an input signal of 10 mV (RMS). The S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value); B = 5 MHz. Weighted in accordance with CCIR 567.

[15] The time-constant of the IF AGC is internal and the speed of the AGC can be set via bus bits AGC1 and AGC0. The AGC response time is also dependent on the acquisition time of the PLL demodulator. The values given are valid for the 'norm' setting (AGC1 = 0 and AGC0 = 1) and when the PLL is in lock.

[16] The AFC control voltage is generated by the digital tuning system of the PLL demodulator. This system uses the external crystal frequency as a reference and is therefore very accurate. For this reason no maximum and minimum values are given for the window sensitivity figures. The tuning information is supplied to the tuning system via the I^2C-bus. Two bits are reserved for this function. The AFC value is valid only when bit LOCK = 1.

[17] Exceeding this amplitude leads to intermodulation distortion.

[18] The intercarrier sound (2nd SIF) signal is not normally an analog output signal of the IC. It can be made available on the DTV output pins by setting bus bits DSIF = 1 and DFIF = 0.

[19] The weighted S/N ratio is measured under the following conditions:

a) The vision IF modulator incidental phase modulation for black-to-white jumps less than 0.5 degrees.

b) QSS AF performance of the vision IF modulator, measured with the television demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (deviation 27 kHz) for 6 kHz sine wave black-to-white modulation.

c) Picture-to-sound carrier ratio of the vision IF modulator: PC/SC1 = 13 dB (transmitter).

d) The measurements must be carried out with the Siemens SAW filters G3962 for vision IF and G9350 for sound IF. Input level for sound IF 10 mV (RMS) with 27 kHz deviation.

e) The PC/SC ratio at the vision IF input is calculated as the addition of the TV transmitter ratio and the SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N(W) values as indicated.

[20] The demodulated AM sound signal can be made available in the analog domain on LINE or SCART audio outputs by selecting AM internal via the I^2C-bus (bus bit AMX = 0).

[21] The frequency range of the 2nd SIF channel is limited by the 2nd SIF anti-alias filter. If a 10.7 MHz FM radio IF signal is supplied to the external 2nd SIF input, an external 10.7 MHz bandpass filter must be used, and the internal anti-alias filter must be bypassed by setting bus bit SLPM = 1.

[22] The cascade of sound trap and group delay correction filter compensates for the group delay pre-distortion of the BG standard, curve A (see *Recommendation ITU-R BT.470-4*). The indicated values are the difference between the group delay at 4.43 MHz and the group delay at 10 kHz.

[23] The digitized U and V signals have the following polarity: U = +(B−Y) and V = +(R−Y).

[24] The S/N ratio is defined as the ratio of the full scale black-to-white amplitude to the black level noise voltage (RMS value).

[25] The S/N ratio is defined as the ratio of the full scale peak-to-peak signal amplitude to the zero signal noise voltage (RMS value).

[26] The video ADC is specified as a stand-alone circuit. Distortion and noise of the video switch and anti-alias filters is not included.

[27] The gain of the microphone amplifiers can be switched between low (17 dB) and high (35 dB). The low gain can be used for microphones with a sensitivity between 5 mV (RMS) and 40 mV (RMS) at 94 dB SPL. The high gain can be used for microphones with a sensitivity of less than 5 mV (RMS) at 94 dB SPL.

[28] If the audio supply voltage is 8 V; the 5 V full scale reference voltage for the audio A to D converters at pin 91 (VAADCP) is generated by the IC itself, using the internal band gap reference. This gives the best power supply rejection ratio for the digital audio outputs. If the audio supply voltage is 5 V; pin 91 must be connected to the external 5 V supply. This results in a reduced power supply rejection ratio for the digital audio outputs.

[29] Signals HV_PRIM and HV_SEC must be generated by the digital video processor using a 13.5 MHz clock. Where pulse widths are specified in clock pulses, a 13.5 MHz clock is assumed (1 clock pulse is 74.1 ns). To enable detection of the vertical blanking interval, a larger pulse width is used for a number of lines during the vertical blanking period; see Figure 9 and Figure 10.

[30] Most timing parameters in this section are expressed in number of clock cycles, abbreviated as ck.

[31] The east-west drive circuit is a voltage to current converter circuit, that requires an external conversion resistor. The open drain output transistor can only sink current. The relation between input voltage and output current is as follows: $I_o = \frac{V_i}{4 \times R_{ew}}$ where R_{ew} is the external conversion resistor. The voltage across the external conversion resistor is equal to $V_i/4$. The voltage at output pin EWIOUT must not be lower than $V_i/4 + 0.25$ V. The output current must not be larger than 1.2 mA.

[32] The switching levels of pins SDA and SCL are compatible with an external signal amplitude of 3.3 V and 5 V.

[33] The IRQ output is an open-drain output; active LOW. The pin IRQ must be loaded with a pull-up resistor.

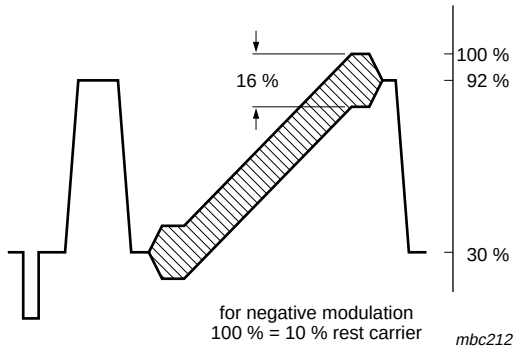


Fig 3. Video output signal

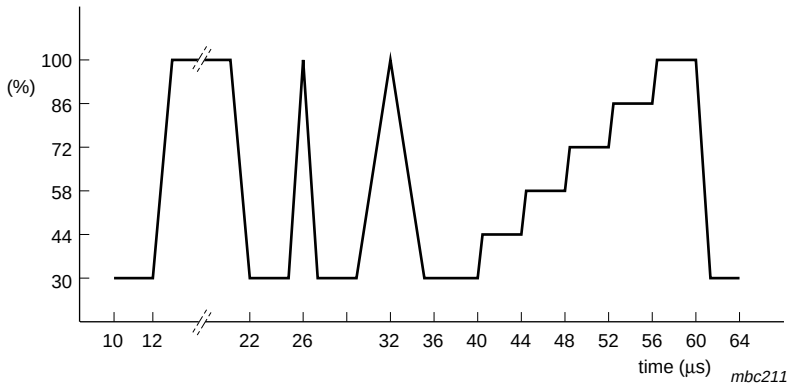
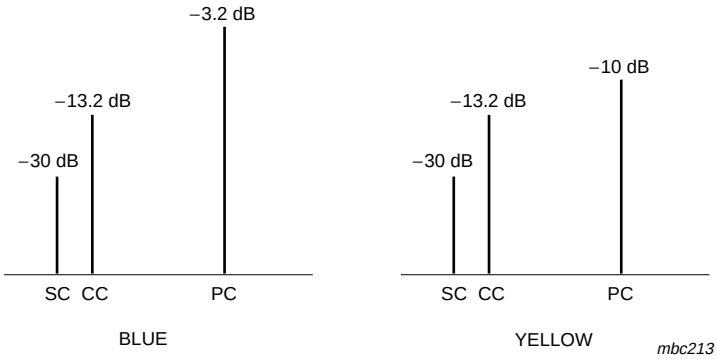


Fig 4. Test signal waveform

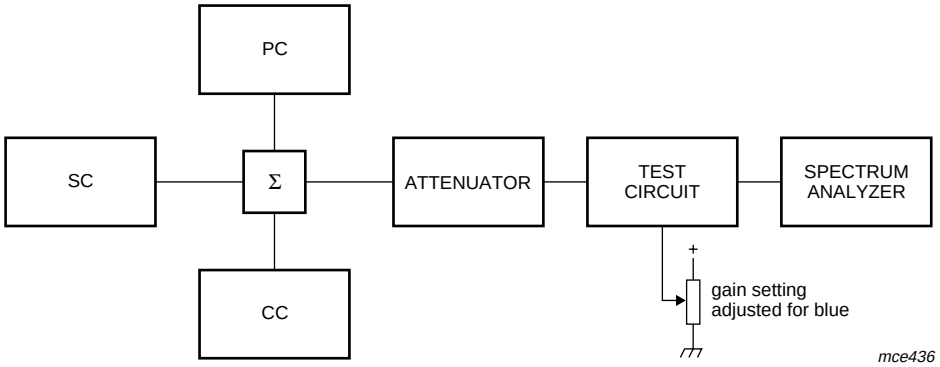


Input signal conditions: SC = sound carrier; CC = color carrier; PC = picture carrier. All amplitudes with respect to top sync level.

$$Value\ at\ 3.58\ MHz\ or\ 1.1\ MHz = 20log\frac{V_o\ at\ 3.58\ MHz\ or\ 4.4\ MHz}{V_o\ at\ 0.92\ MHz\ or\ 1.1\ MHz} + 3.6\ \text{dB}$$

$$Value\ at\ 2.66\ MHz\ or\ 3.3\ MHz = 20log\frac{V_o\ at\ 3.58\ MHz\ or\ 4.4\ MHz}{V_o\ at\ 2.66\ MHz\ or\ 3.3\ MHz}\ \text{dB}$$

a. Input signal conditions



b. Test set-up

Fig 5. Test set-up intermodulation

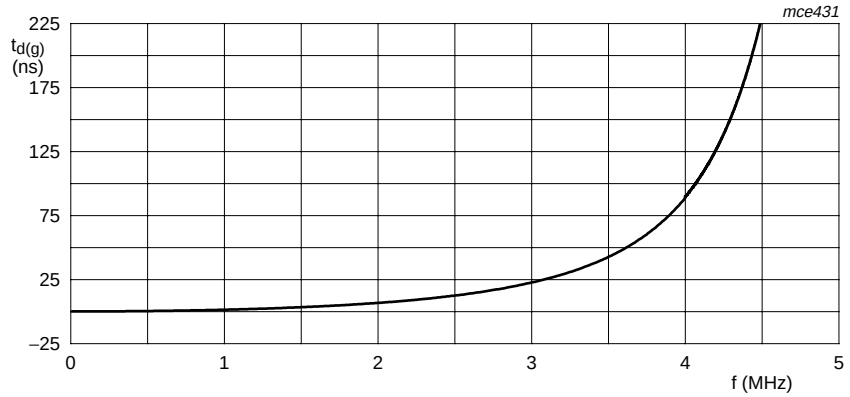


Fig 6. Group delay characteristic without group delay correction (sound trap: 5.5 MHz)

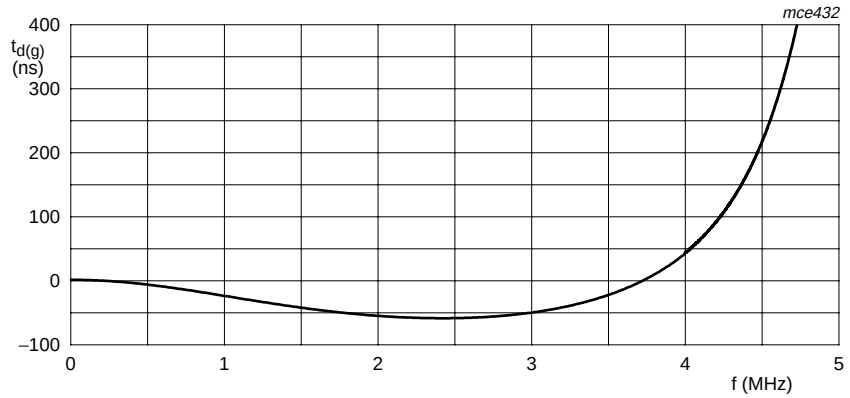


Fig 7. Group delay characteristic with group delay correction (sound trap: 5.5 MHz)

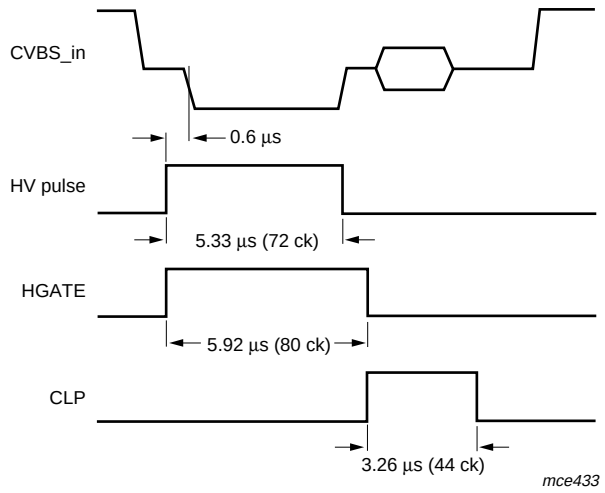


Fig 8. Timing of some horizontal timing signals compared to incoming CVBS signal ($1f_H$ mode)

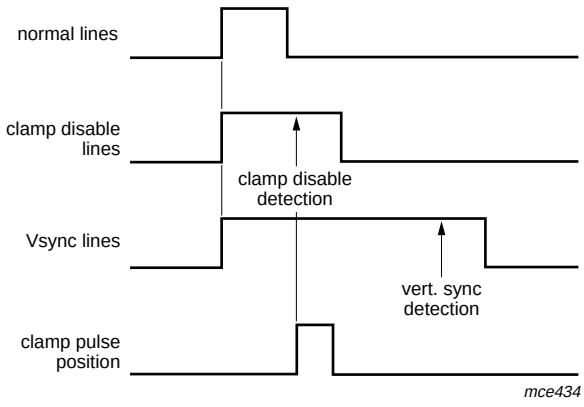


Fig 9. Horizontal timing of HV pulses ($1f_H$ mode)

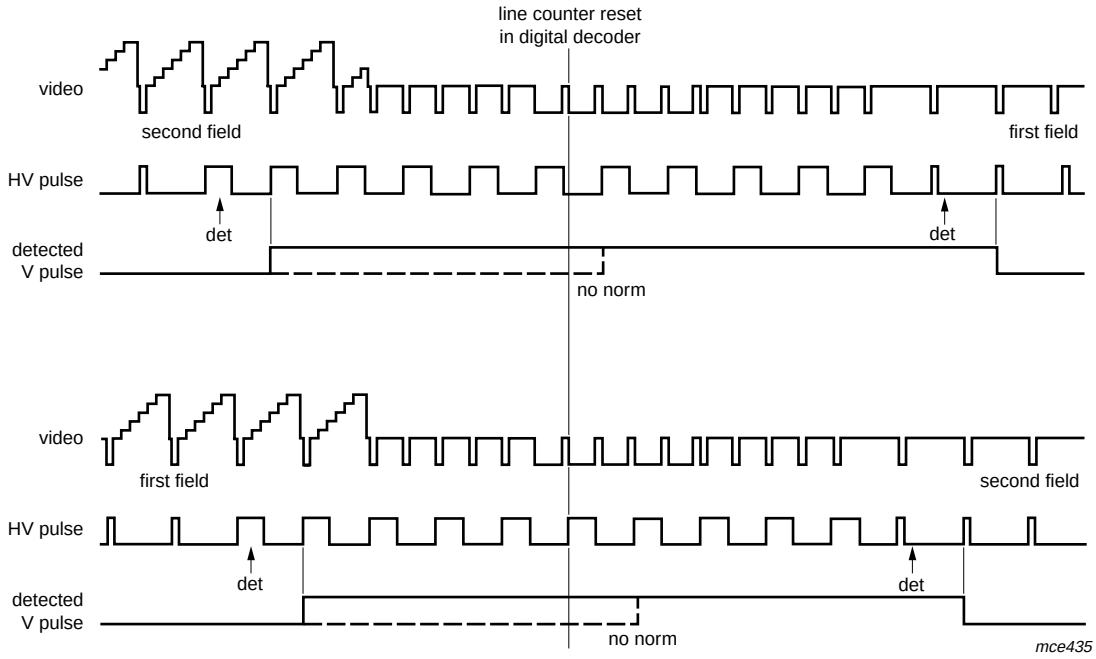


Fig 10. Recommended vertical timing of incoming HV pulses ($1f_H$ mode)

12. Application information

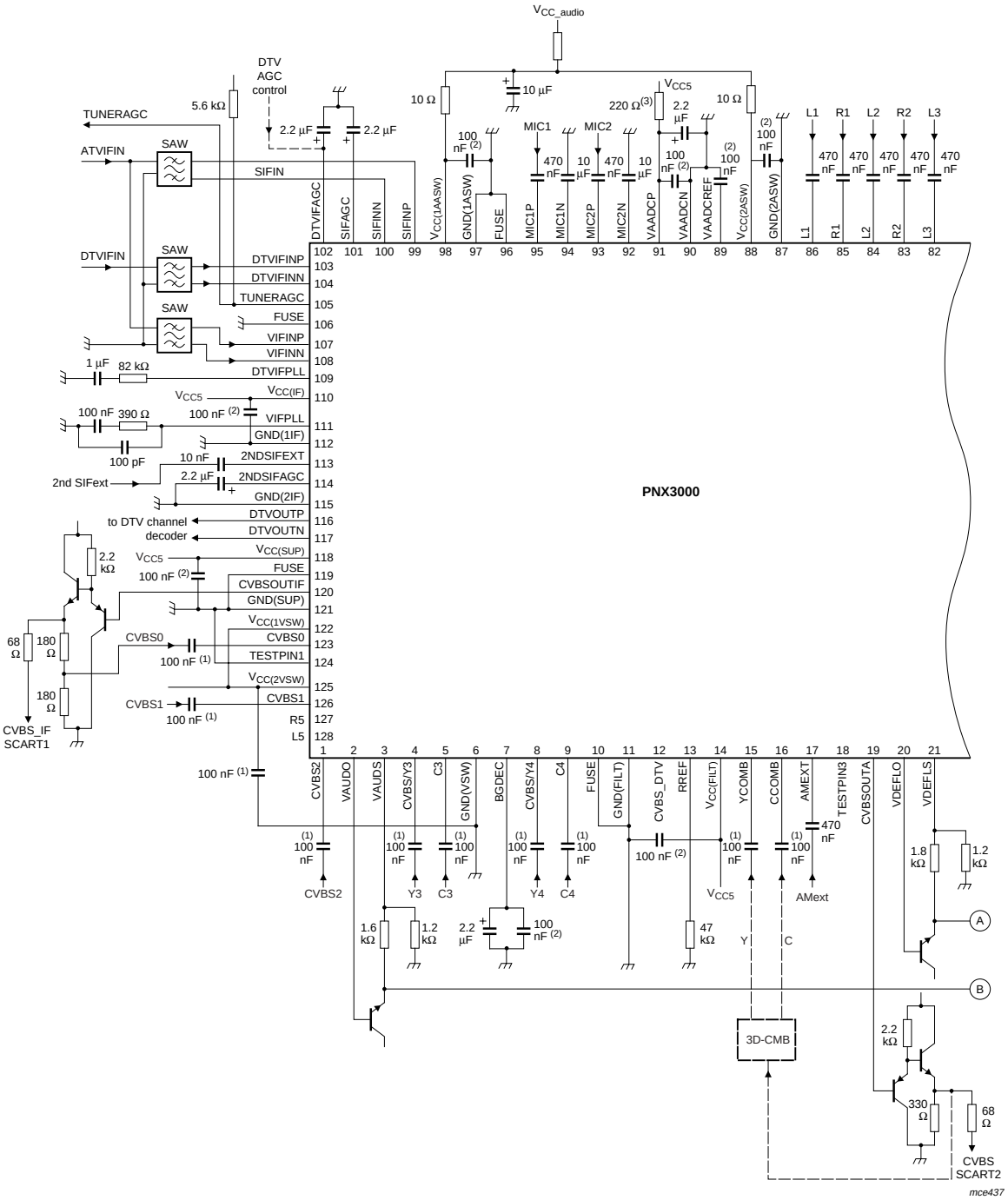
12.1 Power supply and decoupling

For optimal THD and SNR performance of the analog and digital audio channels, it is important to have stable 5 V and 8 V supply voltages for the audio part of the PNX3000.

The following pins need a stable supply voltage without disturbances in the baseband audio frequency range:

- Pins $V_{CC(1ASW)}$ and $V_{CC(2ASW)}$ (pins 98 and 88); the supply voltage for the analog audio switches. The supply current to both of these pins is less than 5 mA. Note that this supply voltage may be 5 V or 8 V.
- Pin VAADCP (pin 91); the 5 V full scale reference for the audio ADCs. The current consumption of this pin is about 0.25 mA. This pin must only be connected to the 5 V supply if an audio supply voltage (pins $V_{CC(1ASW)}$ and $V_{CC(2ASW)}$) of 5 V is used. If an audio supply of 8 V is used, this pin must not be connected to the 5 V supply voltage. In this case the reference voltage is generated by the IC itself, and only a decoupling capacitor should be connected to this pin.
- Pin $V_{CC(AADC)}$ (pin 77) is the 5 V supply voltage for the audio ADCs. The supply current for this pin is about 23 mA.

12.2 Application diagram



V_{CC5} = 5 V analog supply.

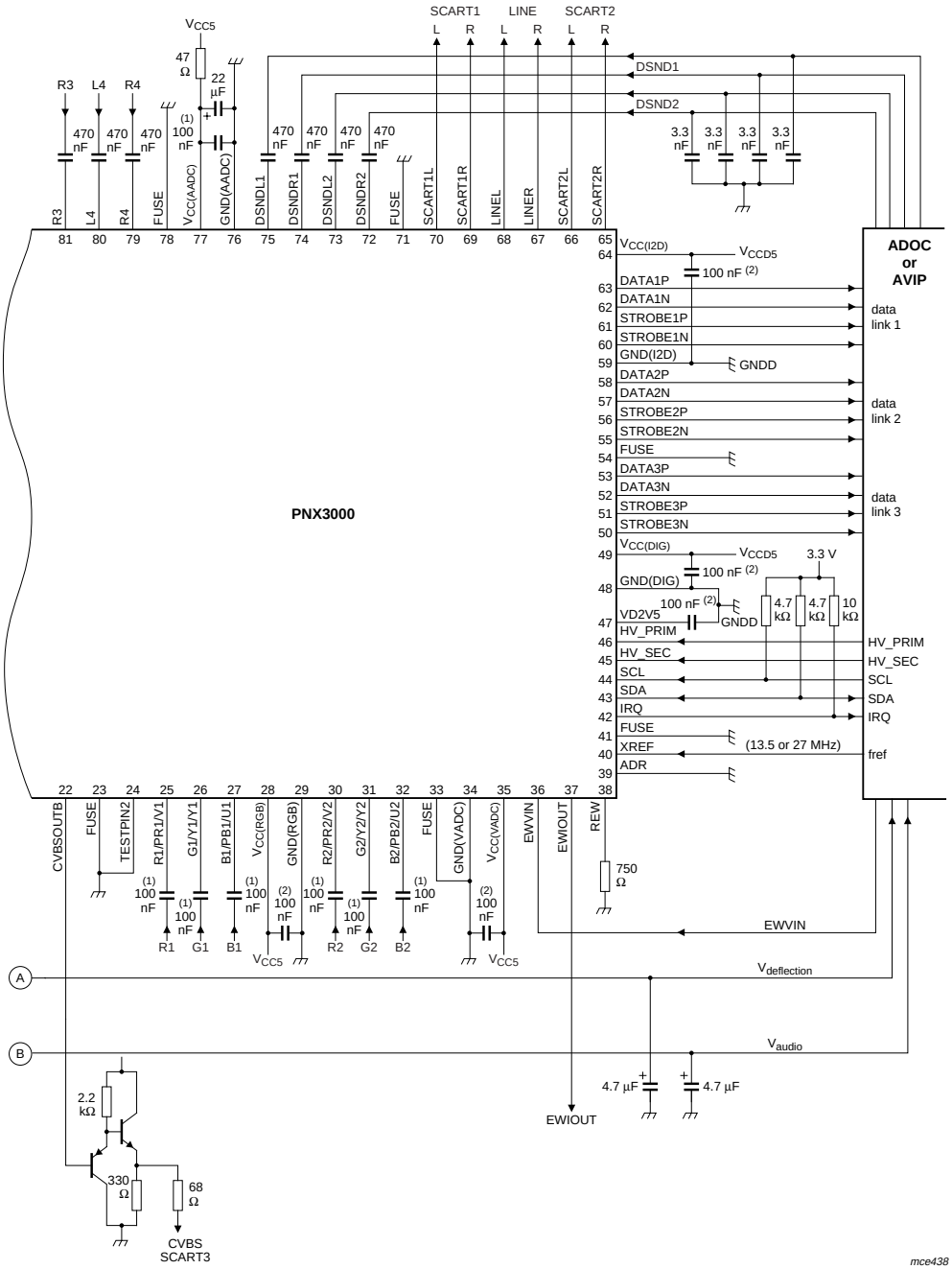
V_{CC_audio} = 5 V or 8 V for audio switch matrix.

(1) foil or ceramic capacitor

(2) ceramic multi-layer capacitor for supply decoupling

(3) This resistor is only used when V_{CC_audio} = 5 V, remove if V_{CC_audio} = 8 V

Fig 11. Application diagram (continued in Figure 12)



V_{CC5} = 5 V analog supply.

V_{CCD5} = 5 V digital supply.

GNDD = digital ground.

(1) foil or ceramic capacitor

(2) ceramic multi-layer capacitor for supply decoupling

Fig 12. Application diagram (continued from Figure 11)

13. Test information

13.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

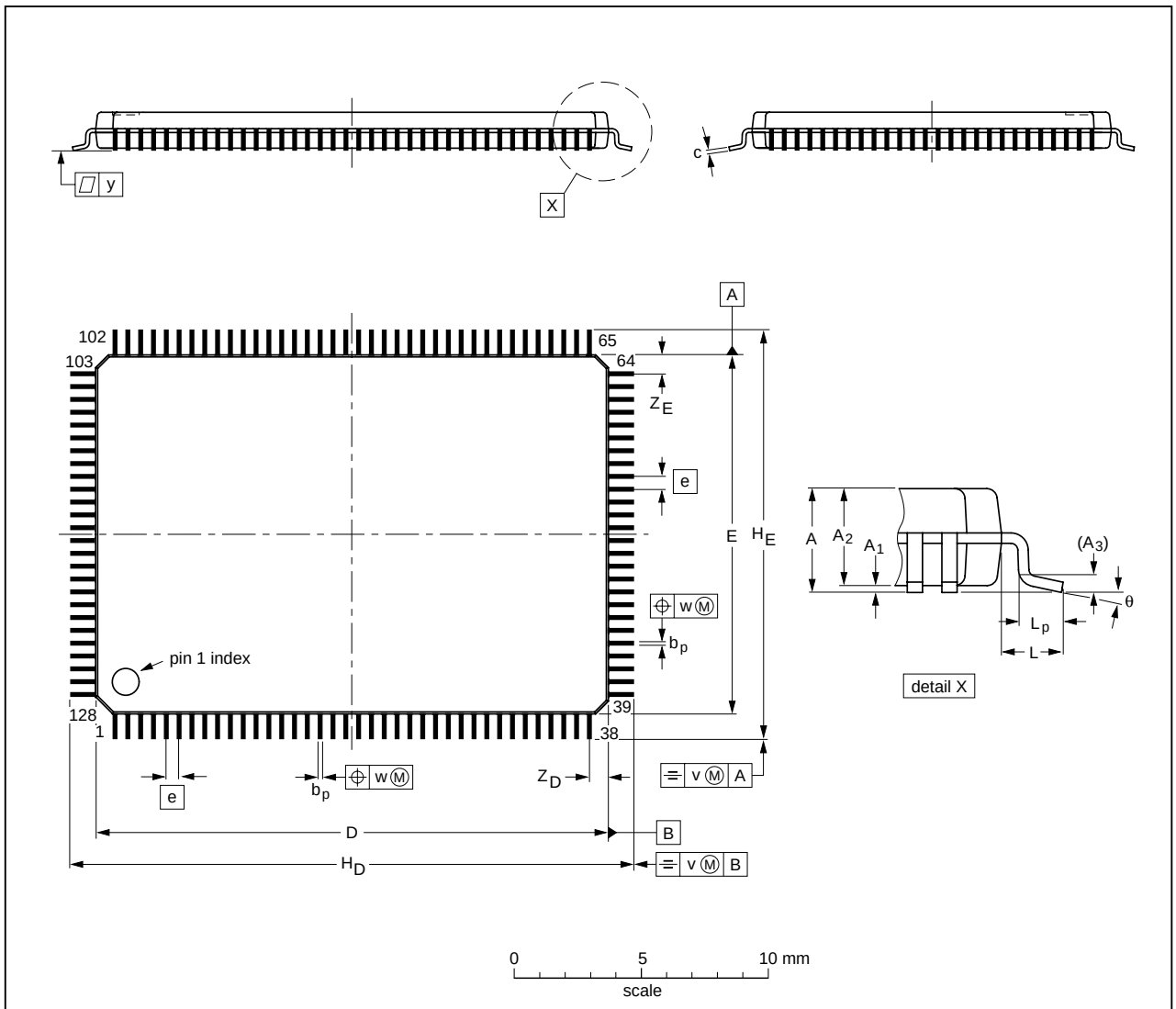
13.2 Latch-up performance

At T_{amb} = 70 °C all pins meet the following specification:

- Positive stress test: $I_{trigger} \geq 100$ mA or $V_{pin} \geq 1.5\ V_{DD(max)}$
- Negative stress test: $I_{trigger} \leq -100$ mA or $V_{pin} \leq -0.5\ V_{DD(max)}$

14. Package outline

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm **SOT425-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1	0.75 0.45	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT425-1	136E28	MS-026				~~00-01-19~~ 03-02-20

Fig 13. Package outline SOT425-1 (LQFP128)

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 80: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Revision history

Table 81: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PNX3000_4	20050329	Product data sheet	-	9397 750 14661	PNX3000_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Changed data sheet status to Product data sheet • Modified Section 11 “Characteristics”: replaced four “tbf” declarations with values • Modified Table 24 “IF PLL offset adjustment”: replaced two “tbf” declarations with “negative correction” and “positive correction”				
PNX3000_3	20041004	Preliminary specification	-	9397 750 14086	PNX3000_2
PNX3000_2	20040624	Preliminary specification	-	9397 750 13372	PNX3000_1
PNX3000_1	20031208	Preliminary specification	-	9397 750 11285	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21. Contents

Date of release: 29 March 2005
Document number: 9397 750 14661

Published in The Netherlands