C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3324 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3324 can regenerate access pauses during redial. During the original entry, only one access pause is stored automatically or several via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3324 is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; > 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3324P: 18-lead DIL; plastic (SOT-102G).
PCD3324D: 18-lead DIL; ceramic (SOT-133).

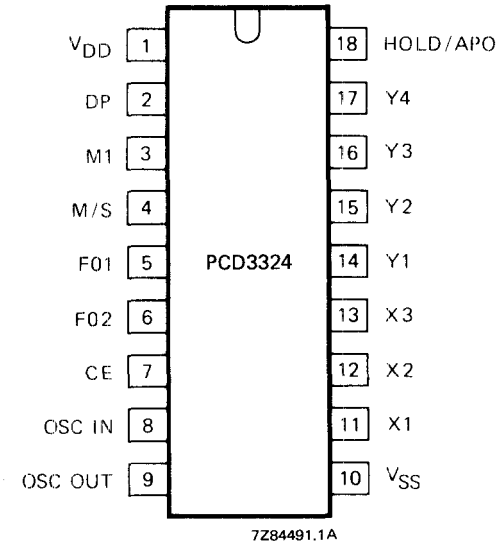


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

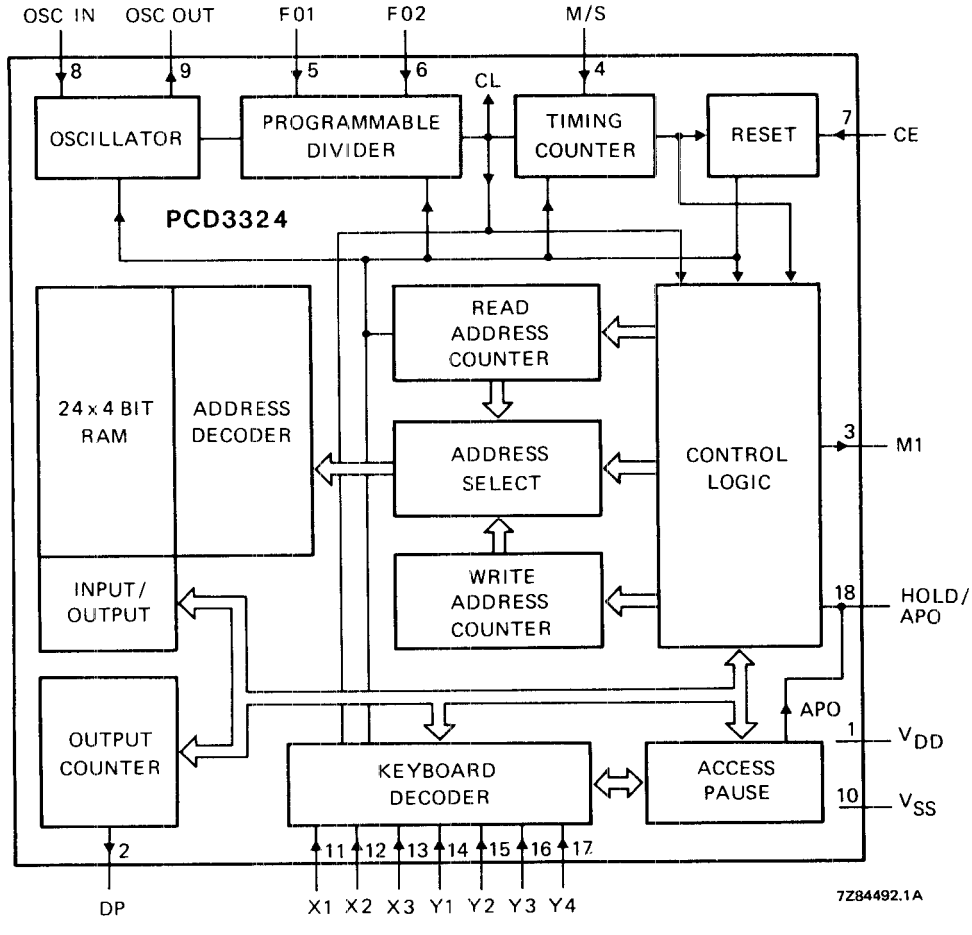


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the **PCD3324** is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

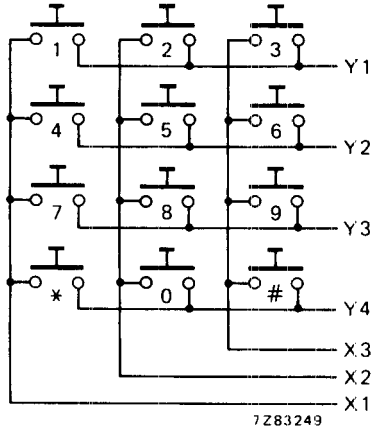
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the **PCD3324.** During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

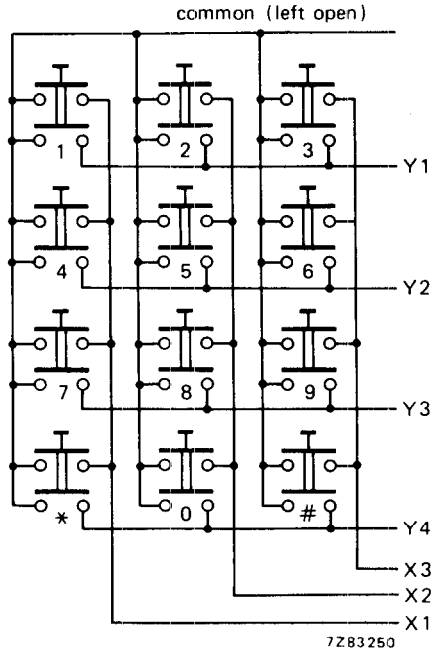


Fig. 4 Double contact keyboard.

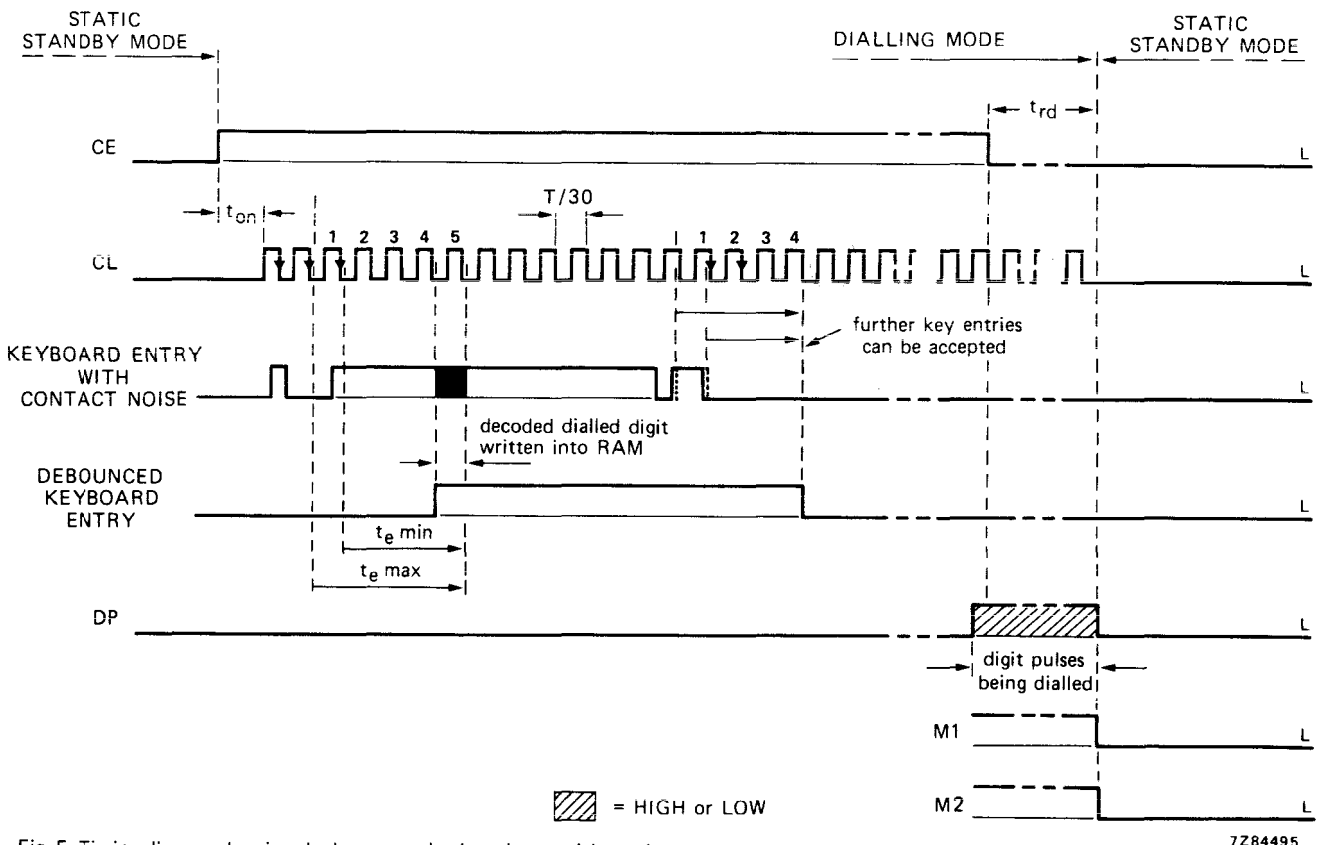


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

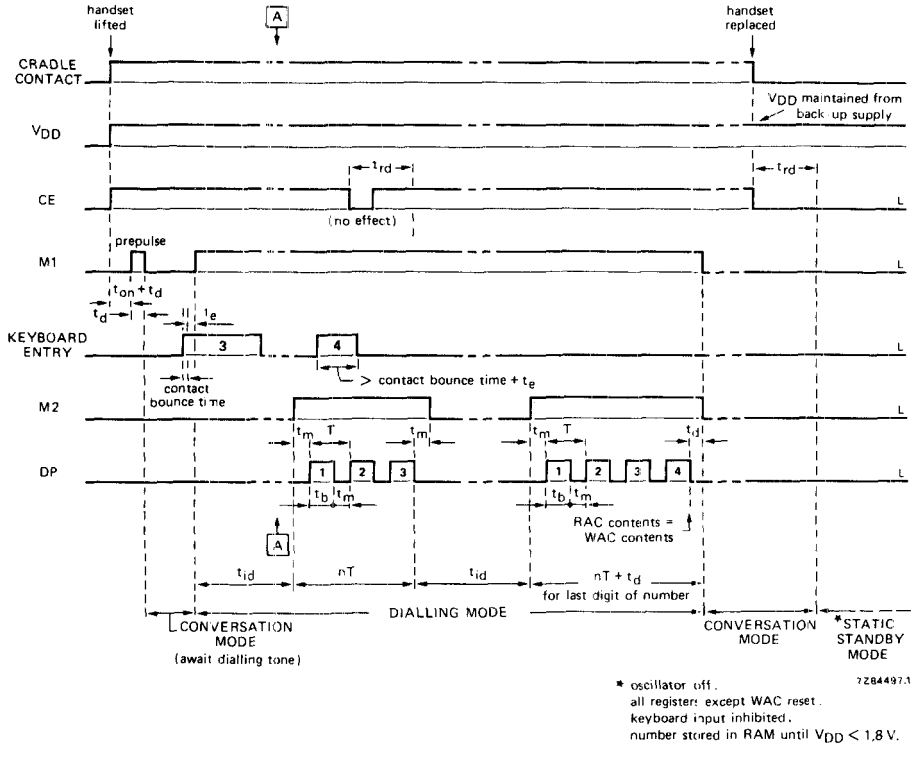


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

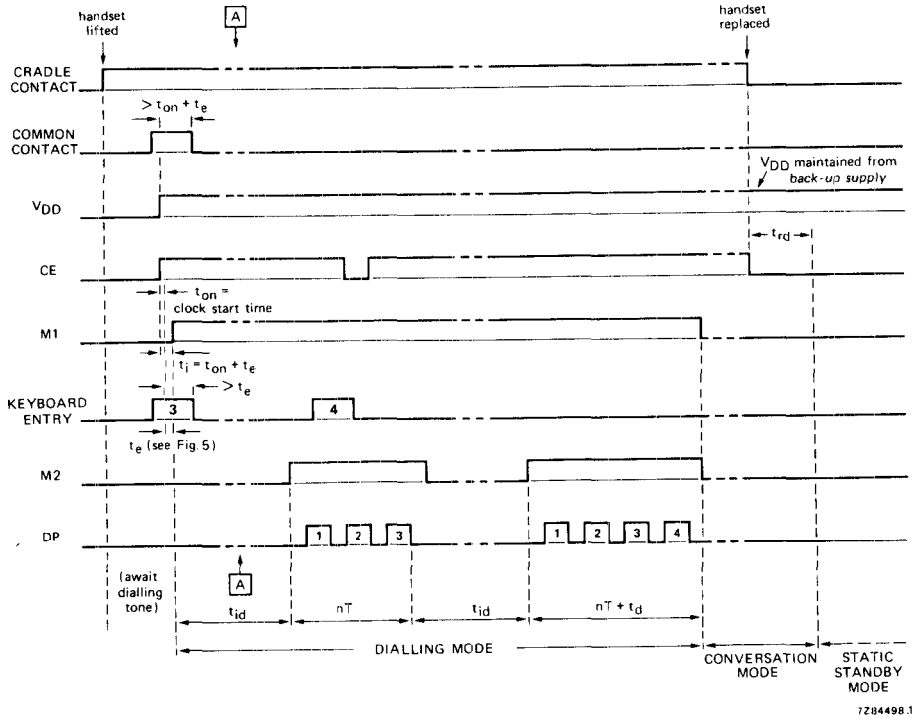


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

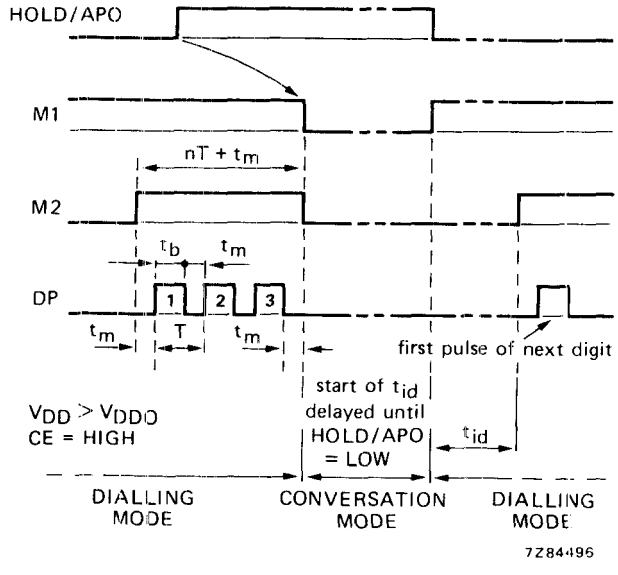


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

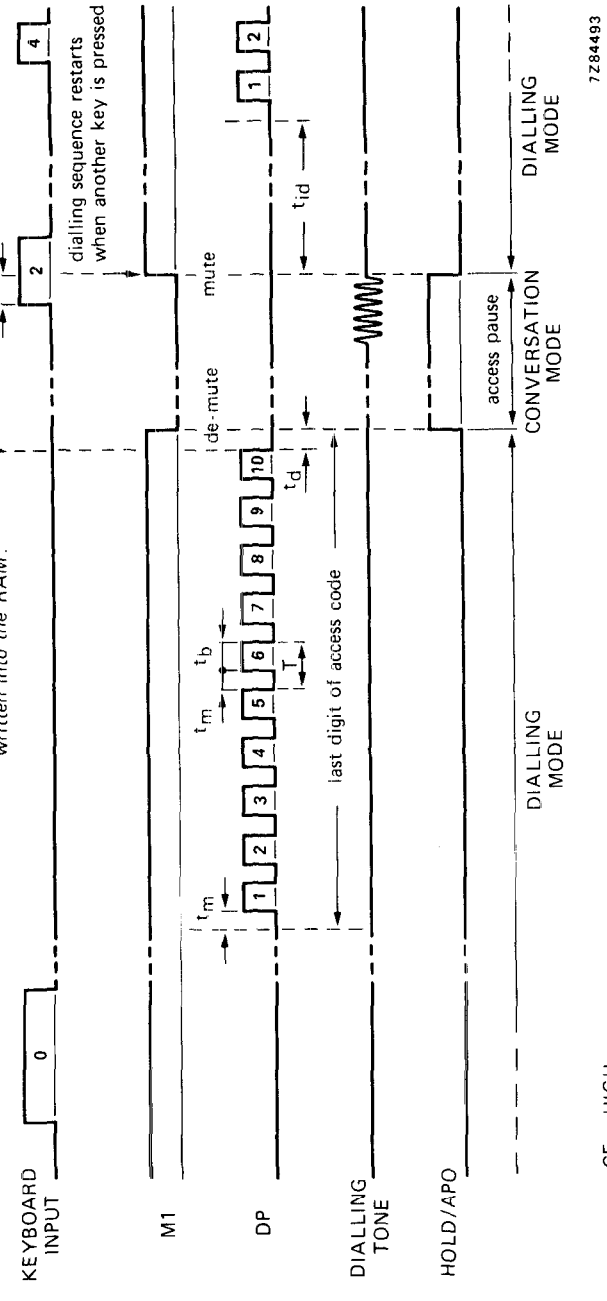
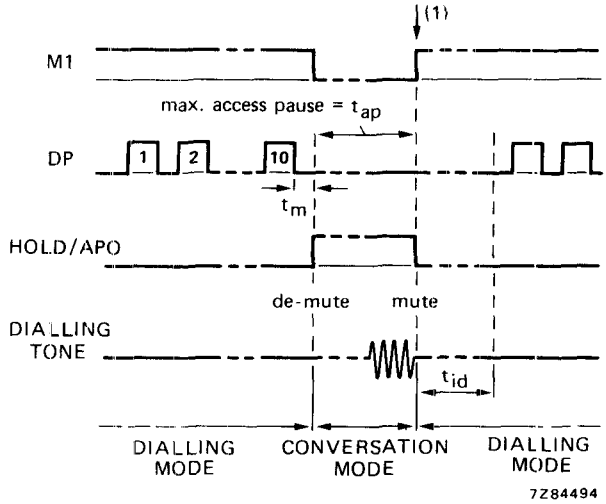


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO)will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Only one access pause can be entered into the RAM in this manner. Alternatively, the access pause key (★) can still be pressed to insert (more) access pauses manually (digits + access pauses $\leqslant 23$).
During redial, access pauses will be automatically regenerated.

Three methods of terminating an access pause:
1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recogniser, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.



(1) a. Access pause (t_{ap}) expires or press redial before end of t_{ap}.

b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW before t_{ap} expires; access pause $< t_{ap}$
HOLD/APO forced to HIGH after t_{ap} expires; access pause $> t_{ap}$.

Fig. 10 Timing diagram showing Access Pause Reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	2	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	$V_I = V_{SS}$
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	$V_I = V_{DD}$
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	$V_I = V_{SS}$

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APC						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 4)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939.2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	—	—	—	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

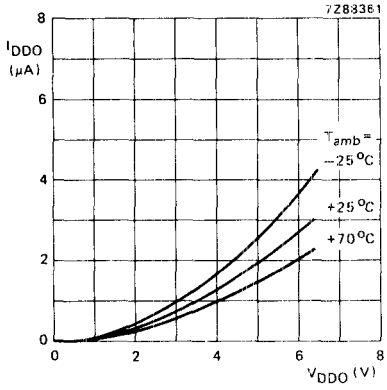


Fig. 11 Standby supply current as a function of standby supply voltage.

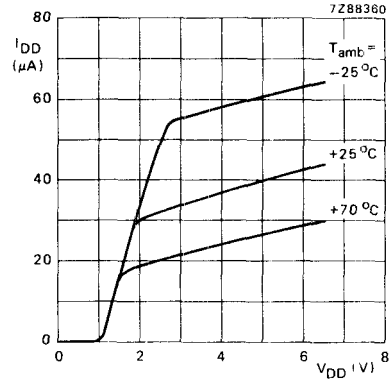


Fig. 12 Operating supply current as a function of operating supply voltage.

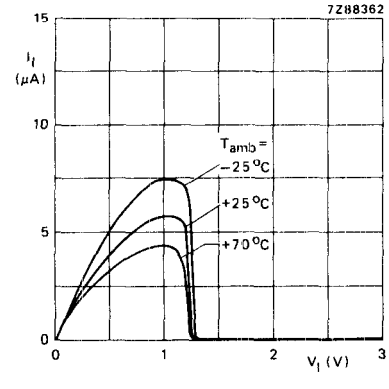


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

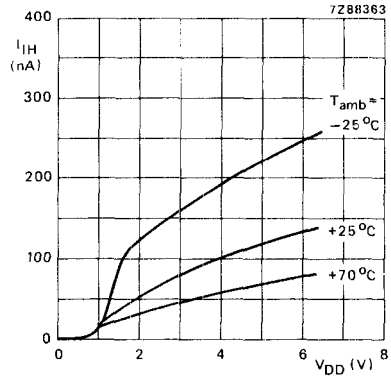


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

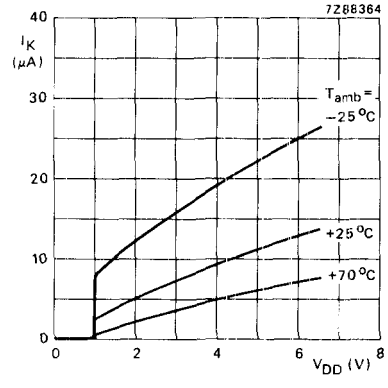


Fig. 15 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

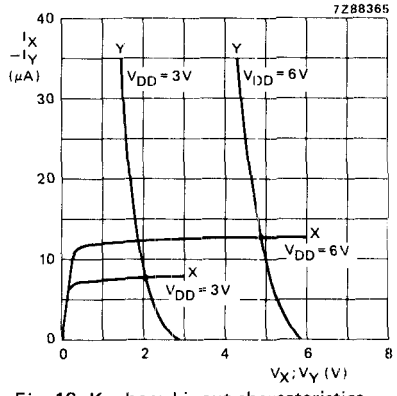


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

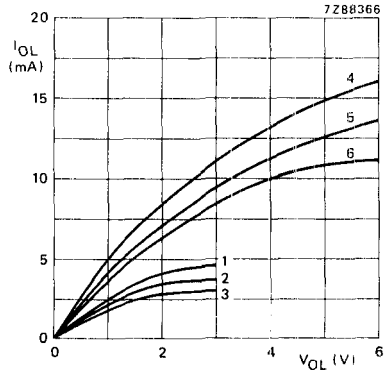


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

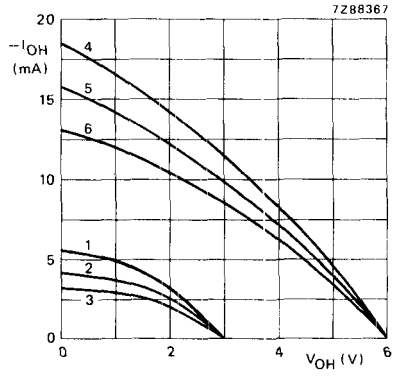
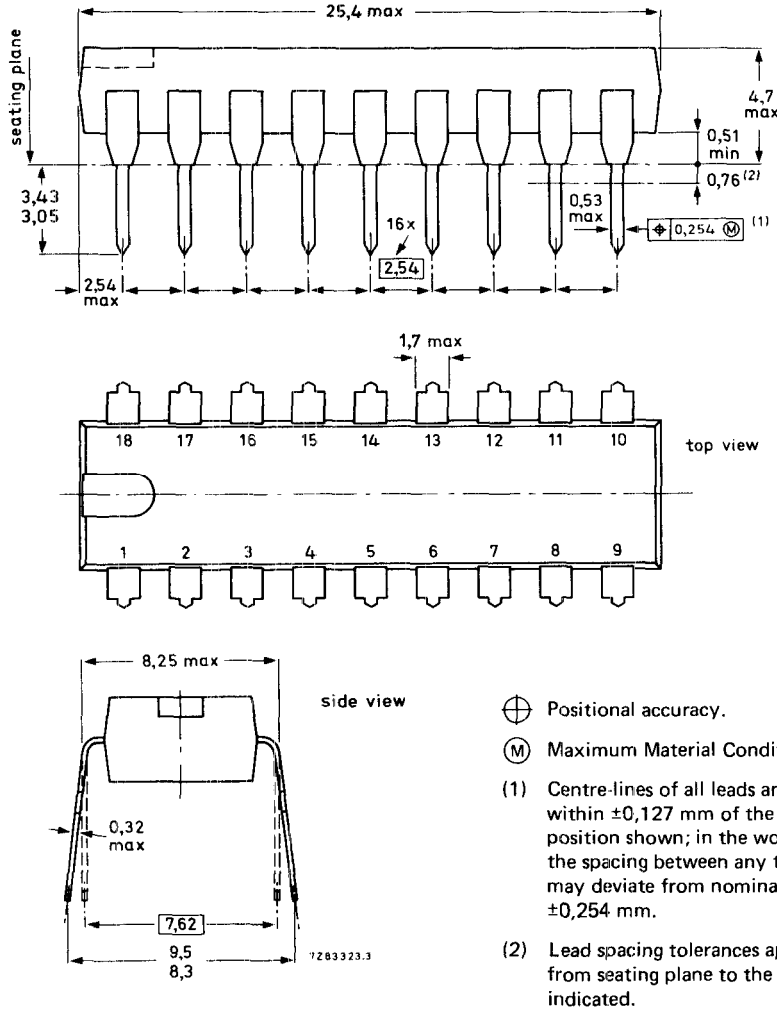


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102G)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

See next page.

SOLDERING

1. **By hand**

   Apply the soldering iron below the seating plane (or not more than 2 mm above it).
   If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

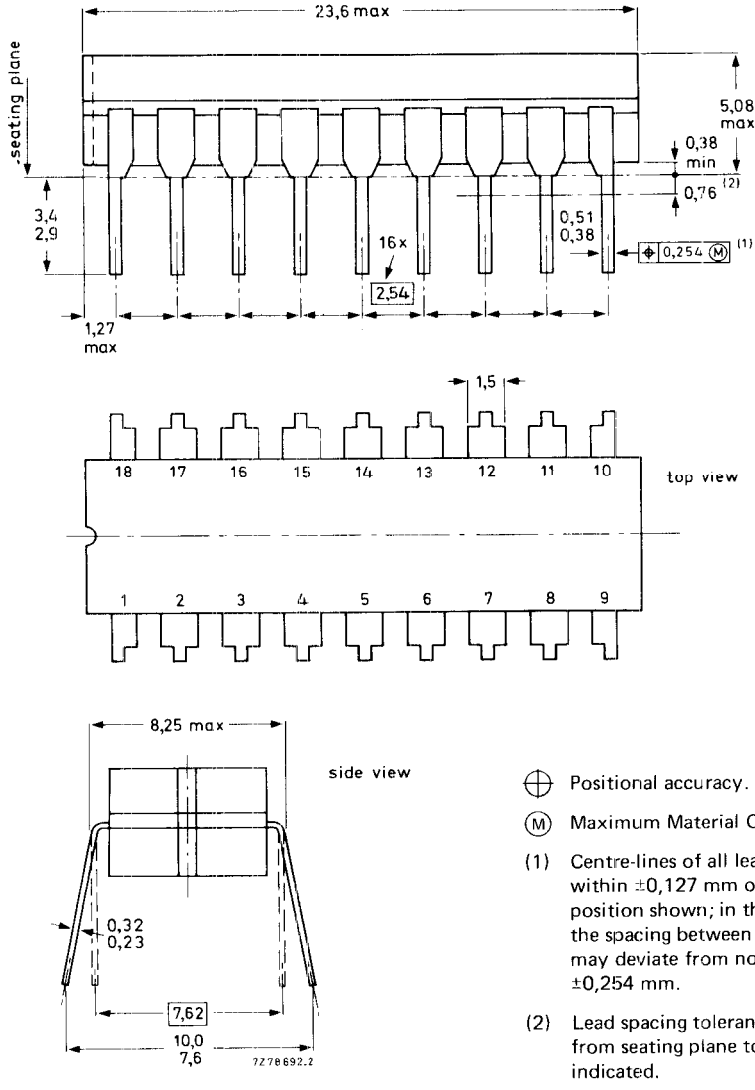
2. **By dip or wave**

   The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-133)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm