DATA SHEET

PCA8510
Standalone OSD

Objective specification
File under Integrated Circuits, IC14

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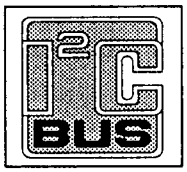
Philips Semiconductors

PHILIPS

CONTENTS



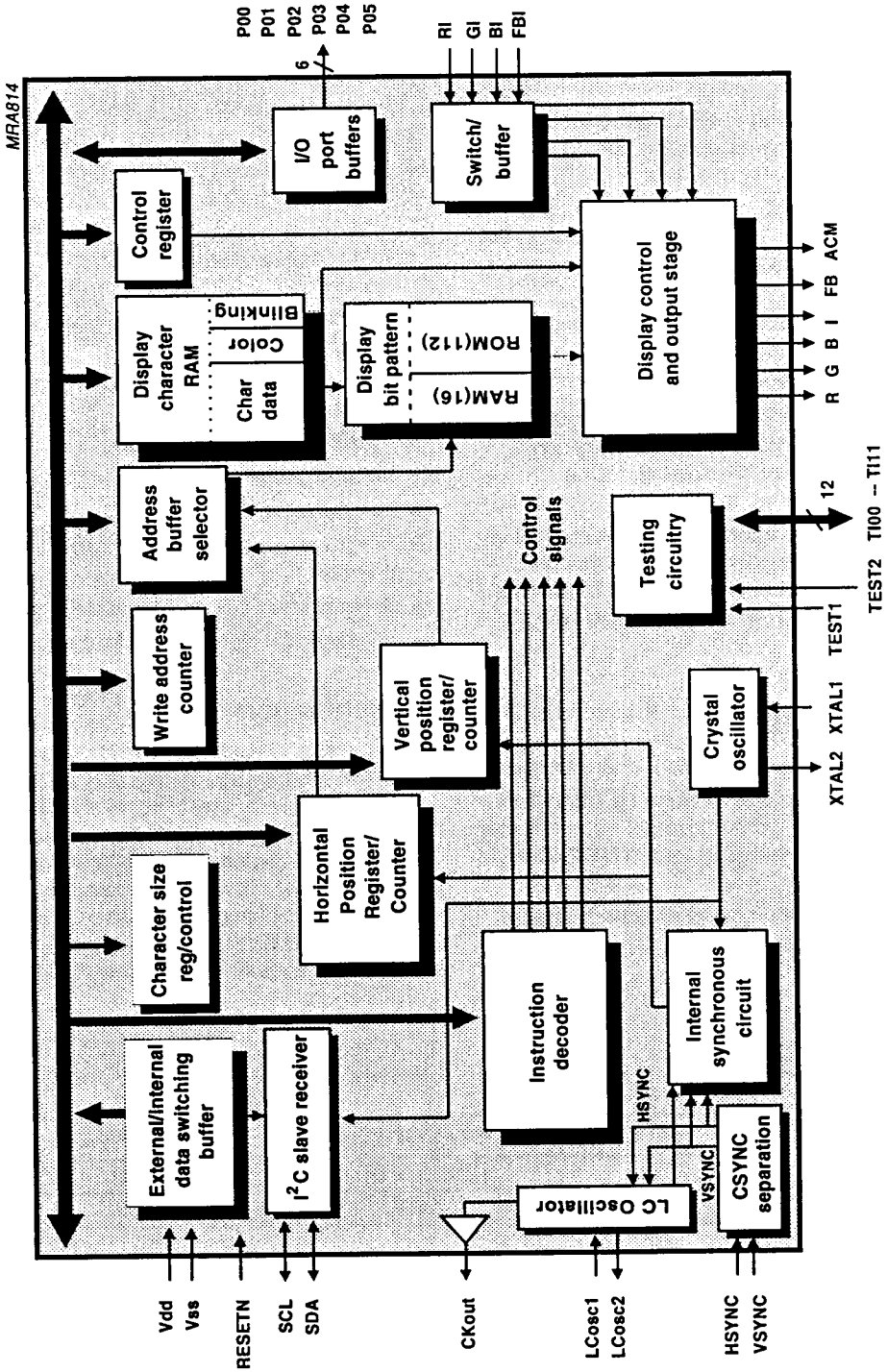


Fig.1 Block diagram.

1 FEATURES

- Display RAM: 192 × 12 bits
- Display character fonts: 112 (fixed in ROM, mask programmable) + 16 (programmable by S/W in RAM)
- Display starting position of the first character: 64 different positions by software control, both in either the vertical and/or horizontal direction
- Character size: 4 different character sizes, on a line-by-line basis, 1 dot = 1H/1V, 2H/2V, 3H/3V, 4H/4V (H = No. of OSD clock period, V: No. of horizontal scan lines)
- Character matrix: 12 × 18 with no spacing between characters and no rounding function
- Foreground colours: 16, combination of Red, Green, Blue and Intensity. Character-by-character basis
- Background/shadowing modes: 4, no background, box shadowing, north-west shadowing, frame shadowing (raster blanking), frame basis
- Background colours: 16, combination of Red, Green, Blue and Intensity, word-by-word basis. Available when background mode is either in "box shadowing" or "north-west shadowing" and "frame shadowing" mode
- OSD oscillator: LC
- Character blinking rate: 1:1, 1:3, 3:1 (frequency: 1/16, 1/32, 1/64 or 1/128 of VSYNC, programmable. e.g. NTSC: 60/16 Hz; PAL: 50/60 Hz etc.), character basis.
- Display format: Flexible display format by using CR (carriage return) code, maximum number of character per line is flexible and depending on the OSD clock (see chapter 9)
- Spacing between lines: 4 different choices from 0, 4, 8, 12 horizontal scan lines
- Display character RAM address-auto-post-increment when writing data
- RAM based character font automatic character address/row address post-increment when writing data
- I²C slave receiver for data/command transfer
- Special scanning mode control to make LPS (1050/60 for NTSC) or 50 Hz to 100 Hz conversion (1250/100 for PAL) possible, feasible for IDTV/EDTV application
- ACM (Active Character Monitor) output special for camcorders application, word basis
- 6 general output port lines, good for microcontroller output expansion
- RGB and fast blanking input for teletext character switch
- Package: 24SDIP or 24SO
- Voltage range 5 V ± 10%
- Temperature range – 80°C – + 70°C
- Programmable HSYNC and VSYNC active input polarity
- Programmable R, G, B, I and FB output polarity
- LC oscillator clock output for frequency fine tuning

2 DESCRIPTION

The PCA8510 standalone OSD chip is a member of the PCF85CXXX CMOS family. It is an on-screen character display generator that is controlled by the microcontroller through I²C-bus. It is for TV or camcorder applications. Special "CR (carriage return)" code makes the display format flexible. Scanning speed control is implemented to make LPS (line progress scan, 1V/2H, for NTSC) and 50 Hz to 100 Hz conversion (2V/2H, for PAL) possible, this also means it can be used in IDTV/EDTV applications.

3 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8510P	24	DIL24SHR	plastic	SOT234
PCA8510T	24	SO24L	plastic	SOT137

4 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
I(VOW3)	1	O	output signal: VOW3 for intensity control
ACM(VOB2)/P04	2	O	active character monitor output (VOB2) or output Port 04 line
TEST1	3	I	testing mode selection, for normal mode operation, TEST1 is GND
TEST2	4	I	testing mode selection, for normal mode operation, TEST2 is GND
RESETN	5	I	master reset (active LOW), normal operation = HIGH
V_{SYNC}	6	I	vertical sync input, active polarity programmable
H_{SYNC}	7	I	horizontal sync input, active polarity programmable
SDA	8	I/O	data line of I²C slave transceiver
SCK	9	I/O	clock line of I²C slave transceiver
XTAL1	10	I	crystal oscillator or resonator for internal operation
XTAL2	11	O	crystal oscillator or resonator for internal operation
V_{SS}	12	I	ground
LC_{OSC2}	13	O	OSD LC oscillator
LC_{OSC1}	14	I	OSD LC oscillator
CK_{OUT}/P05	15	O	buffered LC oscillator output, for fine tuning the frequency/or output Port line 05
R(VOW0)	16	O	character output signal: VOW0, for Red
P00/RI	17	I/O	general purpose output Port 00 or colour R input (e.g. teletext)
G(VOW1)	18	O	character output signal: VOW1, for Green
P01/GI	19	I/O	general purpose output Port 01 or colour G input (e.g. teletext)
B(VOW2)	20	O	character output signal: VOW2 for Blue
P02/BI	21	I/O	general purpose output Port 02 or colour B input (e.g. teletext)
FB(VOB)	22	O	fast blanking output (VOB)
P03/FBI	23	I/O	general purpose output Port 03 or Fast blank for switching RGB source input (e.g. teletext)
V_{DD}	24	I	V_{DD} power supply

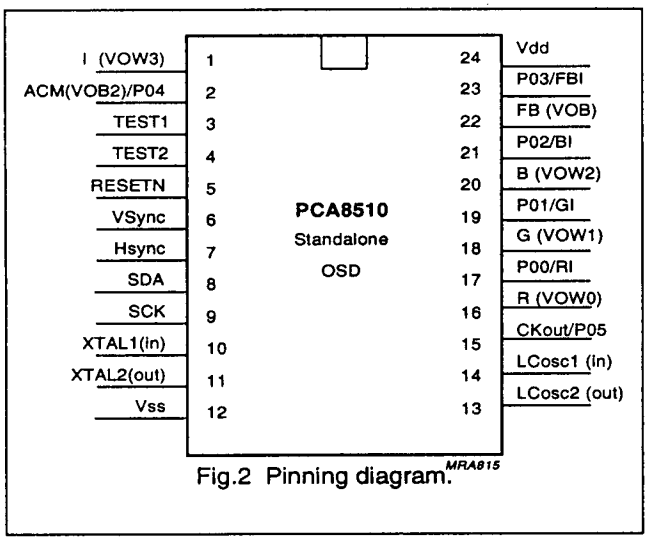


Fig.2 Pinning diagram.

5 I²C SLAVE RECEIVER

The I²C slave receiver is implemented for data to be transferred between either CPU or microcontroller and the standalone OSD chip.

The I²C slave address is "1011 101". As in the normal mode of operation the PCA8510 is "write only" from the master I²C, the last bit of the slave address is always 0. It is only in test mode that the last bit is 1.

The commands to control different functions of this chip are shown in Table.1. The details are given in the following chapters. The control command stream sent through the I²C-bus is shown in Fig.3, the first byte is the slave address and from the second byte onwards, all recognized types of commands can be transferred. A STOP condition is required to complete the data transfer. An acknowledge bit is sent upon successful reception of

a complete slave address/data byte in the shift register. The I²C slave receiver is reset to its initial state, which is to wait for slave address call under the following conditions.

- after master reset
- after the I²C-bus is out of control by uncompleted bus protocol. (e.g. bus error)

The data in the I²C shift register is then abandoned.

Table 1 Standalone OSD command overview.

COMMAND		(1) BS	MSB							LSB
			(2) 7	6	5	4	3	2	1	0
0	Command bank selection	X	0	1	1	1	1	0	0	(1) BS
1	Display character	0	1	C6	C5	C4	C3	C2	C1	C0
2	Attribute	0	0	0	0	T4	T3	T2	T1	T0
3	Display character address H	0	0	0	1	0	A7	A6	A5	A4
4	Display character address L	0	0	0	1	1	A3	A2	A1	A0
5	DFR bit pattern (DFRDR)	1	0	0	P5	P4	P3	P2	P1	P0
6	DFR character address (DFRAR)	1	1	0	0	0	CA3	CA2	CA1	CA0
7	Control register 1	1	0	1	0	0	M1	M0	Bp	EN
8	Control register 2	1	0	1	0	1	Hp	Vp	S1	S0
9	Control register 3	1	0	1	1	0	BF1	BF0	BR1	BR0
A	Control register 4	1	0	1	1	1	0	A/P	C/S	P/I
B	Vertical start position H	1	1	0	0	1	V5	V4	V3	V2
C	Vertical position L/Horizontal position H	1	1	0	1	0	V1	V0	H5	H4
D	Horizontal start position L	1	1	0	1	1	H3	H2	H1	H0
E	Port 0 value (write)	1	1	1	O5	O4	O3	02	01	O0
F	Background colour in frame shadowing mode (control register 5)	0	0	1	0	0	R	G	B	I

Notes

1. BS Bit = Bank Selection
2. Bit (7 - 0) = I²C data byte contents

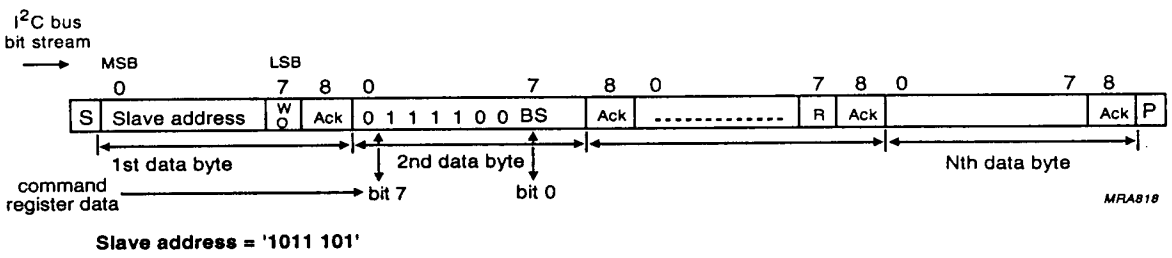


Fig.3 I²C write timing diagram – data stream (an example).

6 DISPLAY CHARACTER FONTS ORGANIZATION

The fonts are organized as 112 in ROM which is metal (IN) mask programmable in diffusion phase and 16 in RAM which is alterable (i.e. soft fonts) in run time.
A character is composed of 12 × 18 dots which can be used to display a semigraphic pattern, kanji, hiragana or even Chinese characters. With no spacing between characters on the same row and the space between two rows being programmable to 0 horizontal lines makes even higher resolution characters possible.

The character font stored in the PCA8510 is in 12 x 19 format in which the row 1 to 18 is the visible dots on the screen. The row 0 is for the combination of two characters in a vertical direction when north-west shadowing mode is selected (see section 8.3 and Figs.28, 29 and 30).

6.1 Display Fonts in RAM (DFR) – soft font

There are 16 (chars) x 12 (column) x 19 (row) bits of RAM available for storing character fonts which are subject to change from application to application. Users can switch the display patterns in and out according to different condition meant in the application.
Except the basic 112 fonts in ROM, customized pattern can be implemented easily through loading the Display Fonts RAM with bit patterns. Also during the development phase, users can emulate the character set by this DFR function (thus no EPROM or OTP version is needed for emulation purpose).

6.2 How to load bit pattern into DFR

There are two steps to initialize the DFR:

1. to initialize the address of the character within the 16 RAM locations
2. then to load the bit patterns to the RAM locations.

In the first step, three special register are for DFR control: DFR address register (DFRAR), DFR row register (DFRRR) and DFR data register (DFRDR). But DFRRR is transparent to the user. Table.2 shows the register configuration.

DFRAR (3:0) is to determine the Nth (0-15) character in the DFR, see Fig.4.
DFRRR (5:1) is to determine the Nth (0-18) row in this character.
DFRRR (0) is to determine the first 6-bit pattern or the second 6-bit pattern of that row.

Command 6 (see Table.1) is to configure the DFRAR.

When the DFRAR is loaded with new data via the I²C-bus, DFRRR is reset to zero internally by hardware to point to the start of this particular soft font. Fig.4 shows the character matrix organization.

In the second step, one special register, DFRDR, DFR data register (see Table.2), is used as an intermediate buffer which takes the data loaded via the I²C and transfers to the RAM location pointed to by the DFRAR and DFRRR.

Table 2 Registers for DFR control.

DFR Register	(MSB) 7	6	5	4	3	2	1	(LSB) 0
DFR address register (DFRAR)	reserved (0000)				CA3	CA2	CA1	CA0
DFR row address (DFRRR) <transparent to the user>	reserved (00)		R4	R3	R2	R1	R0	U/L
DFR data register (DFRDR)	reserved (00)		P5	P4	P3	P2	P1	P0

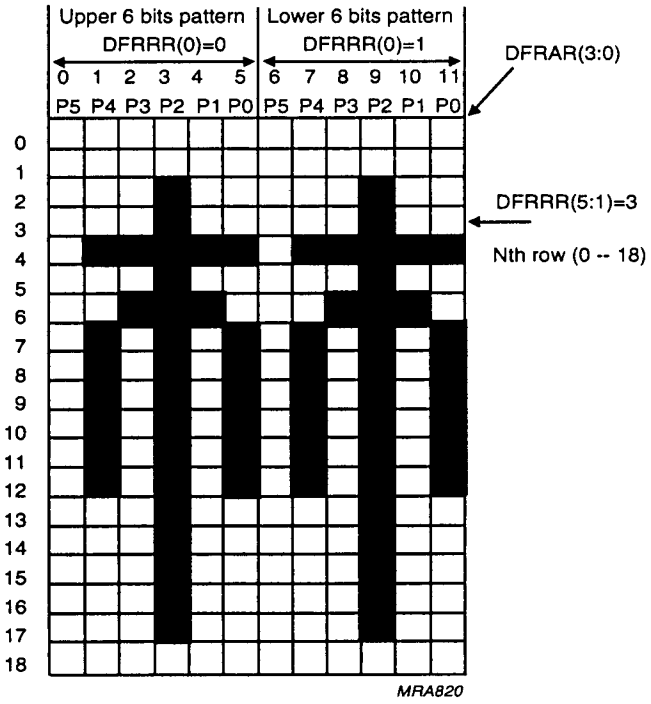
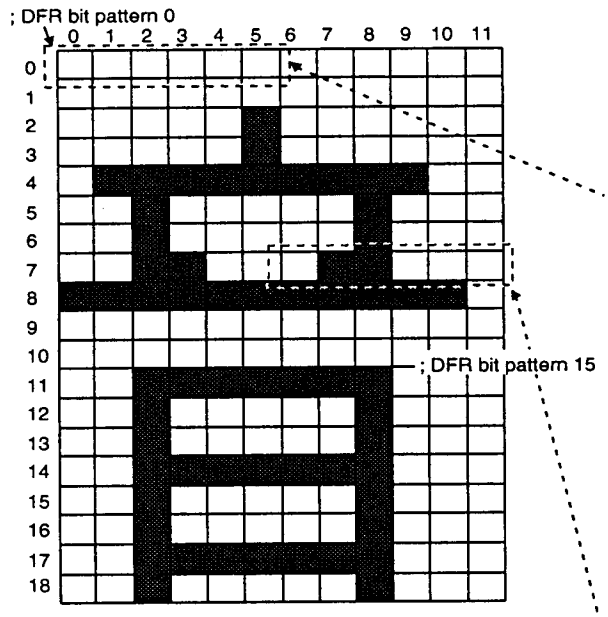


Fig.4 Character Font Dot Matrix Organization.



I^2C Start condition

Byte #1 :	1011 1010	;slave address call (write to slave I^2C)
Byte #2 :	0111 1001	;configurate BS=1
Byte #3 :	1000 0000	;reset DFR character address to 0, DFRAR=0
Byte #4 :	0000 0000	; DFR bit pattern 0
Byte #5 :	0000 0000	; DFR bit pattern 1
Byte #6 :	0000 0000	; DFR bit pattern 2
Byte #7 :	0000 0000	; DFR bit pattern 3
Byte #8 :	0000 0001	; DFR bit pattern 4
Byte #9 :	0000 0000	; DFR bit pattern 5
Byte #10 :	0000 0001	; DFR bit pattern 6
Byte #11 :	0000 0000	; DFR bit pattern 7
Byte #12 :	0001 1111	; DFR bit pattern 8
Byte #13 :	0011 1100	; DFR bit pattern 9
Byte #14 :	0000 1000	; DFR bit pattern 10
Byte #15 :	0000 1000	; DFR bit pattern 11
Byte #16 :	0000 1000	; DFR bit pattern 12
Byte #17 :	0000 1000	; DFR bit pattern 13
Byte #18 :	0000 1100	; DFR bit pattern 14
Byte #19 :	0001 1000	; DFR bit pattern 15
Byte #20 :	0011 1111	; DFR bit pattern 16

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Fig.5 Character font in RAM - I^2C data stream.

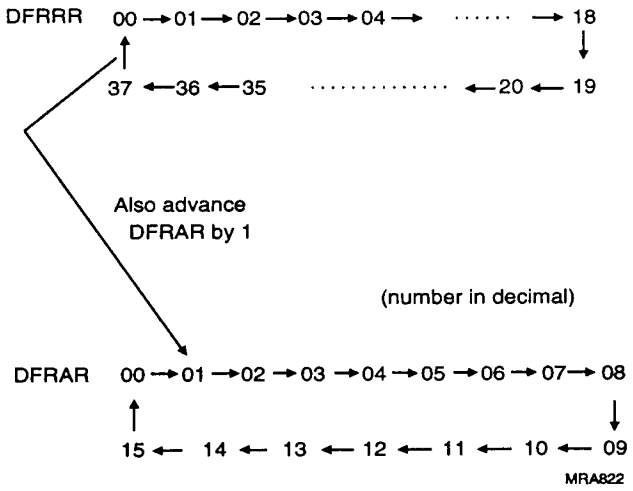


Fig.6 DFRRR and DRFAR increment cycle.

Command 5 (see Table.1) is the bit pattern of the character which is in the display font RAM and is pointed to by the DFRAR and DFRRR.

The bit pattern is loaded after the full byte is received. Then a post increment operation is performed automatically which advances the DFRRR and/or DFRAR by 1.

Fig.5 shows an example of I²C-bus bit stream to configure the font stored in DFR address 0.

Fig.6 shows how DFRAR and DFRRR are incremented and advanced. Overflow of the post-increment makes the registers reset to ZERO.

Initial value (after master reset) of DFRAR, DFRRR and DFRDR is all ZERO.

6.3 Display character fonts address

Fig.7 shows the address map of the display character font in RAM and ROM.

6.4 Display character font in ROM

The character ROM is actually divided into two parts ROM1 and ROM2.

The bit pattern stored in ROM1 and ROM2 is shown in Fig.8.

Row 0 is for use only in the north-west shadowing mode (details see section 8.2 command 8). It is when two character cells are combined in the vertical direction to formulate a new pattern, this row 0 contains the same bit pattern of row 18 of the character above it.

If no combined character in the vertical direction is intended for this character, row 0 should be filled in with all "0's".

The file format to submit to Philips to make customized character sets is also demonstrated in Fig.8. Philips provides software using the MS–DOS environment (IBM/PC) to aid custom design of the character font on the screen and to generate the bit pattern HEX file automatically.

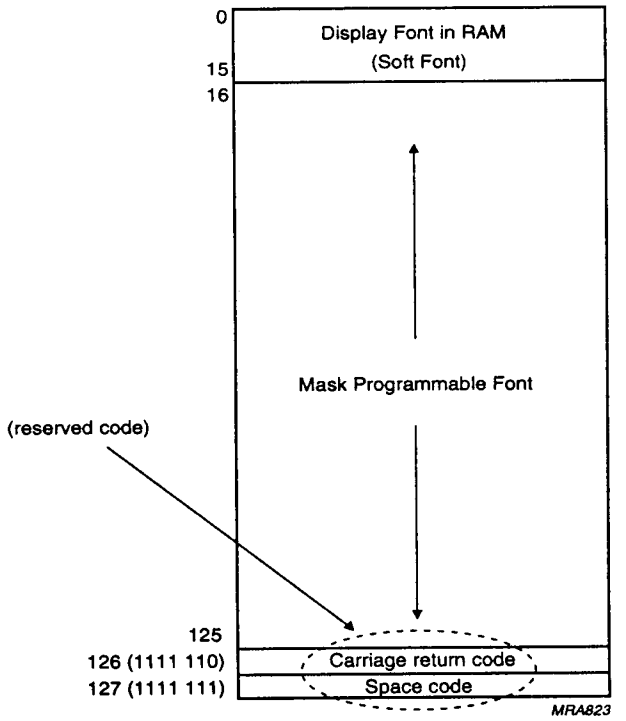
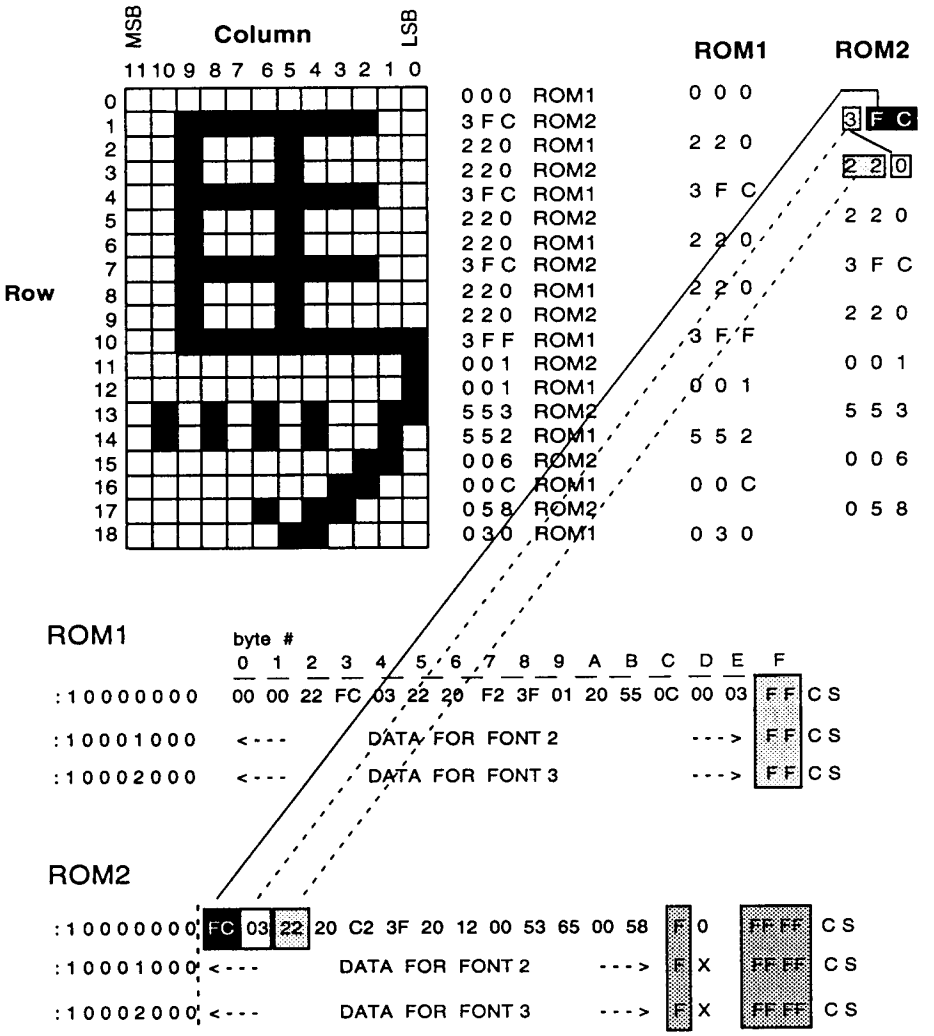


Fig.7 Display character font address map.



Note:

1. The row 0 of each font is reserved for vertical combination of fonts.
2. In vertical mergence, the row 0 of lower font has same code with the row 18th of upper font.
3. Binary "1" stands for dots in PCA8510 and "0" for blank
4. The ROM1 and ROM2 data files are in INTEL hex format with byte basis. Each byte is structured with higher nibble followed by lower nibble .
5. The remaining codes of 16 bytes for one font of ROM1/ROM2 must be filled with " F ".
6. CS stands for checksum.

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Fig.8 Font pattern stored in character ROM1 and ROM2.

Table 3 Display RAM organization overview.

11	10	9	8	7	6	5	4	3	2	1	0
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T0
Customer character data							R G B I foreground colour				Blink
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T0
Space Code (1111111)							R G B I background colour				ACM
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T0
Carriage Return (1111110)							Char Size		Line Space		End

Table 4 Colour table and blinking control.

T4	T3	T2	T1	T0
R	G	B	I (note 1)	blink (note 2)
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Notes

1. "I" stands for Intensity, the fourth output pin to control colour intensity.
2. 0: no blinking of this character
   1: blinking of this character at the frequency of VSync/16, VSync/32, VSync/64 or VSync/128 rate

7 DISPLAY RAM ORGANIZATION

The display character RAM is organized as 192 x 12 bits. See Table.3 for details. Bit < 11:5 > is the character data which determines 1 out of 128 different fonts (126 customized + 2 reserved code, i.e. carriage return code and space code). Bit < 4:0 > contains the attribute like colours etc. of this character font.

7.1 Bits in the Display RAM

There are three different types of bit < 11:5 > configurations to be considered:

1. When bit < 11:5 > indicates a **customized character,** bit < 4:1 > determines the colour (1 out of 16) of this character. Blinking of this character is controlled by bit < 0 >.

   Table.4 gives the colour and blinking control.

2. **Carriage return code** (bit < 11:5 > = 1111110) is a special code that will finish the current display line, and start to display the character next to this code in the beginning of next line (row) with a spacing between lines (rows) defined by bit < 2:1 >.

Table 5 Attribute for carriage return code character size of next row and Line spacing.

T4	T3	size	T2	T1	line spacing between rows	T0	end of display control
0	0	1 dot = 1H/1V	0	0	0H line	0	continue display of next character
0	1	1 dot = 2H/2V	0	1	4H line	1	end of display
1	0	1 dot = 3H/3V	1	0	8H line		
1	1	1 dot = 4H/4V	1	1	12H line		

It displays a transparent pattern on the screen.

Character size of the next line is determined by bit < 4:3 >. 1 dot equals to 1H/1V, 2H/2V, 3H/3V or 4H/4V. (H: OSD clock, V: horizontal scan line)

Bit < 2:1 > determines the number of horizontal lines in between two character rows.
Bit < 0 > is the "end of display" bit which is to indicate the end of the display for the current screen, before display RAM location 192. Table.5 gives the details.

The LC oscillator starts to oscillate when the vertical starting position controlled by the command B, C (see chapter 8.1) is matched and HSYNC is inactive. It stops if one of the following conditions was met: (see Fig.9)

- CR code is met at the end of each line
- end of display bit met
- space between character lines
- exhaustion of RAM location 192

In order to save power consumption (e.g. portable application like camcorder) and reduce the radiation, users are recommended to set the end of the display bit to stop the LC oscillator whenever needed.

3. **Space code** is a code which displays a transparent pattern on the screen and lasts for 1 character width. When the bit < 11:5 > = 1111 111, bit < 4:1 > determines the background colour of the characters/words **from** this space code in "box shadowing" and/or "north-west shadowing" modes (see section 8.2 for details).

Bit < 0 > is the ACM (Active Characters Monitor) control which, when enabled (= 1), will make the ACM pin active during the display of the characters following the space code, and will return to inactive only after the next space code which disables the ACM bit.

Table.6 gives the details and Fig.10 illustrates an example of the timing of ACM, FB and R, G, B, I pins when displaying a line of dots stream in characters.

Table 6 Attribute for space code – Background colour and ACM control.

T4	T3	T2	T1	T0
R	G	B	I (note 1)	(note 2)
0	0	0	0	
0	0	0	0	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Notes

1. "I" stands for Intensity, the fourth output pin to control colour intensity.
2. ACM active control
   0: inactive (ACM pin = LOW)
   1: active (ACM pin = HIGH)

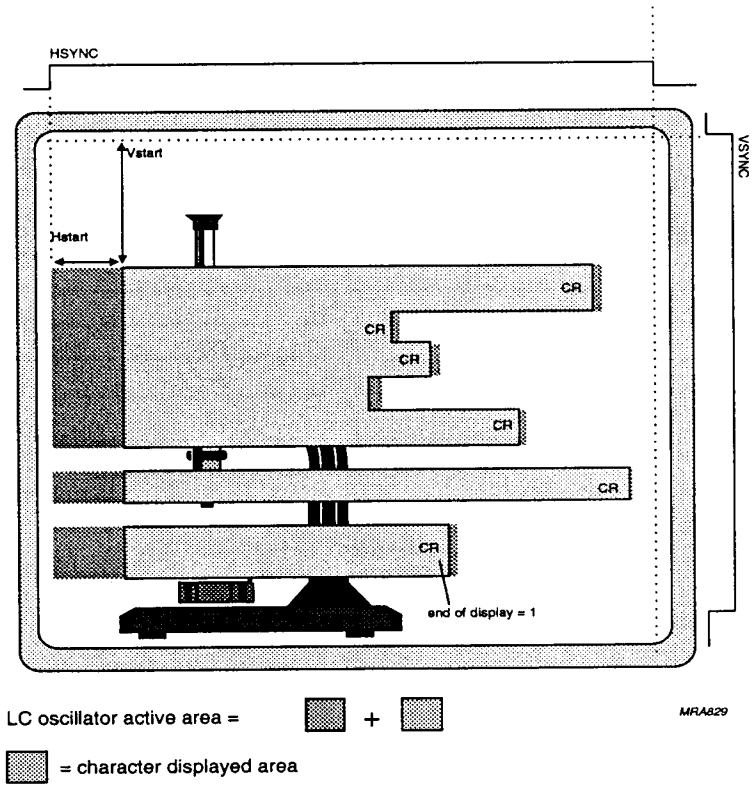
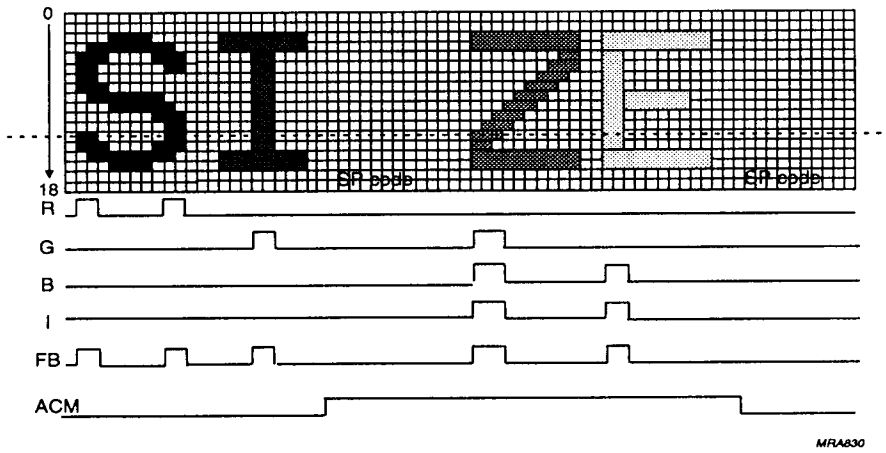


Fig.9 LC oscillator active period.



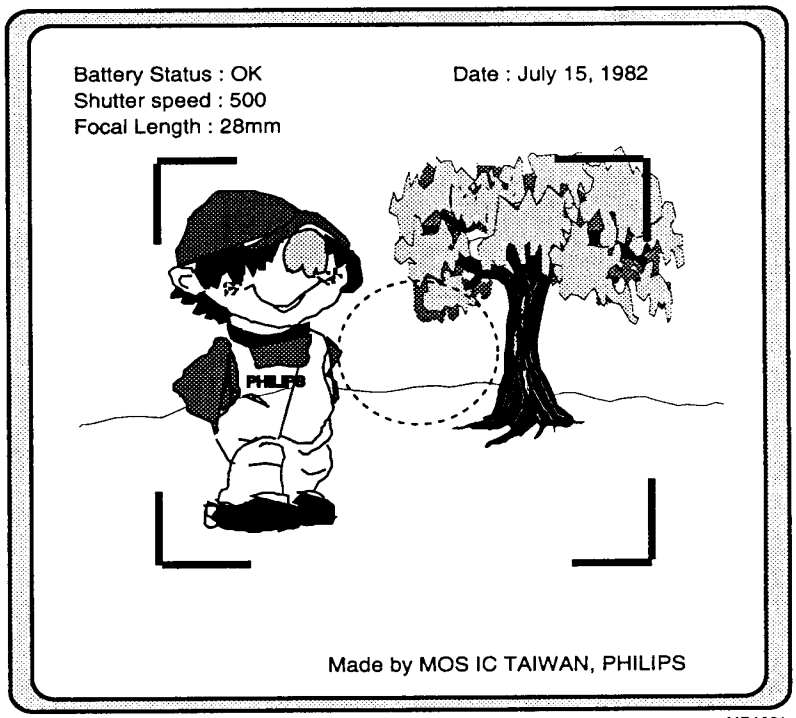
"S" : red color
"I" : green color
"Z" : G+B+I color
"E" : B+I color
1st SP code : ACM = on
2nd SP code : ACM = off

Fig.10 R, G, B, and FB timing.

The ACM signal is for camcorder applications, when some part of the characters are to be recorded on the tape and displayed on the screen, (i.e. Date/Time) while some others (i.e. Battery status = OK) are only to be displayed on the screen. Fig.11 gives an example.

Fig.12 shows an example of the screen which includes some CR and SPACE code in.
In summary

1. Carriage return code is used to control
   - character size of next line
   - space (in terms of number of horizontal lines) between current character line and next line
   - end of display to stop the LC oscillator upto next match of vertical starting address.
2. Space code is to control
   - the background colour of the characters **from** this space code
   - ACM active/inactive from this space code.
3. Display of the characters from RAM address 0 always. Space and carriage return code is to change the attribute and the position of the characters. The last character displayed on the TV screen is either the RAM location 192 or a CR code with "end of display" attribute set to one.



In this example, all the characters are displayed on the viewfinder.
But only the data of "Date : July 15, 1992 is to be recorded onto the tape, so only these characters' ACM attribute bit equal to 1

Fig.11 Example of ACM signal used in the camcorder application.

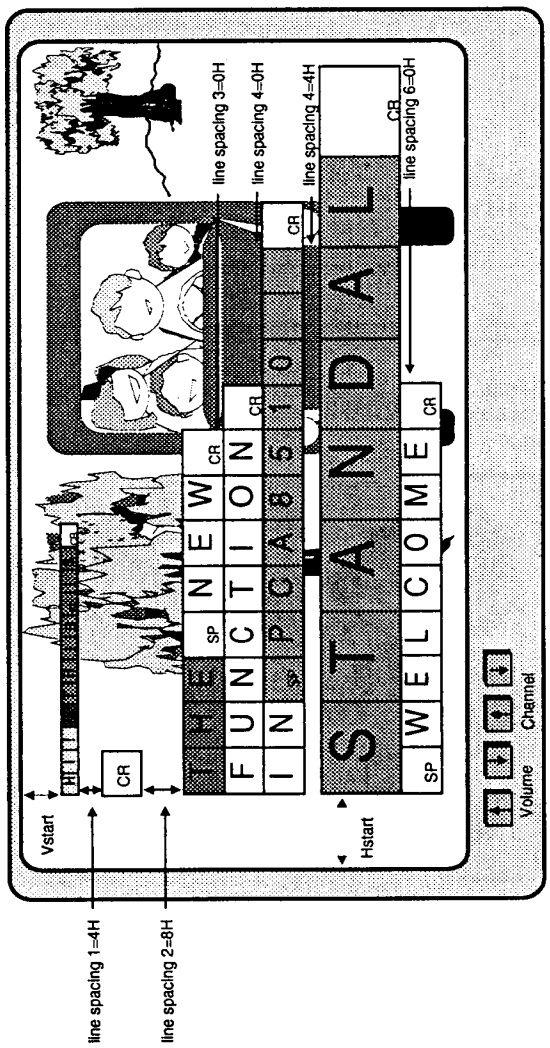


Fig.12 On screen display (an example)

Table 7 Control register for display characters.

Register	7	6	5	4	3	2	1	0
DCR Address register (DCRAR)	A7	A6	A5	A4	A3	A2	A1	A0
DCR Attribute register (DCRTR)	reserved			T4	T3	T2	T1	T0
DCR Character register (DCRCR)	–	C6	C5	C4	C3	C2	C1	C0

7.2 How to load the character data into the display RAM

There are 3 registers to control, address and buffer the display characters.

DCRAR (7:0) is the address register which points to the location of the display RAM for which data is to be written into. The data loaded by command 3 and 4 is stored here.
DCRTR (4:0) is the attribute register which stores the data of command 2.
DCRCR (6:0) is the data register to store the character loaded by command 1 which is going to be loaded into the RAM location pointed to by DCRAR.

Table.7 shows the configuration of these three registers. See also Table.1 for command list.

The method used to write display characters into the display RAM, is similar to writing the bit pattern into the display fonts RAM. Post increment operation of the address counter/register is performed when a character is loaded into the current location pointed by the DCRAR.

Here is the detail:

Step 1. Command 3 and 4 initialize the address of the RAM (one out of 192, i.e. 0 -- 191) and is stored in the DCRAR.

Step 2. Command 2 is to determine the attribute of the character. The meaning of these 5 bits is dependent of the contents of the command 1 (i.e. carriage return code, space code or normal user's code, see section 7.1 for details).

Step 3. Command 1 is the character code to be displayed on screen. When the complete command byte is received, the data which is stored within the DCRTR and this command 1 byte (which is stored in the DCRCR) is loaded in the RAM location by the DCRAR.

Step 4. Post increment operation is executed in the DCRAR to make it point to the next RAM location. Overflow of the DCRAR, i.e. overflow from 191 to 192, makes it undefined. The programmer has the responsibility to keep track of DCRAR and reload the right address whenever necessary.

It is the command 1 which triggers the load of DCRCR and DCRTR into RAM and the post increment operation.

If the attributes of a series of displayed characters are the same, only DCRCR has to be updated.

7.3 Default value of character size and background colour

The default value, after master reset, of the display characters are as follow:

- character size = 1V/1H
- background colour = blue (R = 0, G = 0, B = 1, I =0)
- end of display control = 0

If another value is required, the first character should be space code and the second character should be CR code to define the character size and background colour.

8 ALL REGISTERS, AND COMMAND BANK SELECTION

Command 0, 7, 8, 9, A, B, C, D, F are for general control.

8.1 Command 0, B, C, D

Command 0 is "bank selection". It is to determine the BS bit in the command list in Table.1. After master-reset BS bit is in 0 state.

Command B, C, D are to determine the start position of the characters. 64 different positions are available both for vertical and horizontal positions. Fig.12 shows and example. Also see Table.1 for command list. Default value of starting position is not guaranteed. ("Default" means the state after master reset)

The starting position is calculated as
$HPx = [\ 4 \times (H5 \ldots H0)_{DECIMAL} + 5\ ]$
(OSD LC clock)
in which $(H5 \ldots H0) \geq 10_{DECIMAL}$
and
$VPx = [\ 4 \times (V5 \ldots V0)_{DECIMAL}\ ]$ (Horizontal lines)
in which $(V5 \ldots V0)_{DECIMAL} \geq 0$

Note: These value are exactly the same as those of PCA84C640 families.

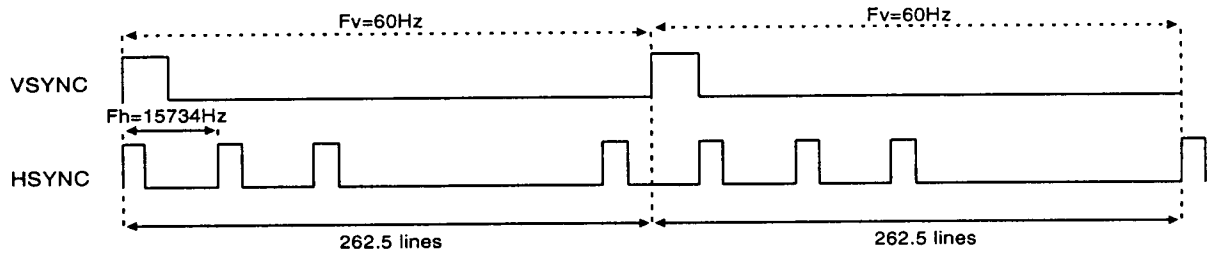
8.2 Command 7, 8, 9, A, F

Command 7, 8, 9 and A, F are the control register 1, 2, 3 and 4, 5 and are to control:

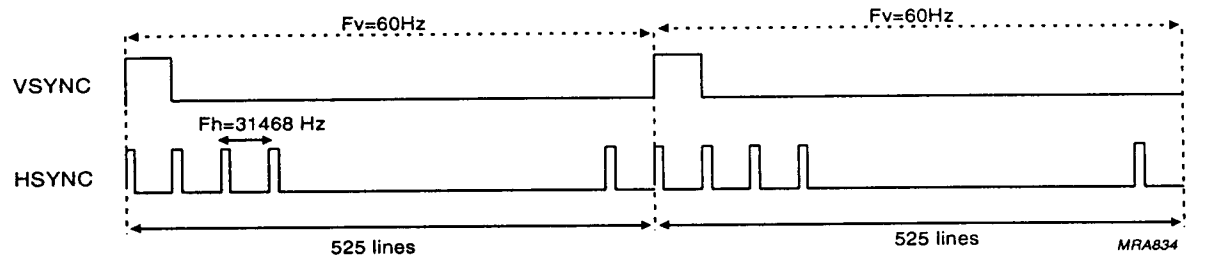
8.2.1 Control register 1 (command 7)

1. the disable (= 0)/enable (= 1) of the OSD (EN bit)
   Default = 0
2. Scanning Mode of the TV standard (M1, M0),
   M1,M0 = 00, 1V, 1H (525LPF (Line Per Frame) /60 Hz - NTSC or 625LPF/50 Hz - PAL)
   M1,M0 = 01, reserved
   M1,M0 = 10, 1V, 2H (1050LPF/60 Hz - NTSC)
   M1,M0 = 11, 2V, 2H (1250LPF/100 Hz - PAL)
   Default = 00

In which 1V, 1H is the conventional NTSC or PAL scanning mode. 1V, 2H is the so called LPS (Line Progress Scan) which is for the IDTV in NTSC and 2V, 2H is for PAL system and is known as 50 Hz to 100 Hz scan conversion. Timing see Figs.13 and 14.



(a) Conventional NTSC 1V/1H



(b) NTSC 1V/2H

Fig.13 Scan format (NTSC).

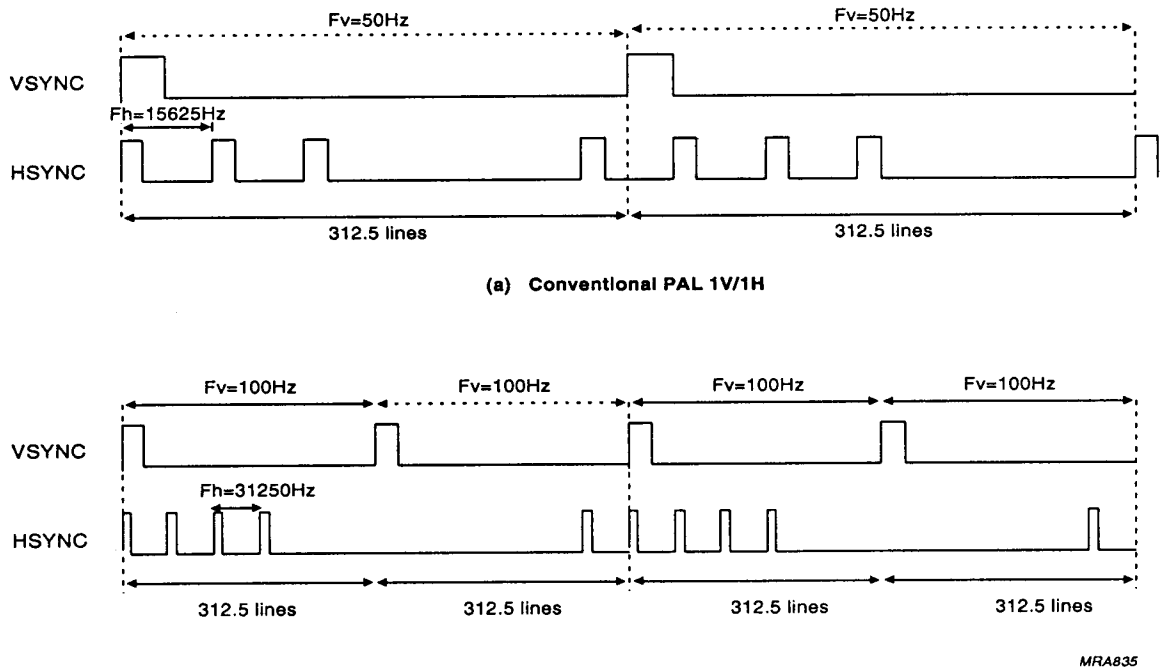


Fig.14 Scan format (PAL).

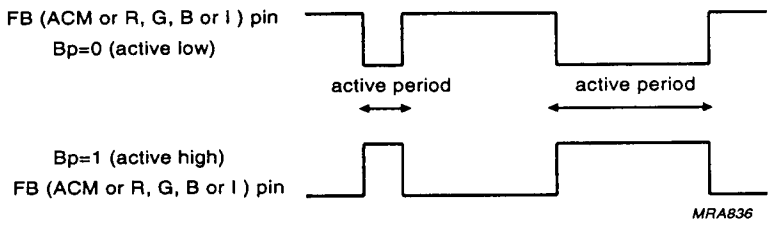


Fig.15 Bp bit to decide the active level of FB, ACM, R, G, B and I pins.

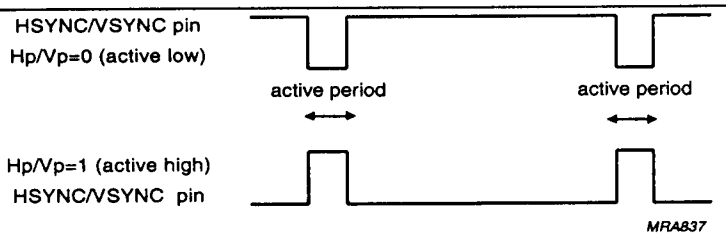


Fig.16 Hp/Vp bits to decide the active level of HSYNC/VSYNC signal.

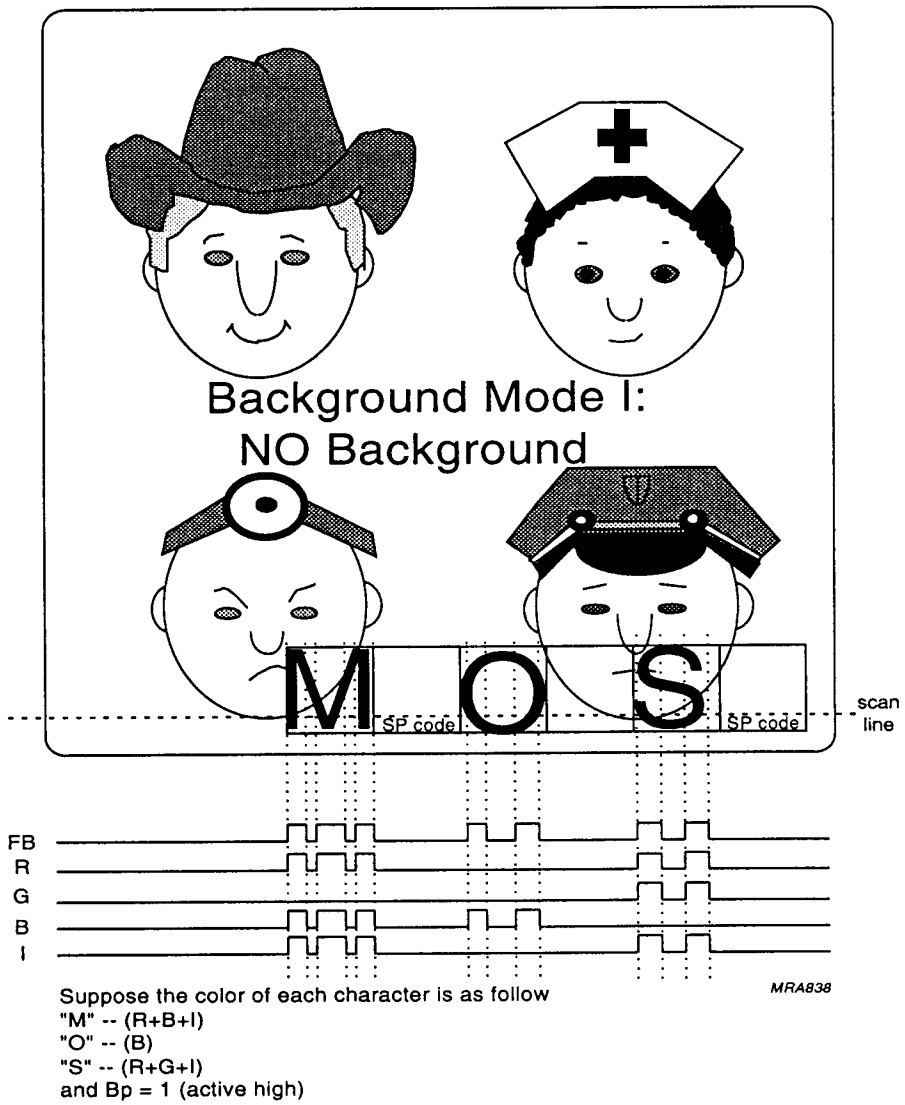


Fig.17 Background shadowing mode (I): NO Background -- Superimpose.

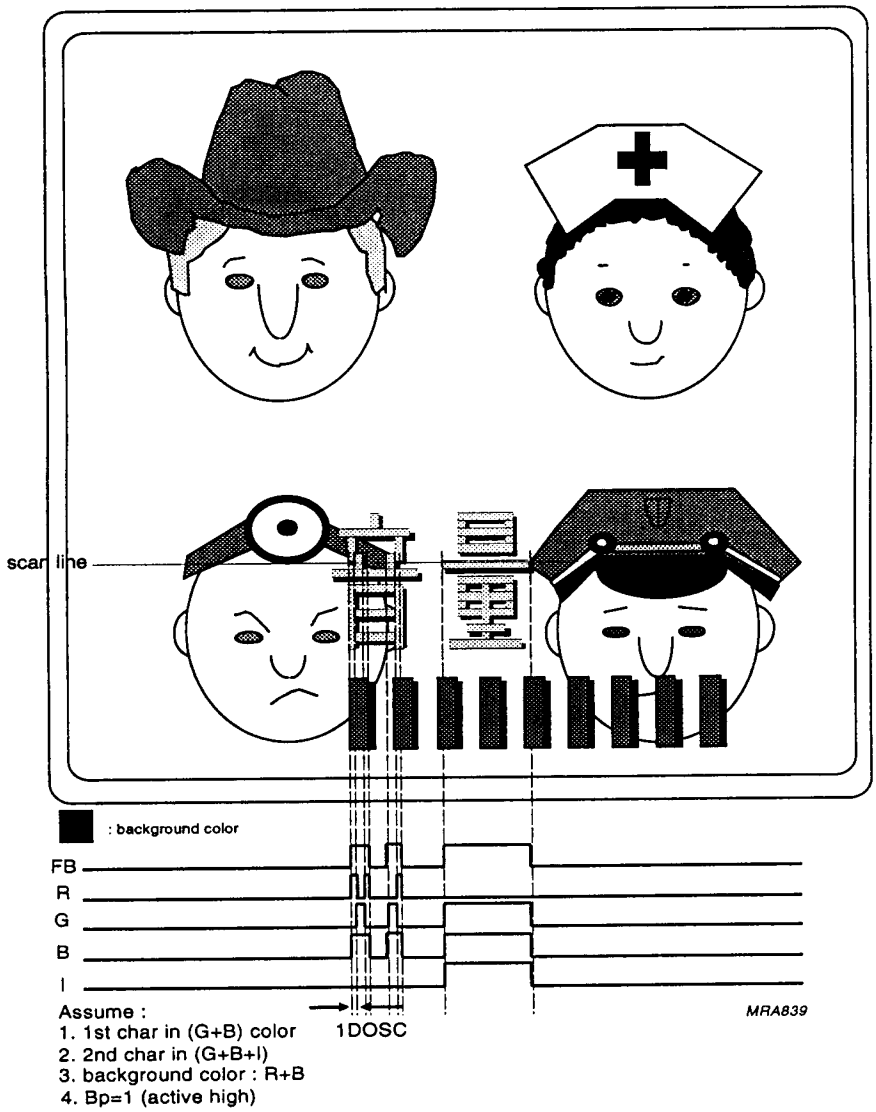


Fig.18 Background shadowing mode (II): North-west Shadowing.

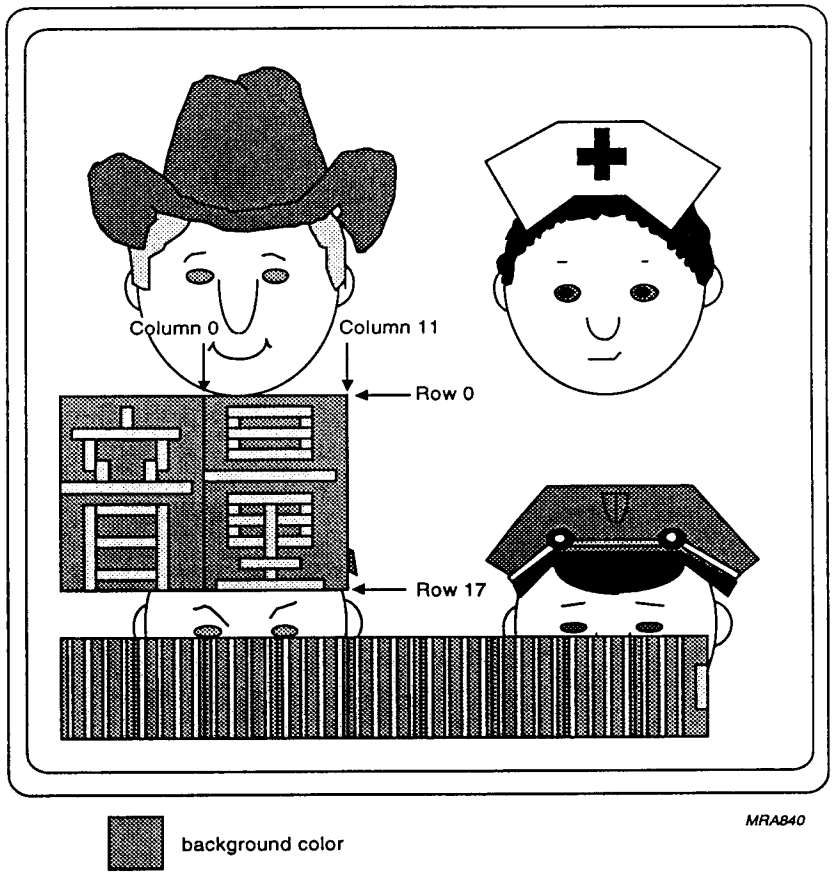


Fig.19 Background shadowing mode (III): Box Shadowing mode.

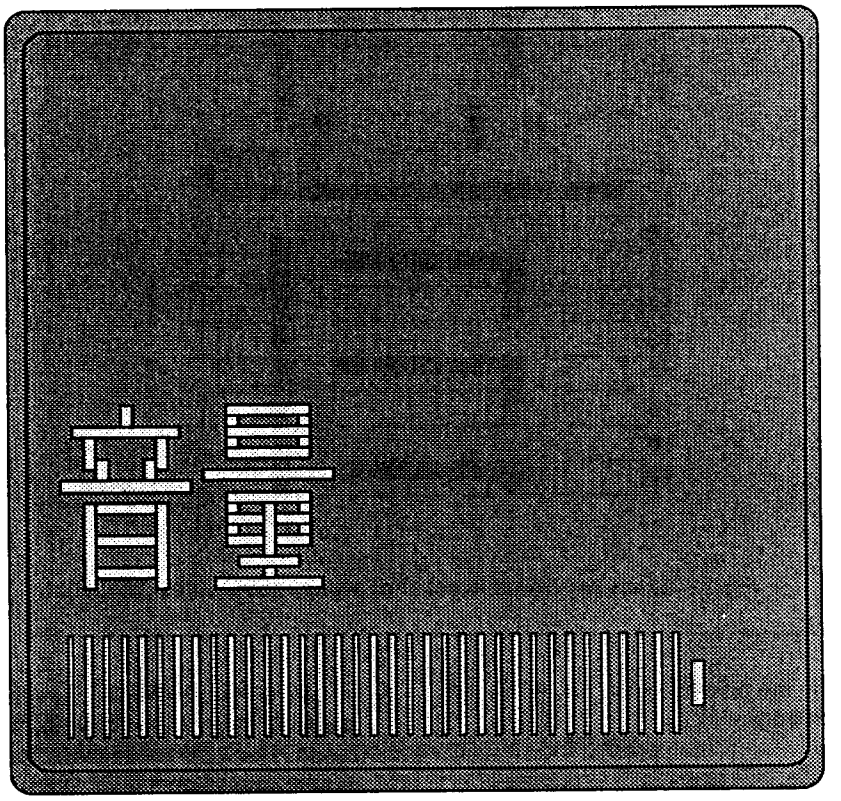


Fig.20 Background shadowing mode (IV): Frame Shadowing Mode.

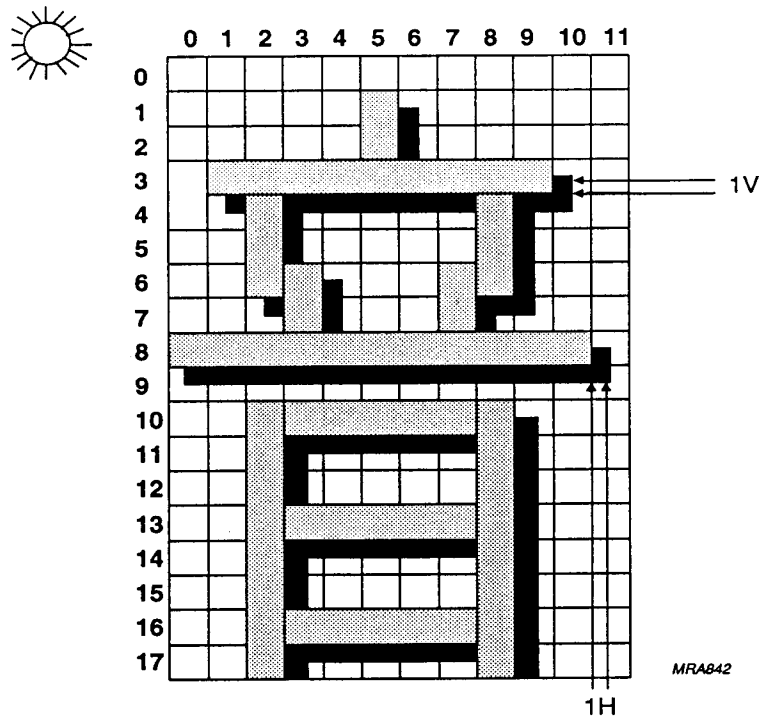


Fig.21 Example of north-west shadowing mode (size = 2V/2H).

3. Bp bit is to determine the polarity of the FB, ACM and RGB and I output polarity.

   Bp = 0, active LOW

   Bp = 1, active HIGH (the output colour is shown in Table.4

   Default = 1

8.2.2 CONTROL REGISTER 2 (COMMAND 8)

4. Hp is for the Horizontal Sync input polarity.

   Hp = 0, active LOW

   Hp = 1, active HIGH

   Default = 0

5. Vp is similar to Hp (i.e. when C/S bit of command D is 0) and is for the Vertical Sync input.

   Vp = 0, active LOW

   Vp = 1, active HIGH

   Default = 0

6. S1, S0 are for background/shadowing mode control.

   Mode 0: (Fig.17) S1,S0 = 00, "no background" mode. The OSD fonts/characters are directly superimposed on the TV video signals.

   Mode 1: (Fig.18) S1,S0 = 01, north-west shadowing, available only in the character size = 2V/2H or 4V/4H.

   The shadows of the characters are generated by placing a light source on the north-west 45 °C direction, (see also Fig.21 and Fig.22).

   The shadow generated by the north-west shadowing mode is only within the 18 rows in vertical direction although it can be one bit extended to next font's 1st column in horizontal direction. Figs.23 and 24 illustrate how to design the bit pattern to get the required north-west shadow effect.

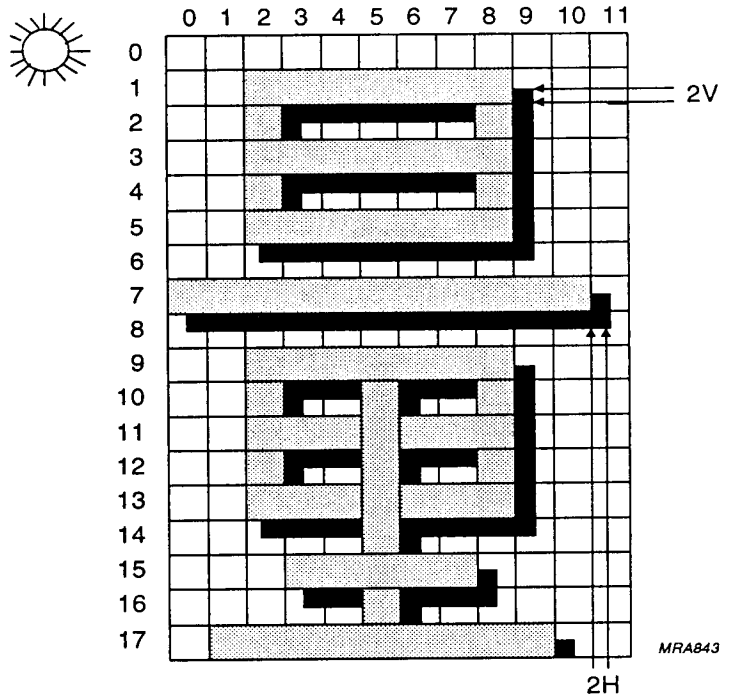


Fig.22 Example of north-west shadowing mode 2H (size = 4V/4H).

Mode 2: (Fig.19) S1,S0 = 10, box shadowing

Box shadowing is to surround the character font by a 12 x 18 dots box in background. i.e. within the character font cell, where there is no foreground dot there is background dot, (see Fig.25).

Mode 3: (Fig.20) S1,S0 = 11, Frame Shadowing (raster blanking), background colour displayed on full screen where no bit patterns are on.
Default colour = blue (B=1, R=G=I=0)

The background colour is decided by command F and has 16 different colours, (see Table.1).

8.2.3 CONTROL REGISTER 3 (COMMAND 9)

BF1,BF0 bits are to control the character blinking frequency. It is decided by the:

$$Vsync/(16 \times 2^{(BF1,BF0)_{decimal}})Hz$$

i.e.
BF1,BF0 = 00, blinking frequency is Vsync/16 Hz
BF1,BF0 = 01, blinking frequency is Vsync/32 Hz
BF1,BF0 = 10, blinking frequency is Vsync/64 Hz
BF1,BF0 = 11, blinking frequency is Vsync/128 Hz

BR1,BR0 bits are to control the active ratio of the character blinking:
BR1,BR0 = 00, active ratio is 3:1
BR1,BR0 = 01, active ratio is 1:1
BR1,BR0 = 10, active ratio is 1:3
BR1,BR0 = 11, reserved

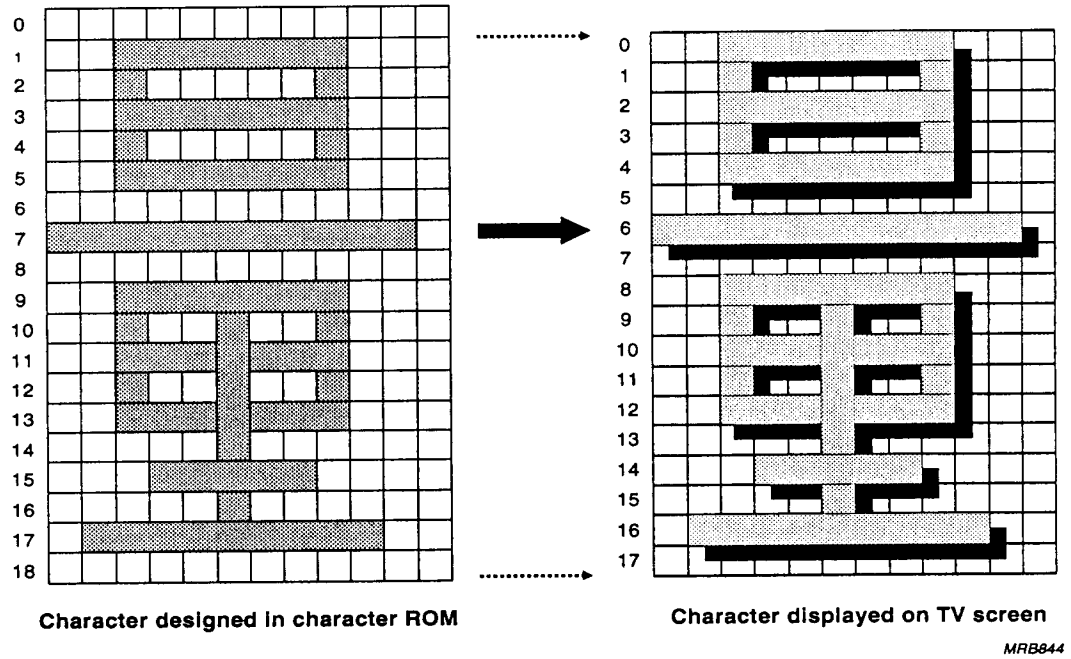
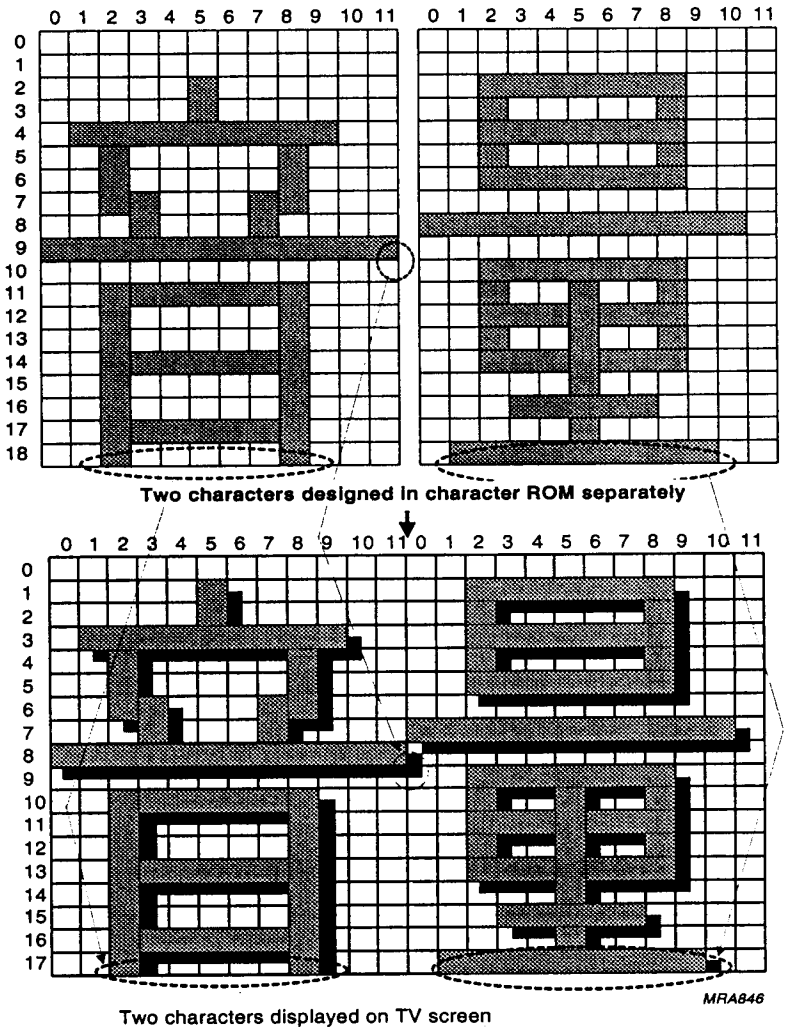


Fig.23 Example of north-west shadowing mode.



Note : Cell boundary (black bold lines)

Fig.24 North-west shadowing.

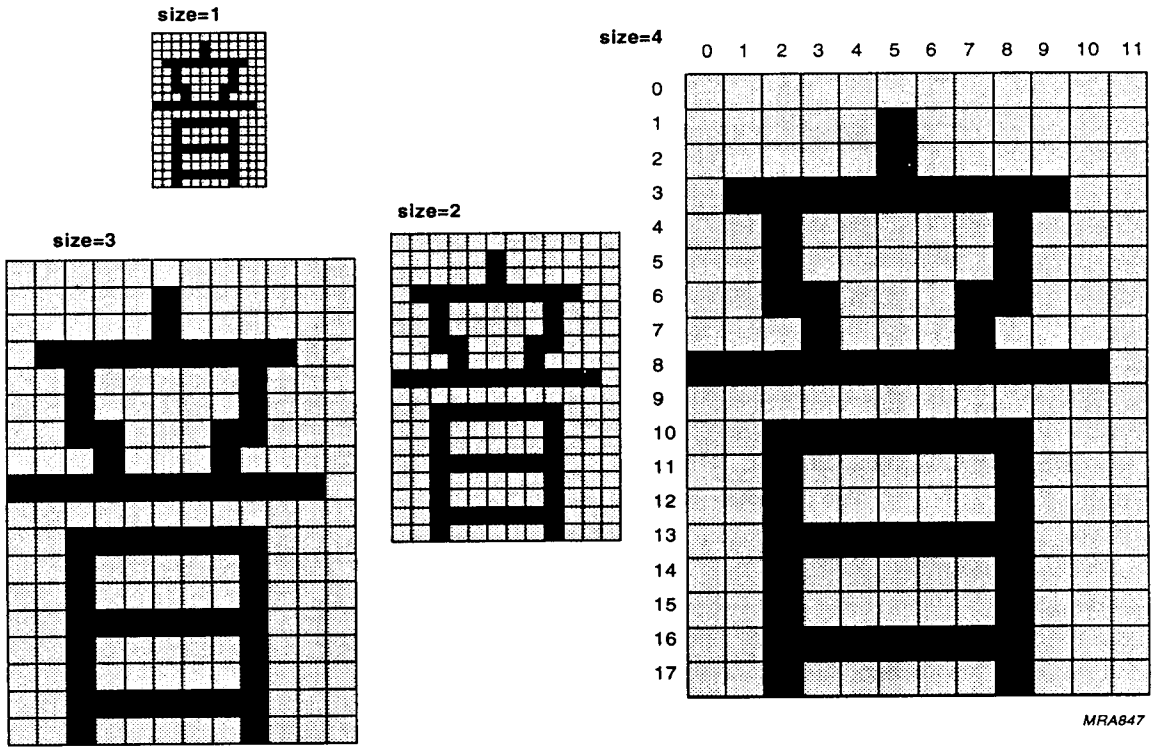


Fig.25 Example of box shadowing mode.

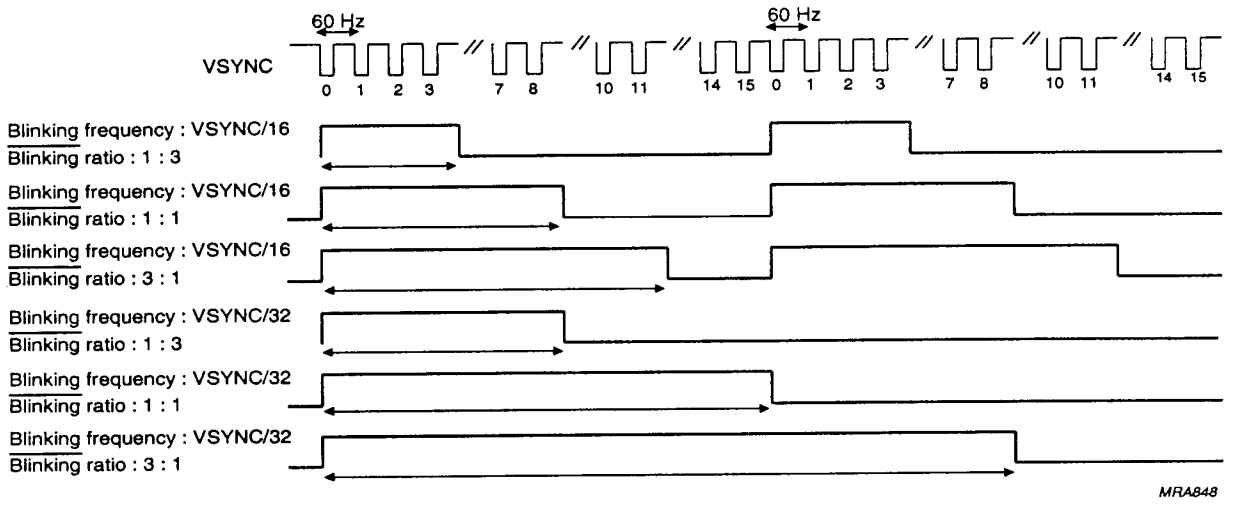


Fig.26 Example of character blinking (NTSC 525LPF/60 Hz)

Fig.26 shows the timing diagram of character blinking frequency and blinking ratio.

8.2.4 CONTROL REGISTER 4 (COMMAND A)

- A/P, to select pin 2, ACM/P04 pin as ACM function or as P04.
  A/P = 0, P04
  A/P = 1, ACM
  Default = 0
- C/S, to select pin 15 as CK_{OUT} or P05.
  C/S = 0, P05
  C/S = 1, CK_{OUT}
  Default = 0
- P/I, to decide the pins 17, 19, 21, 23 are for RI, GI, BI and FBI input or for general Port function.
  P/I = 1, for RI, GI, BI and FBI
  P/I = 0 for general Port
  Default = 0.

8.3 Combination of two or more font cells to formulate a next pattern

The user can combine two (or more) font cells to formulate a next higher resolution pattern, (Figs.27, 28, 29 and 30).

The combination of two cells in the horizontal direction needs no special care. All 4 background/shadowing modes are applicable.

The combination of two cells in the vertical direction needs the following special care:

- space between two rows should be programmed as 0 (bit <2:1> of carriage return code = 00)
- Row 0 is reserved for use only in the north-west shadowing mode (details see section 8.2 command 8). It is when two characters are combined in vertical direction to formulate a new pattern, this row 0 contains the bit pattern of row 18 of the character above it. See (Figs.29 and 30).
- If no combined character in vertical direction is intended for this character, row 0 should be fill in all "0's".

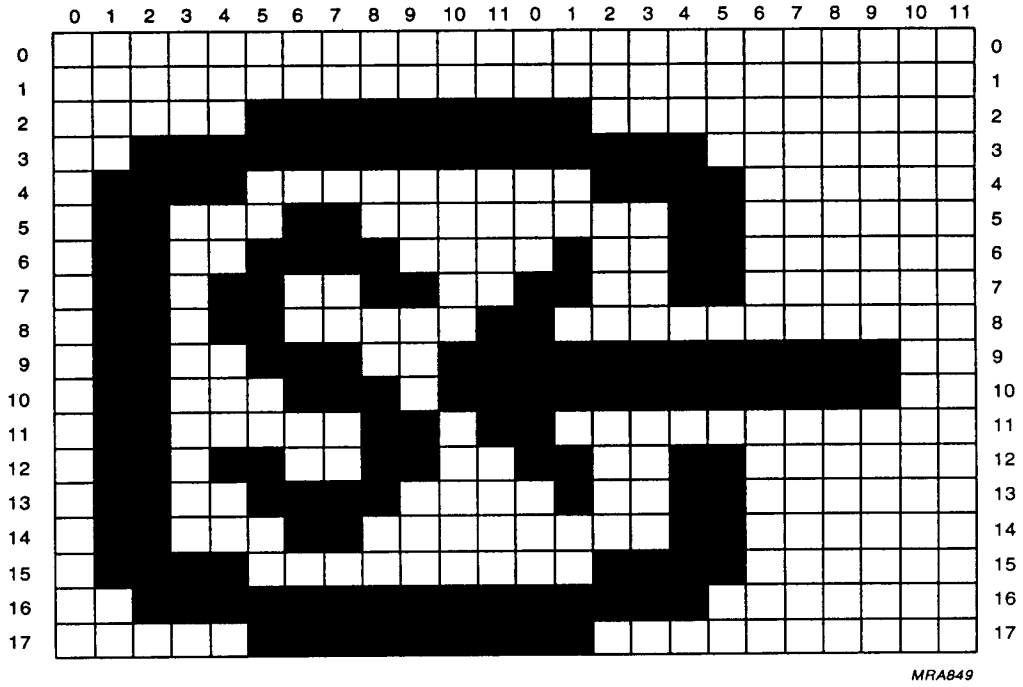


Fig.27 Combination of two character cell to form a next font (in horizontal direction).

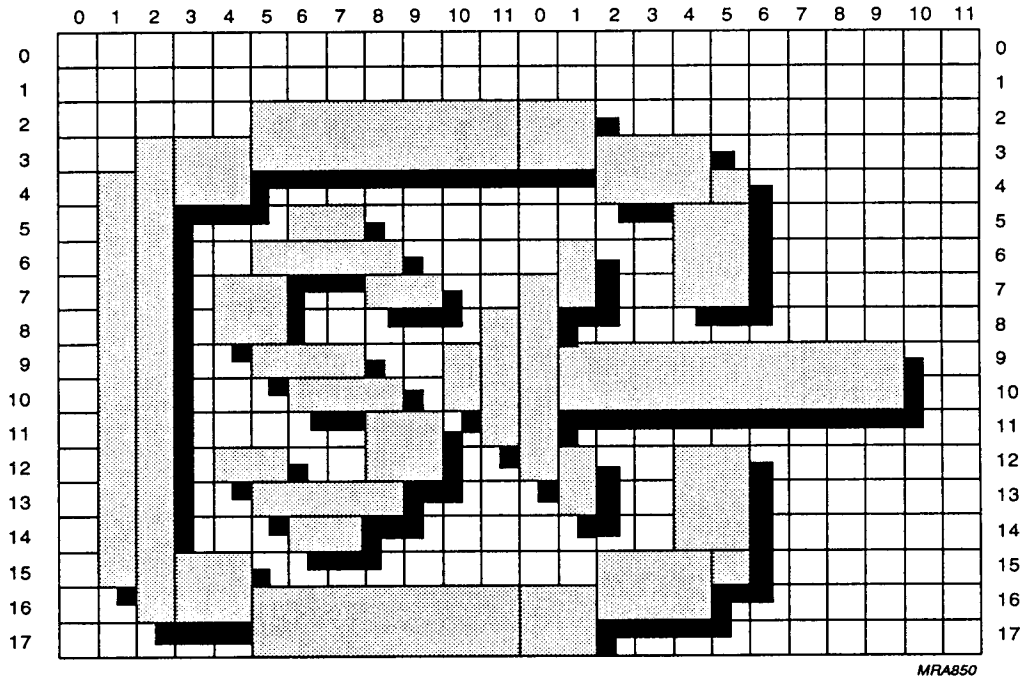


Fig.28 North-west shadowing mode in Combination of two character cell to form a new font (in horizontal direction).

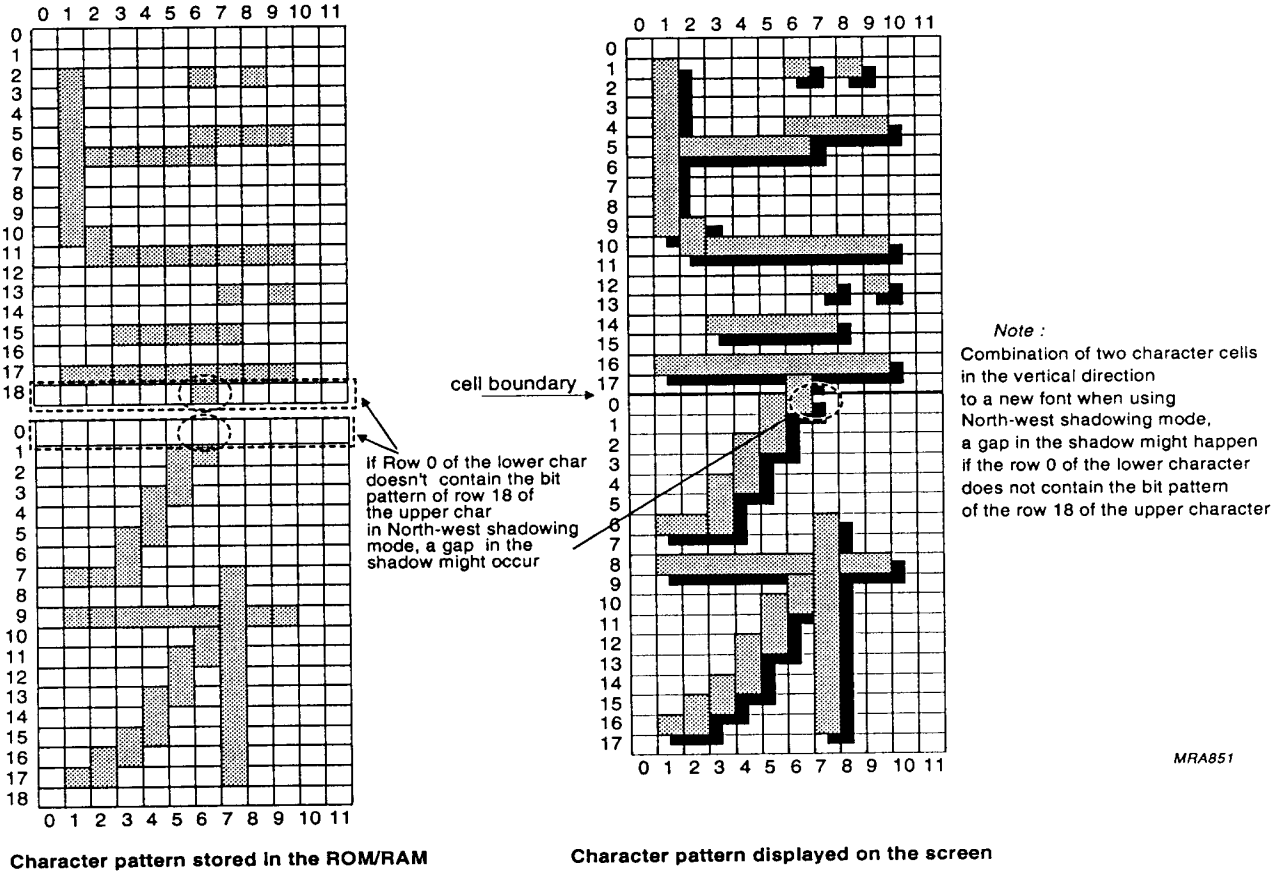


Fig.29 Combination of two characters in vertical direction to formulate a new pattern.

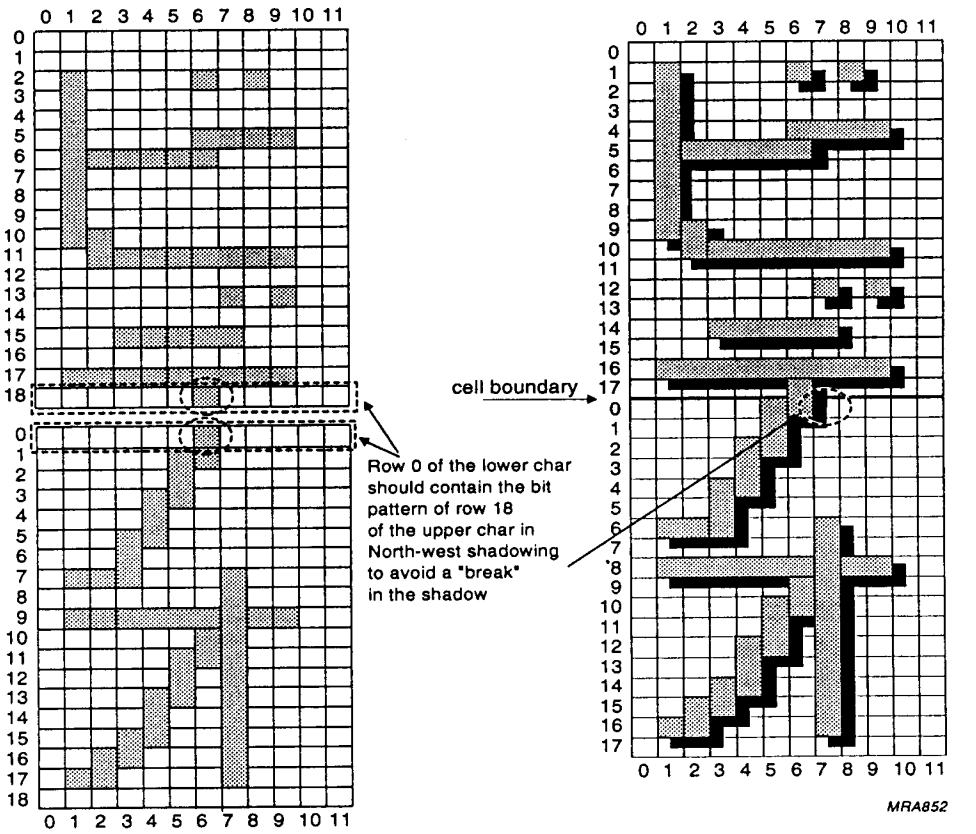


Fig.30 Combination of two characters in vertical direction to formulate a new pattern.

8.4 Space code and carriage return code in different background/shadowing modes

Figs.31, 32, 33 and 34 show the space code and carriage return code in 4 different background/shadowing modes.

1. in mode 0, "no background mode" – both reserved codes display a transparent (no bit) pattern with the video signal as its background (superimpose).
2. in mode 1, "north-west shadowing" – same as mode 0.
3. in mode 2, "box shadowing mode" – space code display an opaque pattern with the background colour that it intends to change or keep (i.e. same as the background colour of the character next to this space code see Fig.33). Also space code can display a "transparent" pattern as shown in Fig.34. To select space code as opaque or transparent is done by metal option in mask making process and should be indicated on ROM code entry form. Carriage return code is a transparent pattern superimposed on the video.
4. in mode 3, "frame shadowing" – transparent pattern with background colour as its colour.

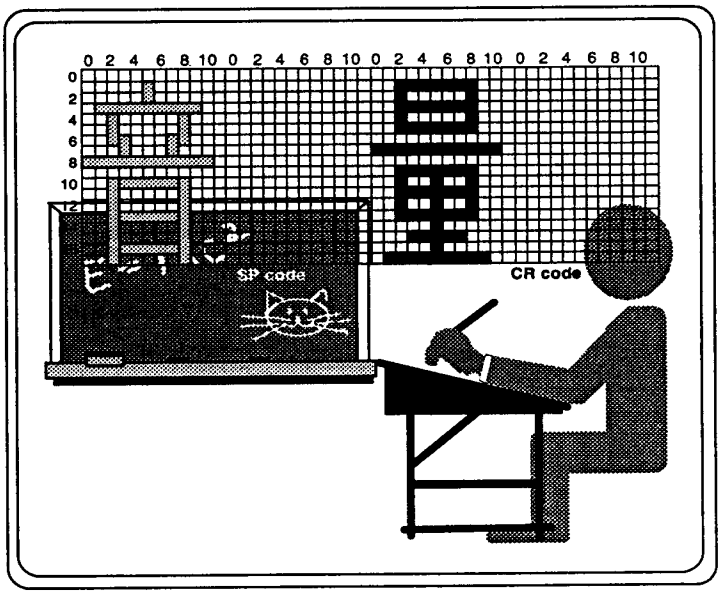


Fig.31 SP and CR code in no background (superimpose) mode (transparent pattern).

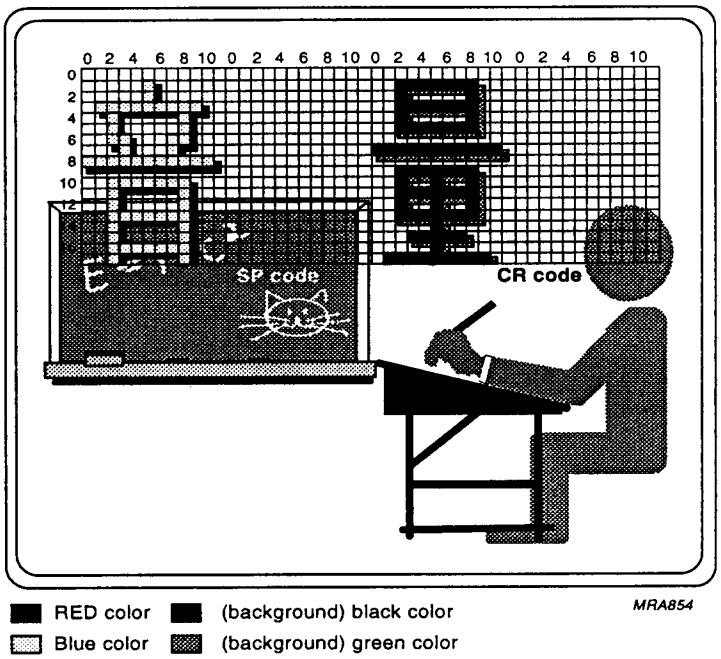
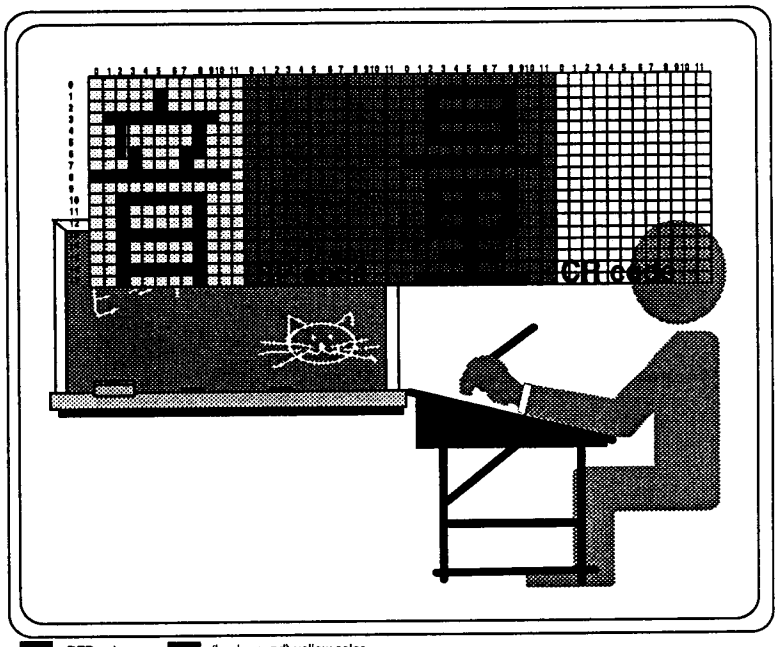


Fig.32 SP and CR code in north-west shadowing mode (transparent pattern).

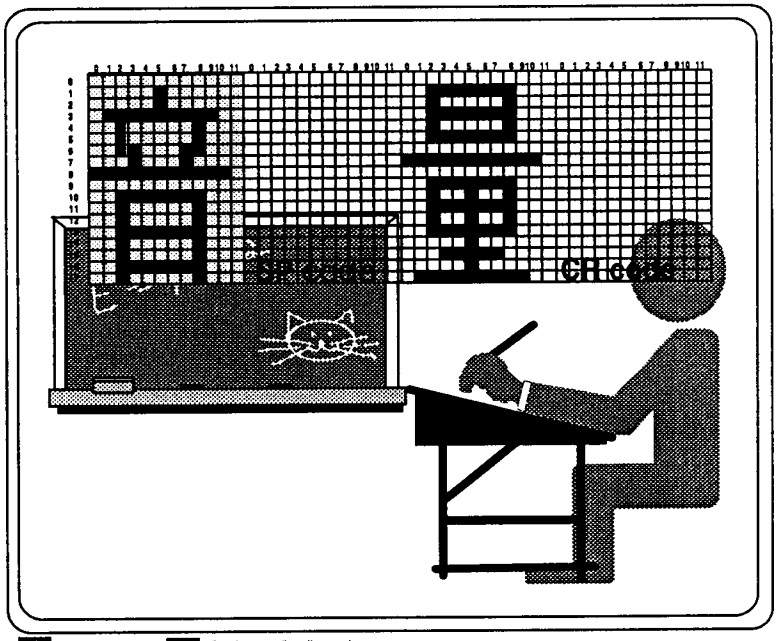


SP code is an opaque pattern with the background color of the character it intends to change or keep

CR code is always a transparent pattern with the video signal as its background

SP code can change the background color of itself and the character/word next to it (in this example : from cyan to yellow)

Fig.33 SP and CR code in the box shadowing mode.

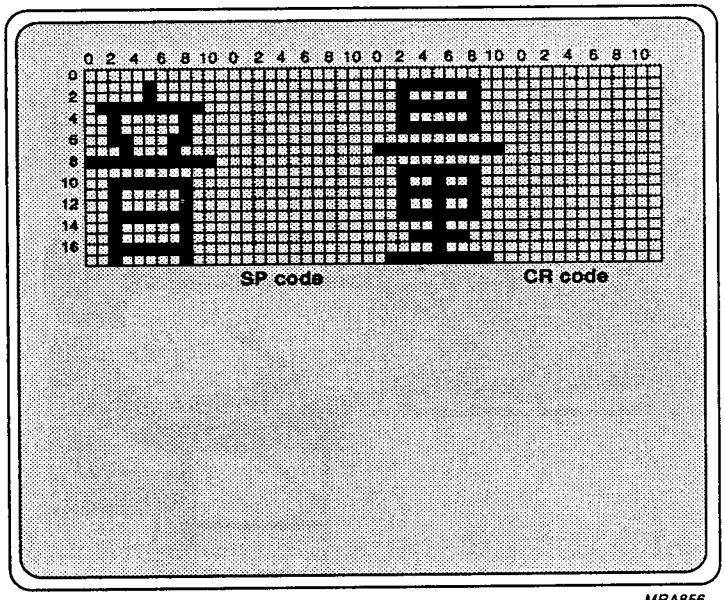


SP code is an transparent pattern without any background color.

CR code is always a transparent pattern with the video signal as its background

SP code can change the background color the character/word next to it
(in this example : from cyan to yellow)

Fig.34 SP and CR code in the box shadowing mode.



RED color (background) yellow color

Blue color

SP and CR code are all transparent pattern with the background color as its color

Fig.35 SP and CR code in the frame shadowing mode.

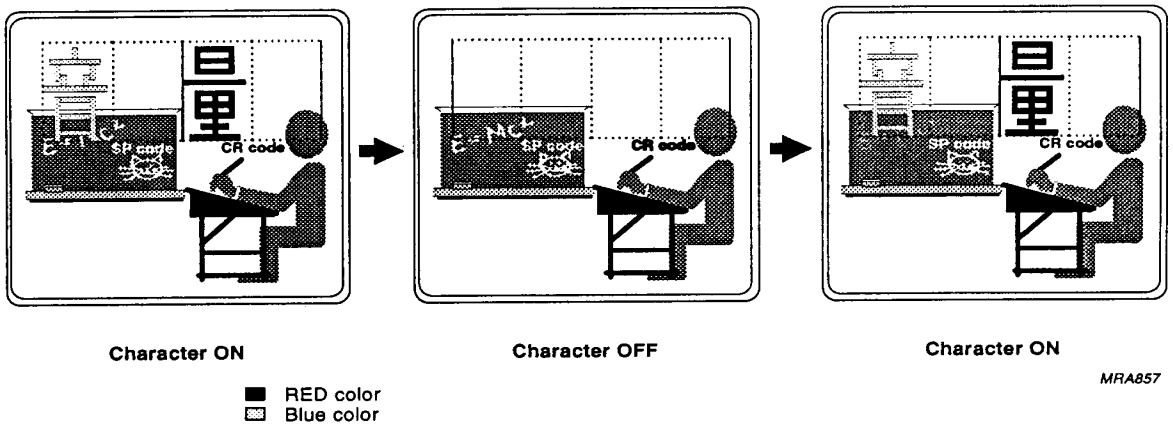


Fig.36 SP and CR code in no background (superimpose) mode (transparent pattern) when blinking of character is set.

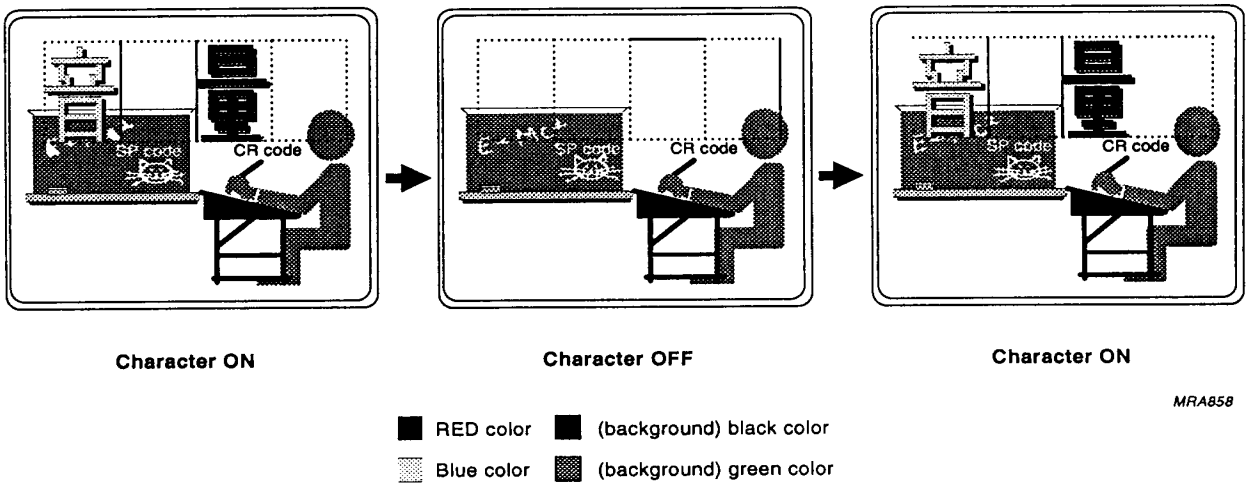


Fig.37 SP and CR code in north-west shadowing mode (transparent pattern) with blinking of character set to active.

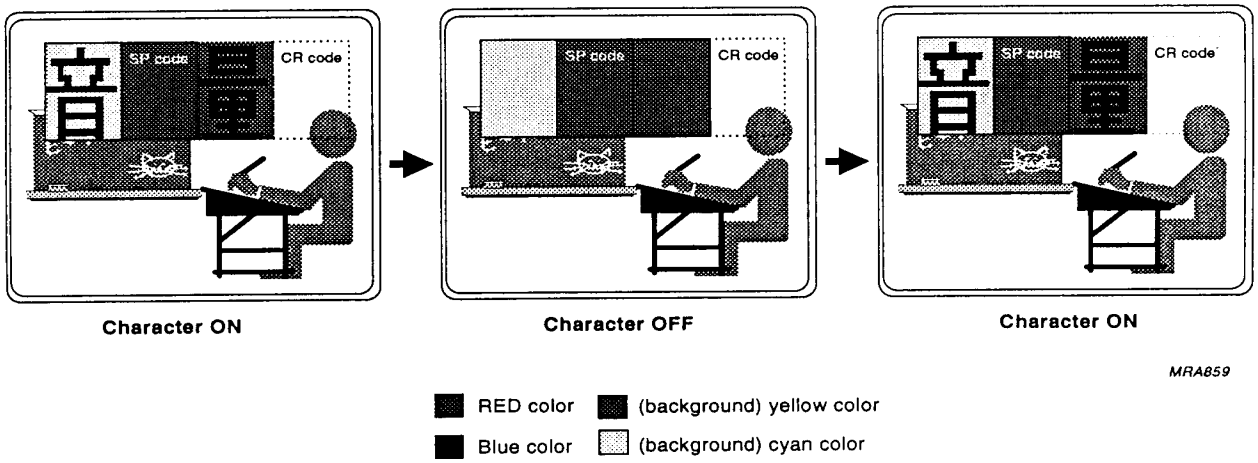


Fig.38 SP and CR code in the box shadowing mode with blinking of character set to active.

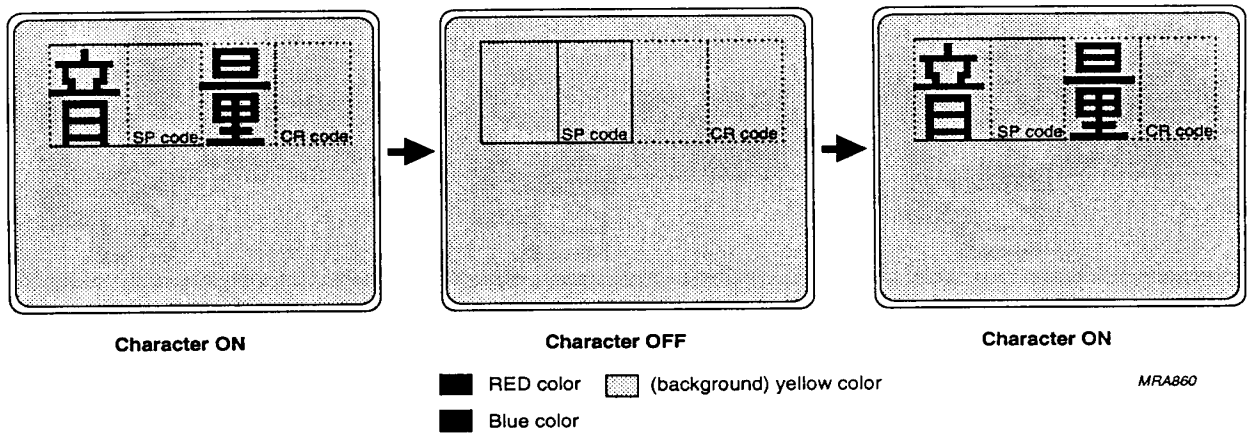
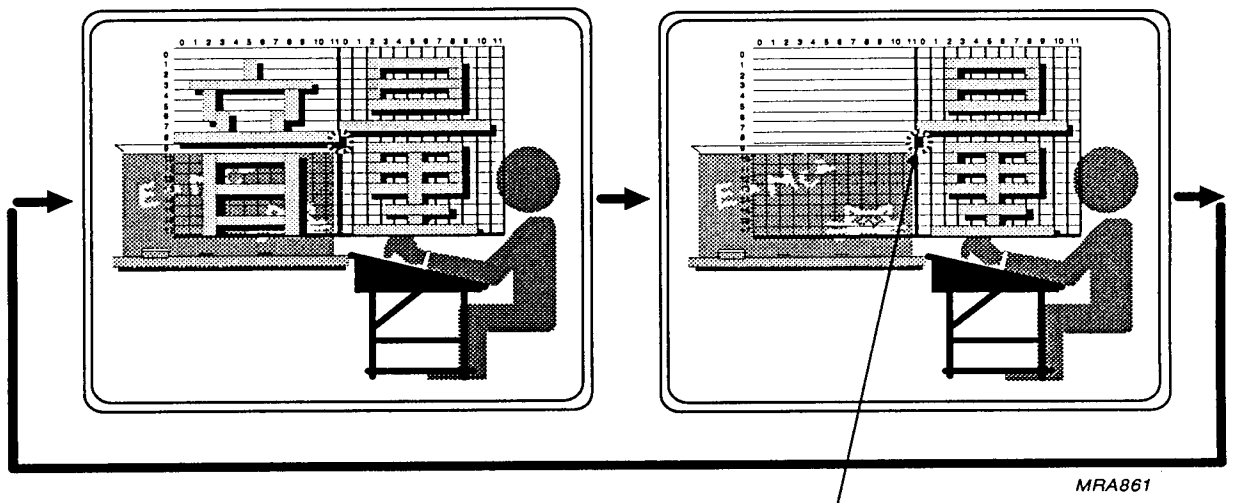


Fig.39 SP and CR code in the frame shadowing mode with blinking of character set to active.



In this example, assume
- 1st character is in blinking mode
- 2nd character is not
- the first character bit pattern is designed such that the north-west shadow of the 1st character falls into the cell of 2nd character

When the 1st character is blinking and shown up in the screen, everything is fine
But when the 1st character is off then the shadow of the 1st character falls into 2nd character cell will still remain there.
To avoid this happen, user can either
- design bit pattern in such a way that shadow does not cross the cell boundry
- make adjectent characters all blinking or all don't blink

Fig.40 Blinking of character is within the character cell only (12 x 18).

9 OSD CLOCK IN DIFFERENT TV STANDARD

9.1 Maximum number of characters/row/frame in different TV standard

The maximum number of characters per row is determined by the

- LC OSD clock frequency
- TV standard

The maximum OSD clock frequency is 14 MHz. Given an NTSC 525LPF (Line Per Frame)/60 Hz example below, (Fig.41).

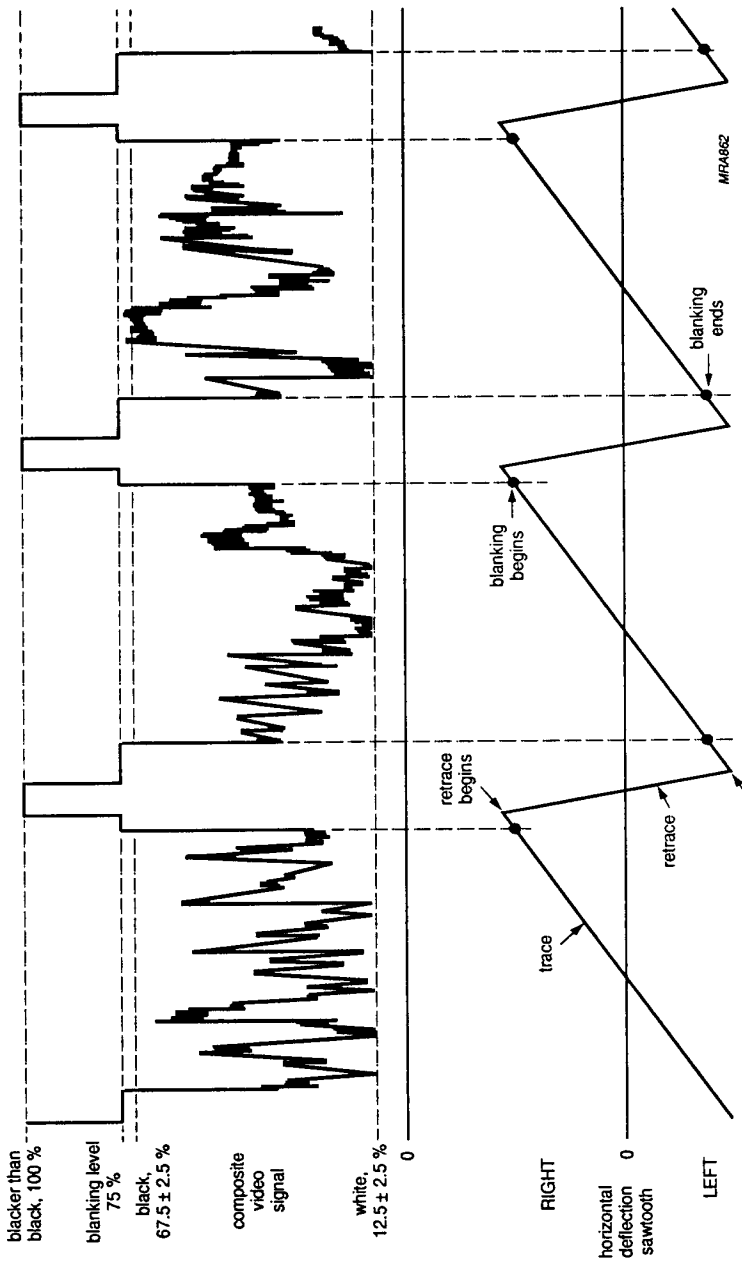


Fig.41 Composite video signal for three horizontal lines compared to three horizontal deflection sawtooth (NTSC 525LPF/60 Hz)

The active video signal period of a horizontal line is 53.5 us. In order to reduce the jittering of the screen edge, overscan is normally applied by the TV manufacturer. It causes the real visible video period of a horizontal line reduced to 53.5 us x 9/10 = 48.15 us.

9.1.1 CASE 1

- OSD clock frequency = 6 MHz i.e. period = 0.166 us,
- number of visible dots on a horizontal line 48.15 us/0.166 us = 290 dots
- the starting of first character dot is roughly 45 dots after HSYNC. (see command B, C, D).
- Thus the visible dots are 290 – 45 = 245 dots.
- Each character is composed of 12 × 18 dots.
- So the maximum number of characters displayed on a row with OSD clock = 6 MHz in 525LPF/60 Hz NTSC are 245/12 = 20 characters.
- In a 19" TV screen, the width of a horizontal line is around 370 mm which gives approximately 18.5 mm/character in width.

9.1.2 CASE 2

- OSD clock frequency = 10 MHz i.e. Dot period = 0.1 us
- 48.15/0.1 = 481 dots per horizontal line
- 481 – 45 = 436 visible dots in a line
- 436/12 = 36 characters per row
- Again, in the 19" TV case, the character width is 370 mm/36 = 10.3 mm per character.

9.2 Maximum number of rows of characters per frame:

- In NTSC 525/60, the active lines are roughly 241.5H to 249.5H per field (Fig.42). Take 241 as an example, the maximum number of character rows per frame is (remember a character is 12 x 18 dots): 241/18 = 13 rows.
- In PAL 625/50, it is around 280/18 = 15 rows.
- In 1050/60 NTSC, although the active lines per frame is doubled but in order to keep the character physical height the same as the 525/60 NTSC, HSYNC is internally divided by two in this mode, (see also section 6.2). So the maximum number of character rows are 13.
- In PAL 1250/100, it is not necessary to divide the HSYNC by two because both horizontal and vertical frequency are doubled. The maximum number of character rows are 15.

9.3 Maximum OSD frequency

The LC OSD oscillator can work in between 4 MHz to 14 MHz.

As PCA8510 supports 4 different TV scanning standards, to apply the right OSD clock frequency to it is essential for best looking characters.

1. In the conventional NTSC 525LPF/60 Hz and PAL 625LPF/50 Hz, the OSD clock is directly applied to the OSD circuitry and can be as low as 4 MHz and as high as 14 MHz.

   In NTSC 525/60 standard, each character dot physical width on a 19" screen, when the OSD clock frequency is 8 MHz, is 13.2 mm.
2. In the 1050LPF/60 Hz NTSC LPS standard, to keep the character dots look with the same width as that of the 525LPF/60 Hz with a OSD clock frequency equal 7 MHz, the DOSC needs to be 14 MHz because the horizontal line frequency is doubled.

   Internally, the HSYNC is also divided by 2 to keep the same character height as that of 525/60 standard.
3. In the 1250/100 PAL standard, the OSD clock frequency needs to be doubled as well to keep the dot physical width the same as that of the 625/50 PAL standard.

   The HSYNC is directly applied to the OSD circuitry without being divided by two because both horizontal frequency (1250 Hz) and vertical frequency (100 Hz) are doubled.

10 OUTPUT PORTS, R, G, B AND FB INPUT

In the teletext with OSD application, there are two "text" sources to be displayed: the teletext characters and the OSD characters.

10.1 Teletext switch

In this proposal, a switching circuit which enables the OSD characters to be displayed on the teletext and TV picture is implemented.

Fig.43 shows the block diagram of the switching circuit. Command A (Table.1) is the control register 4. The P/I bit is to control the RI, GI, BI and FI pins as either text input pins or output Port pins. When P/I bit is configured as the text input, the text deinterlacing function is performed internally to reduce the flickering of the display lines.

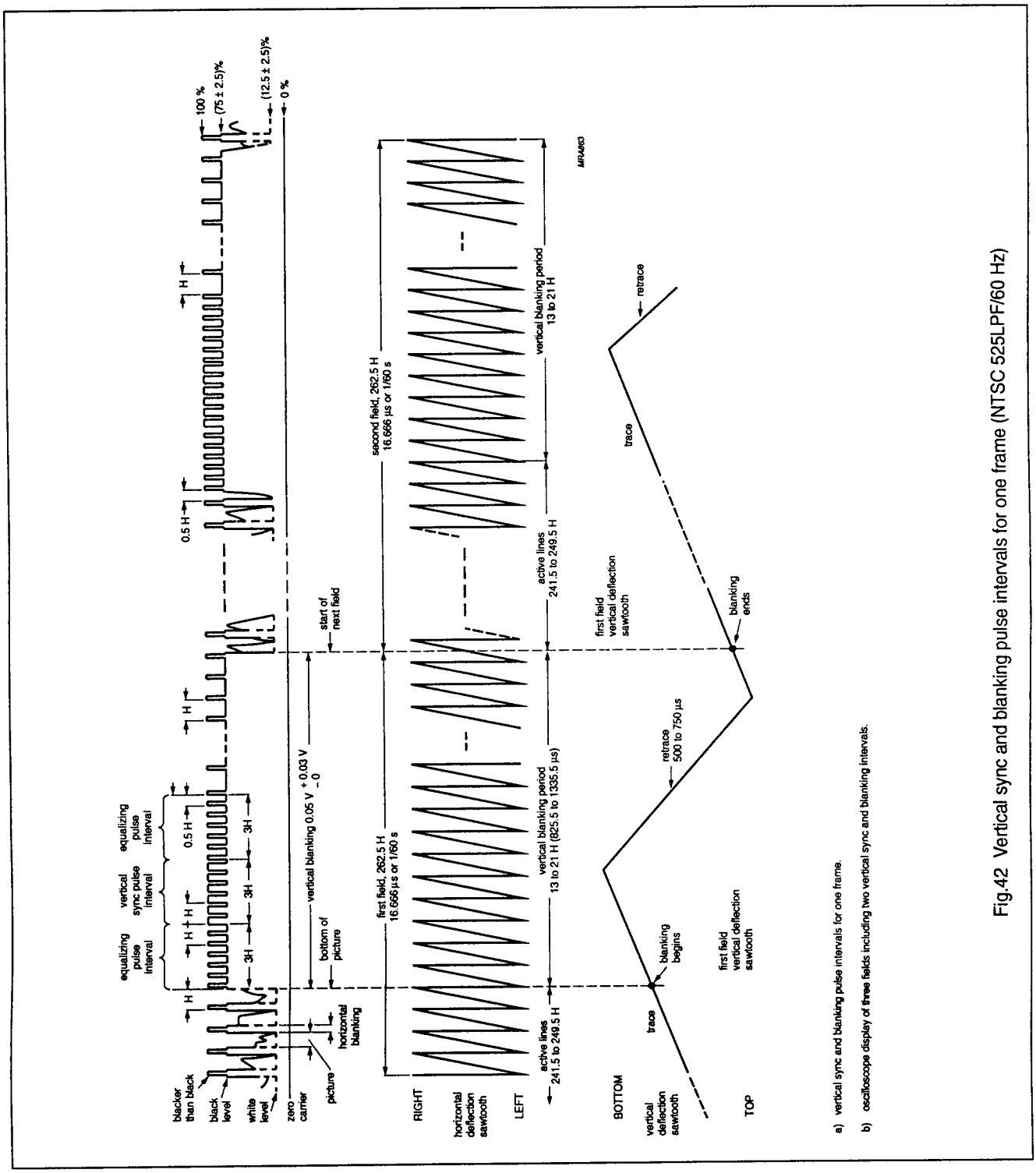


Fig.42 Vertical sync and blanking pulse intervals for one frame (NTSC 525LPF/60 Hz)

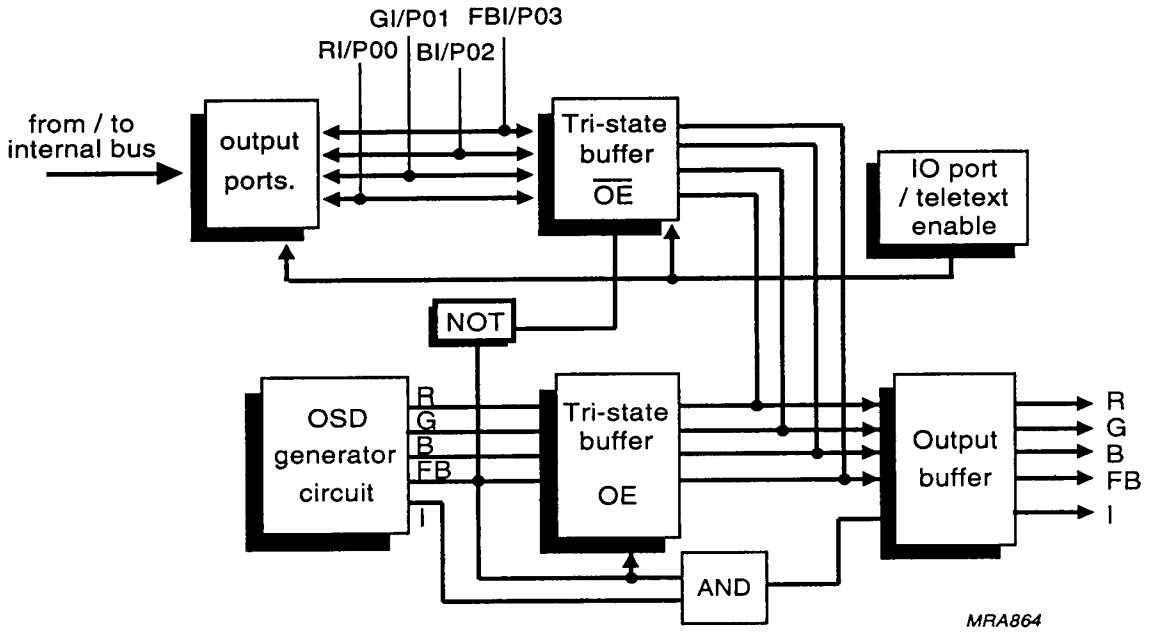


Fig.43 OSD/teletext switching circuit.

10.2 Output Ports

The Port 0 is an output Port.

10.2.1 PORT WRITE

When Port pin is in output state, 0 or 1 can be written to the Port register by command E (see Table.1)

10.2.2 PORT OPTION

Option 1: standard output
Option 2: open drain output
Option 3: push-pull output

10.2.3 POWER ON PRESET/PRE-RESET OF P00 - P05

Mask option is available to configure the P00 - P05 to a predefined stage (0 or 1) after reset signal is active.

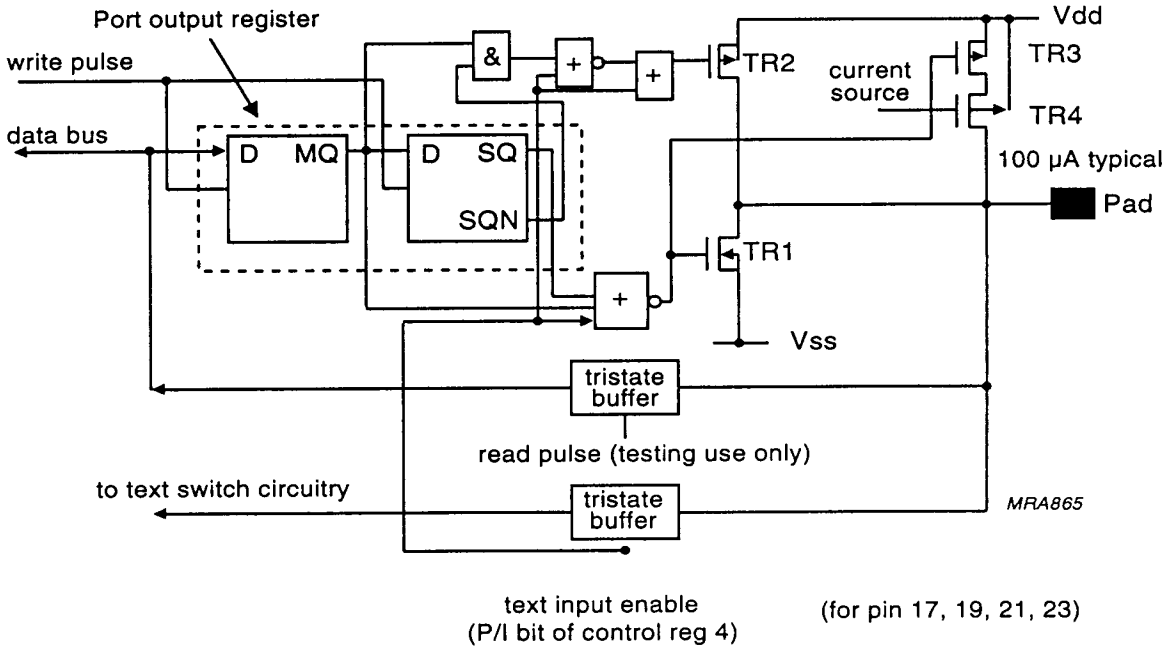


Fig.44 Standard output with switched pull-up current source (option 1).

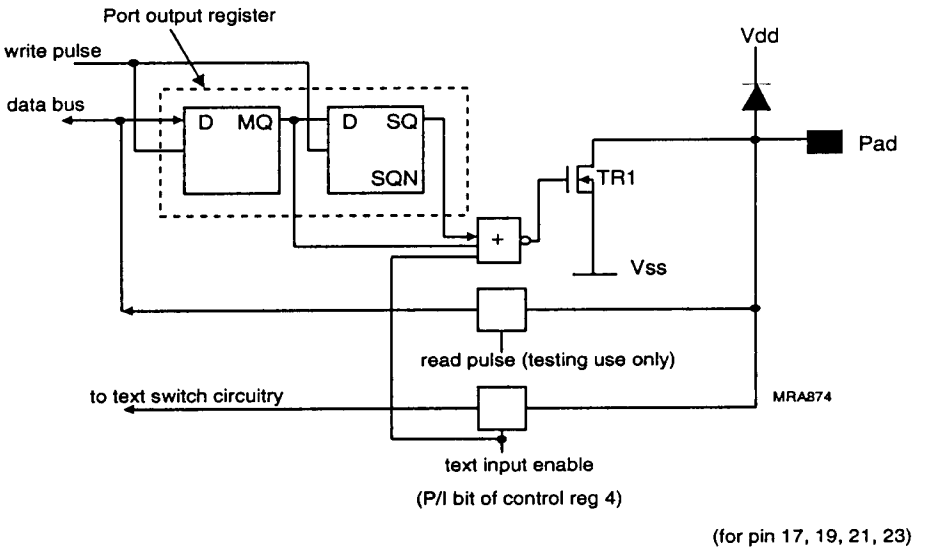


Fig.45 Open drain output (option 2).

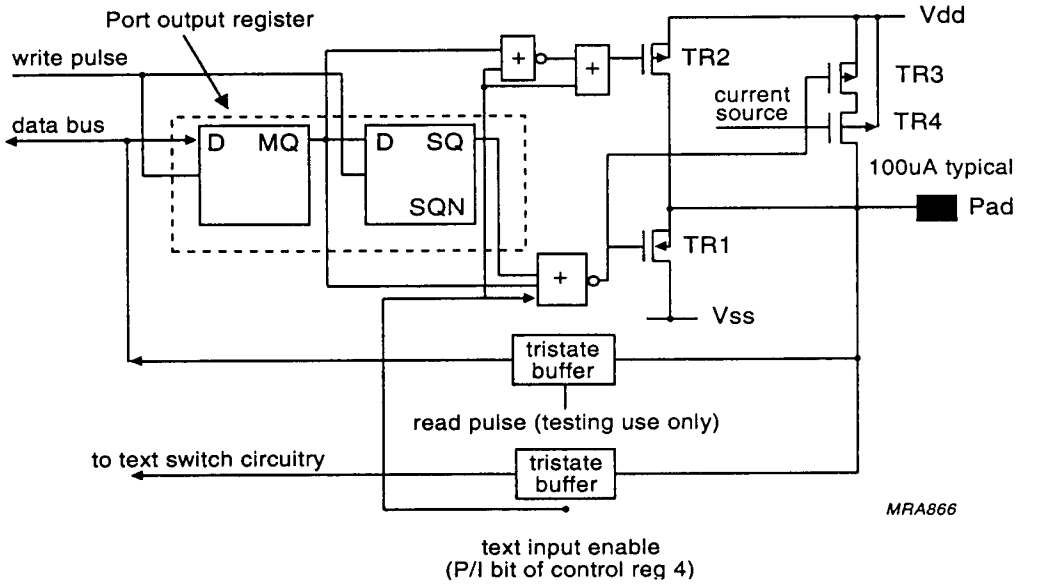


Fig.46 Push-pull output type (option 3).

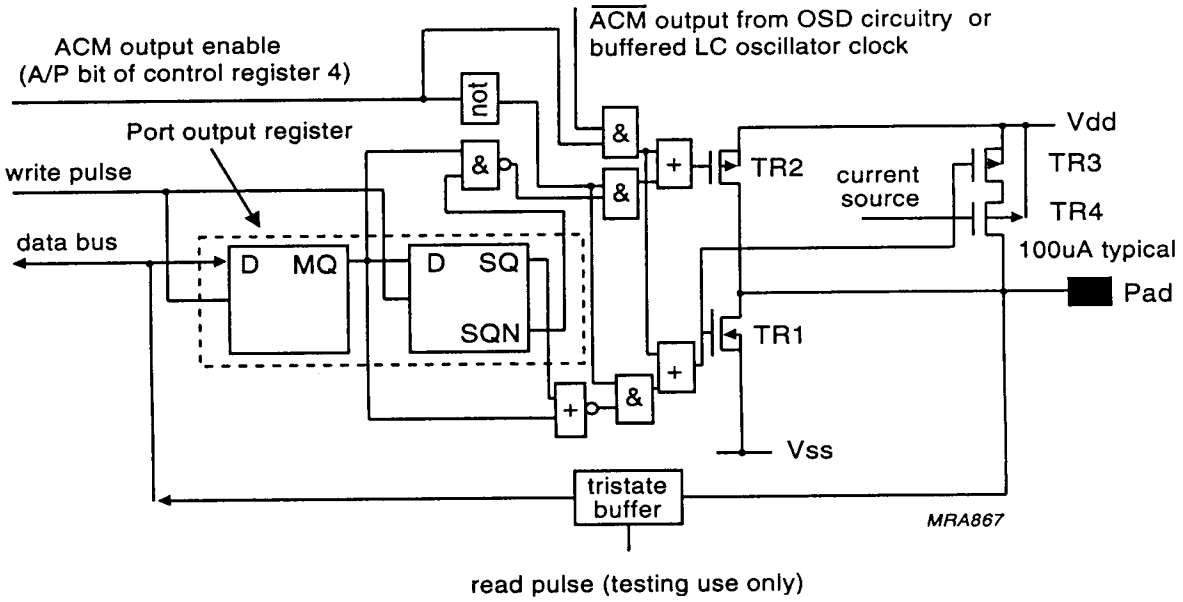


Fig.47 Standard output with switched pull-up current source (option 1)

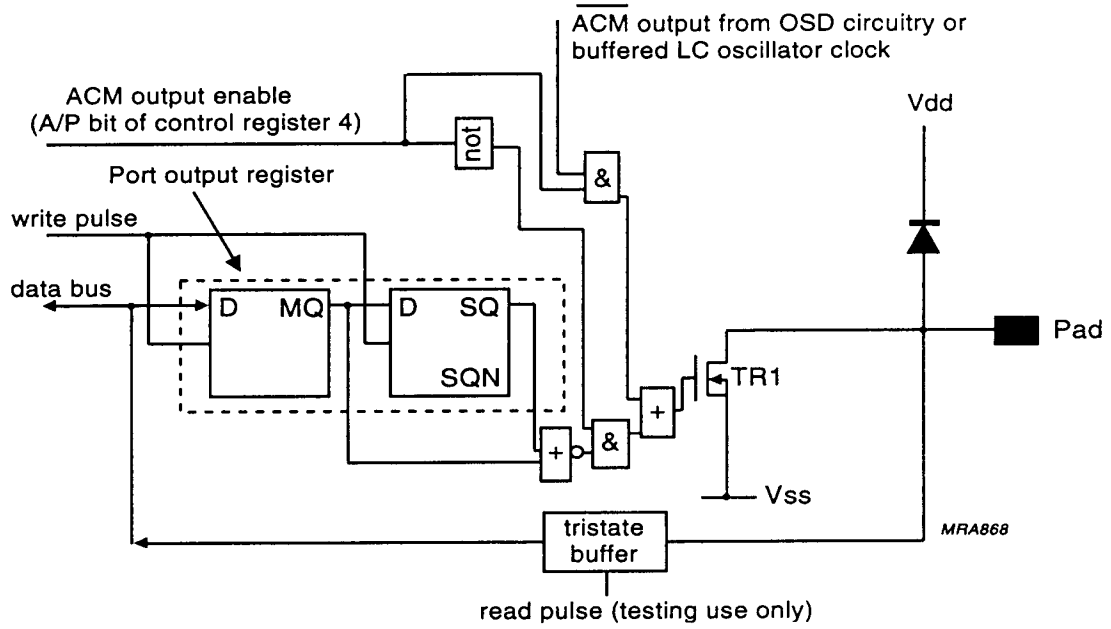


Fig.48 Open drain type I/O (option 2).

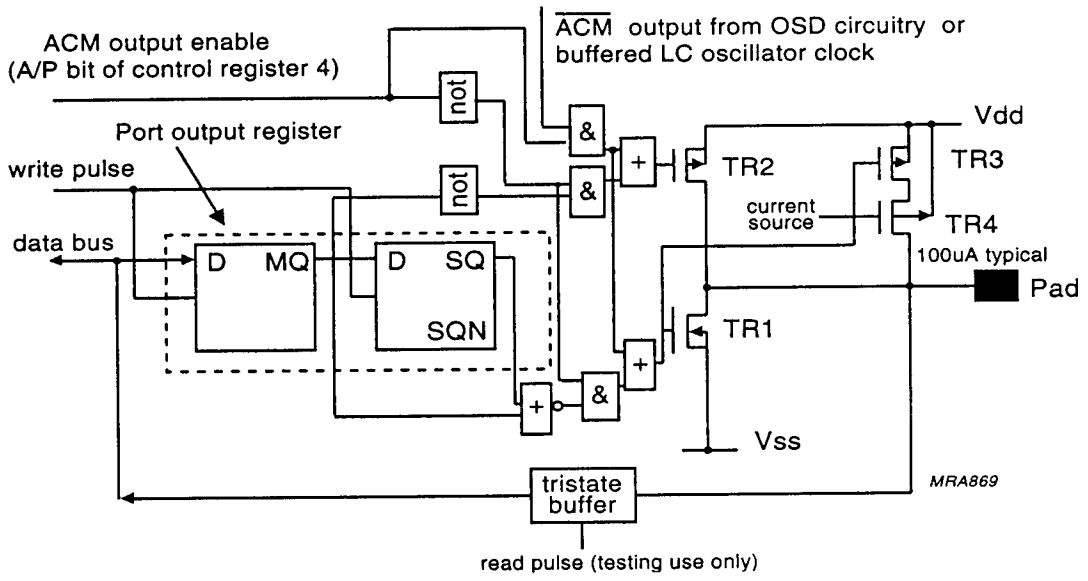


Fig.49 Push-pull type I/O (option 3).

	Pin	Option	Reset/Set
P00	17		
P01	19		
P02	21		
P03	23		
P04	2		
P05	15		
Space code		☐ transparant	☐ opaque

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Fig.50 Port option and after master reset status and space code option.

11 LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	all input voltage	−0.5	V_{DD}+0.5	V
P_{TOT}	total power dissipation	–	500	mW
$-I_{OH}$	maximum source current for all Port lines	–	5	mA
I_{OL}	maximum sink current for all Port lines	–	5	mA
T_{STG}	storage temperature	−55	+125	°C
T_{AMB}	ambient operating temperature range	−20	+70	°C

12 DC CHARACTERISTICS

V_{DD} = 4.5 V; ≈ 5.5 V; V_{SS} 0 V; T_{AMB} = −20 ≈ +70°C; All voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating		4.5	5.0	5.5	V
I_{DD}	supply current operating	V_{DD} = 5 V, F_{XTAL} = 3 MHz, F_{DOSCLC} = 10 MHz	–	5	10	mA
		V_{DD} = 5 V, F_{XTAL} = 3 MHz, F_{DOSCL} = 14 MHz	–	7	14	mA
	supply current operating	V_{DD} = 5 V, F_{XTAL} = 3 MHz, F_{DOSCL} = stop	–	1.0	2.0	mA
RESETN, TEST1, TEST2, HSYNC, VSYNC inputs						
V_{IL}	input voltage LOW		0	–	$0.3V_{DD}$	V
	input voltage HIGH		$0.7V_{DD}$	–	V_{DD}	V
$\pm I_{IL}$	input leakage current	$V_{SS} < V_I < V_{DD}$	0.01	0.20	10	µA
Port P00 - P05 (with combined functions) inputs						
V_{IL}	input voltage LOW		0	–	$0.3V_{DD}$	V
	input voltage HIGH		$0.7V_{DD}$	–	V_{DD}	V
$\pm I_{IL}$	input leakage current	$V_{SS} < V_I < V_{DD}$	–	–	10	µA
Ports P00 - P05 (with combined functions)						
I_{OL}	output sink current LOW	V_{DD} = 5 V, V_O = 0.4 V	5.0	12.0	–	mA
$-I_{OH}$	pull-up output source current HIGH	V_{DD} = 5 V, V_O = $0.7V_{DD}$	40	100	–	µA
	pull-up output source current HIGH	V_{DD} = 5 V, V_O = V_{SS}	–	140	400	µA
	pull-up output source current HIGH	V_{DD} = 5 V, V_O = V_{DD} − 0.4 V	3.0	7.0	–	mA
SDA, SCK inputs						
V_{IL}	input voltage LOW		0	–	$0.3V_{DD}$	V
	input voltage HIGH		$0.7V_{DD}$	–	V_{DD}	V
SDA, SCK outputs (open drain only)						
I_{OL}	output sink current LOW	V_{DD} = 5 V, V_O = 0.4 V	3.0	–	–	mA
R, G, B, I, FB, P04/ACM, P05/CKout outputs						
I_{OL}	push-pull output sink current LOW	V_{DD} = 5 V, V_O = 0.4 V	3.2	5.5	–	mA
$-I_{OH}$	pull-up output source current HIGH	V_{DD} 5 V, V_O $0.7V_{DD}$	40	100	–	µA
	pull-up output source current HIGH	V_{DD} = 5 V, V_O V_{SS}	–	140	400	µA
	push-pull output source current HIGH	V_{DD} = 5 V, V_O = V_{DD} − 0.4 V	1.6	2.4	–	mA

13 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
F_{XTAL}	crystal frequency	V_{DD} = 5 V ± 10%	1.0	3.0	6.0	MHz
F_{DOSCLC}	DOS oscillator for 1V/1H	V_{DD} = 5 V ± 10%	1.0	7.0	10.0	MHz
	DOS oscillator frequency for 1V/2H, 2V/2H scanning mode	V_{DD} = 5 V ± 10%	2.0	12.0	14.0	MHz

14 DEFAULT VALUE OF REGISTERS AFTER MASTER RESET

Unless mentioned below, all the other register's initial values are **not** guaranteed after master reset.

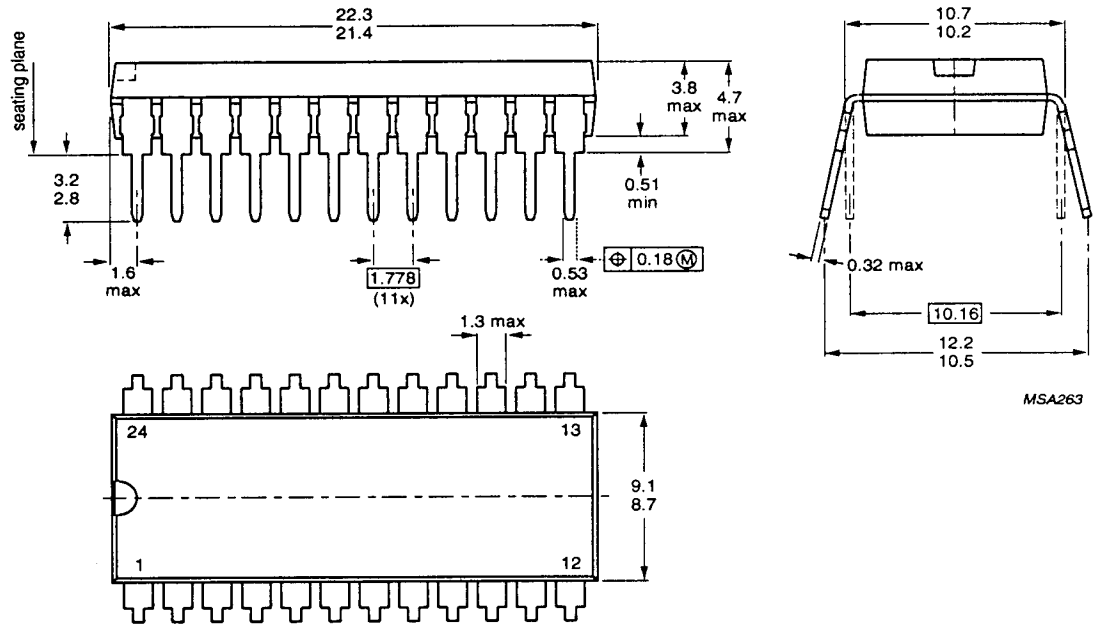
14.1 User directly controllable registers

- BS (Bank select) bit = 0
- EN bit = 0, → OSD is disabled in the initial state It is enabled by setting command 7
- Scanning mode, M1,M0 = 00, → conventional 525 LPF/60 Hz-NTSC and/or 625LPF/50 Hz-PAL
- Bp = 1, → initial state of FB, ACM, R, G, B, I active level is active high
- Hp = 0, → HSYNC active level, initially, is active low
- Vp = 0, → VSYNC active level, initially, is active low
- S1,S0 = 00, → default background mode is "no background or so called superimpose"
- Control register 5, background colour in frame shadowing mode: blue (B = 1, R = G = I = 0)
- A/P = 0, → ACM/P04 pin acts as output Port pin
- C/S = 0, → CK_{OUT}/P05 pin acts as output Port pin
- P/I = 0, → P00/RI, P01/GI, P02/BI and P03/FBI act as output Port pins.

14.2 User indirectly controllable registers

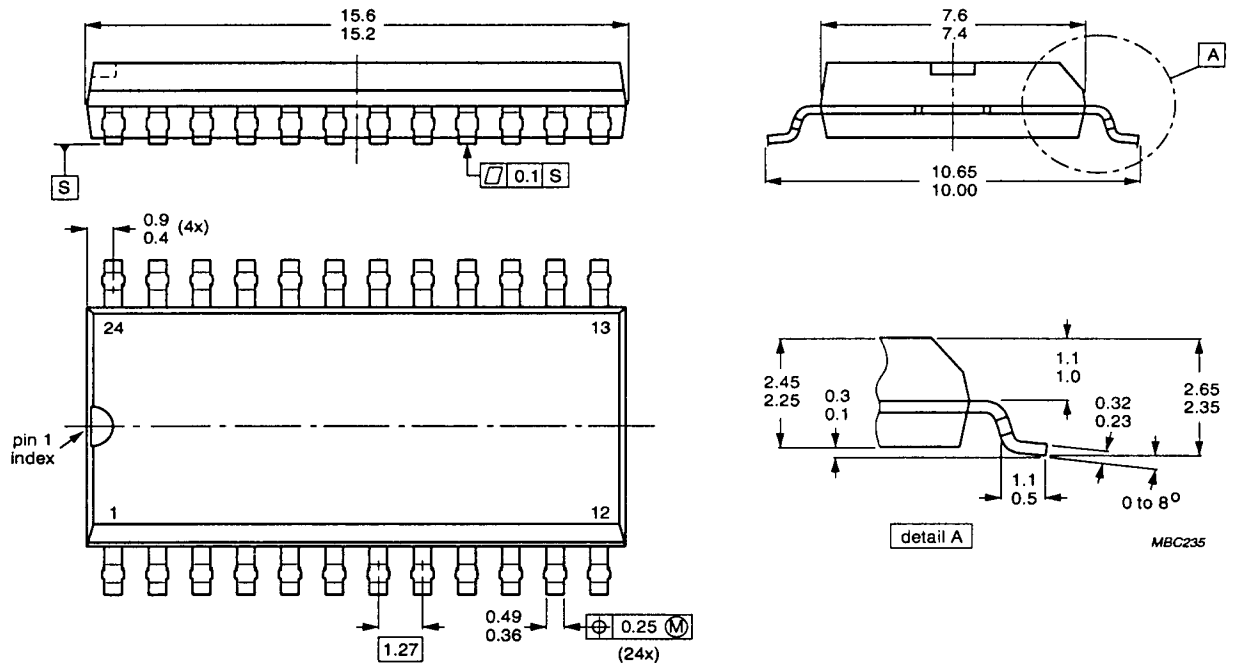
- ACM register = 0, → initial state is ACM output low unless changed by the space code
- Character size register = 00, 1V/1H, → initial state of character size is the 1V/1H unless changed by carriage return code
- Background colour register = blue (B = 1, R = G = I = 0); → unless changed by space code
- "End of display" register = 0, → so display is enabled if EN bit of control register 1 (command 7) is enabled
- Bank Selection register (BS bit of command) = 1.

15 PACKAGE OUTLINE



Dimensions in mm

Fig.51 Plastic shrink DIL, 24-pin (DIL24SHR).



Dimensions in mm

Fig.52 Plastic SOL, 24-pin (SO24L).

16 SOLDERING

16.1 Plastic dual in-line packages

16.1.1 BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.1.2 REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

17 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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