CHIPS

82C201, 82C201-10/82C202/82A203/82A204/82A205
CS8220: PC/AT COMPATIBLE CHIPSet™

- **Fully IBM™ PC AT Compatible**
- **Flexible architecture allows usage in any iAPX 286 design**
- **Early ALE Generation**
- **Early RAS Generation**
- **Low Power CMOS Process Technology for 82C201 and 82C202, and Advance Low Power Schottky Process Technology for 82A203, 82A204 and 82A205**
- **10 or 8 MHz with One Wait State or 6 MHz with Zero Wait State Capability**
- **Complete System Board Memory Decode**
- **Configurable RAM Selects**
- **16 Bit to 8 Bit Conversion Logic**
- **Variable Wait State Selection**
- **24 mA sink and -3.3 mA source current for System Bus outputs**
- **Single 5 Volt Supply**

The CS8220 PC/AT compatible CHIPSet is a 5 chip LSI implementation of most of the MSI/SSI logic used to control the IBM Personal Computer AT. The flexible architecture of the chip set allows it to be used in any iAPX 286 based system design. The 82C201 and 82C202 perform the functions of the Intel 82284 Clock Generator and Ready Interface, 82288 Bus Controller for iAPX286 processors, 8284A Clock Generator and Driver, and replace 30 other MSI/SSI devices in the IBM PC AT design. Significant new features have been added to enhance system performance while still maintaining PC AT compatibility.

The 82C201 is the standard 8 MHz device. The 82C201-10 will operate with a system clock frequency of 10 MHz.

Two signals, ALE and RAS, can be altered with the activation of the Early Mode select line ($\overline{EMODE}$). When $\overline{EMODE}$ is low, both signals become valid before the normal ALE and RAS signals. This allows the use of 120nsec DRAMS in a 6Mhz zero wait state system or 150nsec DRAMS in a 8Mhz one wait state system. The 10 MHz one wait state system using 82C201-10 will require 120 nsec DRAMs. Variable wait state selection is also provided to accommodate slower memories and peripherals where necessary.

The 82A203, 82A204, and 82A205 include most of the buffers and drivers required in an IBM PC AT compatible design. Advanced Schottky Bipolar process technology is used to implement these devices, allowing high speed and high source (-3.3mA) and sink (24mA) current capability.

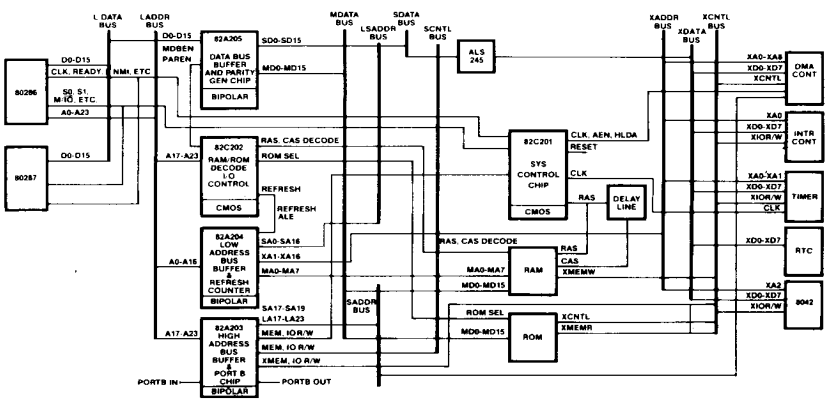
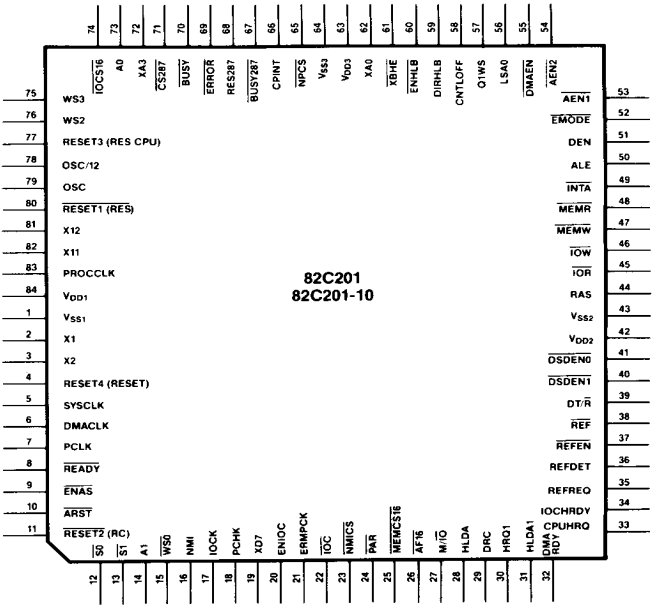
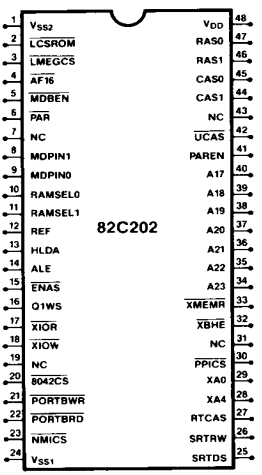
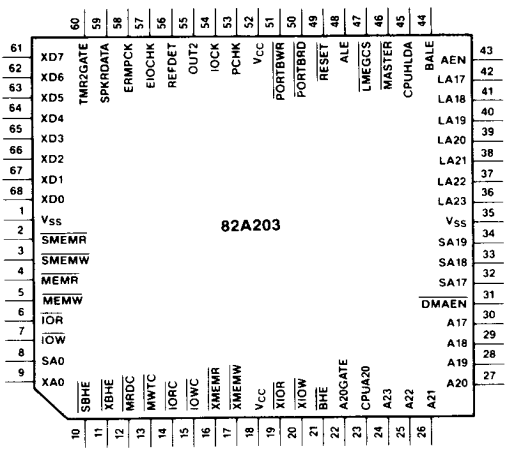


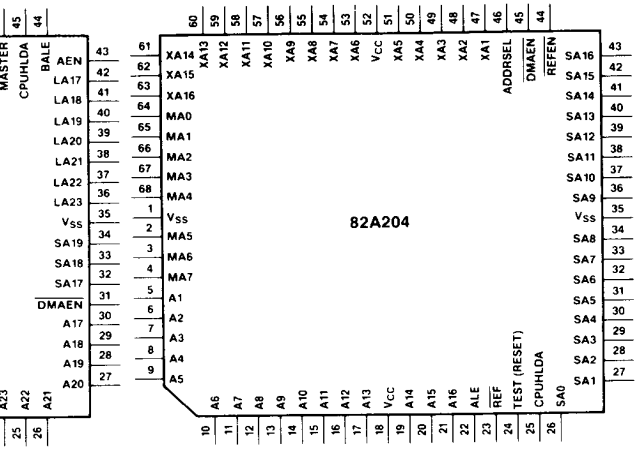
Figure 1. PC/AT Block Diagram

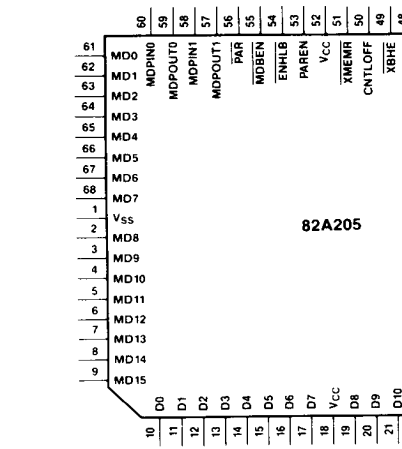
PRINTED IN USA 5M 2/86 REV 3











82C201 Pin Description

Pin No.	Pin Type	Symbol	Pin Description
2,3	I	X1,X2	CRYSTAL Inputs for parallel resonant fundamental mode frequency crystal. The crystal frequency must be twice the processor clock frequency. Alternatively, a TTL clock may be connected to X1.
15	I	$\overline{WS0}$	ZERO WAIT STATE option. When active the memory accesses will have no wait state cycles inserted. For proper operation set-up and hold times to the clock must be met.
12, 13	I	$\overline{S0}$, $\overline{S1}$	STATUS inputs from the CPU. The status signals are used by the bus controller to determine the state of the CPU. Pull-up resistors should be provided on these inputs.
8	O	$\overline{READY}$	$\overline{READY}$ is an active low output indicating that the current bus cycle be completed. Ready is an open collector output requiring an external pull up resistor. S0, S1, WS0 and RESET1 inputs control $\overline{READY}$ output.
80	I	$\overline{RESET1}$	$\overline{RESET1}$ ($\overline{RES}$) is connected to the Power Good signal. When low it will provide a reset signal for the system.
11	I	$\overline{RESET2}$	$\overline{RESET2}$ (RC) is an active LOW input generated by the Universal Peripheral Interface device 8042. It forces a CPU reset by activating RESET3 signal.
77	O	RESET3	RESET3 (RES CPU) is the reset signal to reset the CPU. RESET3 is generated when $\overline{RESET1}$ or $\overline{RESET2}$ inputs become active. RESET3 is also activated when a HALT status is generated by the CPU by forcing M/IO, $\overline{S0}$, $\overline{S1}$ and A1 LOW.
4	O	RESET4	RESET4 (RESET) is generated as a result of $\overline{RESET1}$ becoming active and provides the reset for the system. RESET4 is synchronized with the Processor clock.
83	O	PROCCLK	PROCESSOR CLOCK signal provides the clock for the CPU. It is equal to the crystal frequency on pins X1 and X2.
5	O	SYSCLK	SYSTEM CLOCK is equal to half the PROCCLK and may be used for clocking peripheral devices. It is synchronized to the processor T-states.
6	O	DMACLK	DMA CLOCK is an output running at half the SYSCLK frequency. This clock is synchronized to the CPU T-cycles. It is clock source for the DMA Controller.
7	O	PCLK	PCLK (Peripheral Clock) is half the rate of the PROCCLK. It is used for clocking the peripheral controllers.

82C201 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
9	O	$\overline{ENAS}$	ENABLE ADDRESS STROBE is an active LOW output which enables the Address Strobe input of the Real Time Clock device MC146818. It goes low at the first read status input ($\overline{S1}$ = 0) from the CPU.
14	I	A1	ADDRESS 1 is the demultiplexed address signal from the CPU. It is used to detect the 'SHUT DOWN' condition of the CPU.
73	I	A0	ADDRESS 0 is the address signal from the CPU. It is used to generate the enable signal for the data bus transceivers.
82,81	I	X11,X12	CRYSTAL inputs for the internal oscillator which generates the clock for the I/O devices and other peripherals in the system. A parallel resonant fundamental frequency mode crystal should be connected across the X11, X12 inputs. Alternatively, a TTL clock may be connected to X11.
79	O	OSC	OSCILLATOR output is the clock frequency of the crystal connected across X11, X12.
78	O	OSC/12	OSCILLATOR divide by 12 is an output with a clock frequency equal to 1/12 of the crystal frequency across the X11, X12 inputs.
27	I	M/$\overline{IO}$	MEMORY-INPUT OUTPUT is the M/$\overline{IO}$ signal from the CPU. When HIGH it indicates memory access,when LOW it indicates an I/O access. It is used to generate the Memory andI/O control signals for the system.
49	O	$\overline{INTA}$	INTERRUPT ACKNOWLEDGE is an active LOW output. It is used by the Interrupt Controllers to output the interrupt vector onto the data bus. It is tri-stated when HLDA is active high and CNTLOFF output is low.
45	I/O	$\overline{IOR}$	I/O READ signal for the I/O devices. When LOW it indicates an I/O READ command is in progress. It is tri-stated when HLDA is high and CNTLOFF output is low.
46	I/O	$\overline{IOW}$	I/O WRITE signal for the I/O devices. When LOW it indicates an I/O WRITE command is progress. It is tri-stated when HLDA is high and CNTLOFF output is low.
48	I/O	$\overline{MEMR}$	MEMORY READ COMMAND instructs a memory device to place data on the data bus. $\overline{MEMR}$ is also active low during refresh cycles. It is tri-stated when HLDA is high and CNTLOFF output is low.

82C201 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
47	I/O	$\overline{\text{MEMW}}$	MEMORY WRITE COMMAND instructs a memory device to read the data on the data bus. It is tri-stated when HLDA is high and CNTLOFF output is low.
50	O	ALE	ADDRESS LATCH ENABLE is an active HIGH signal and controls the address latches used to hold the address during a bus cycle. ALE is not issued for halt bus cycle.
44	O	RAS	RAS is an active HIGH output. It is used to generate the RAS and CAS signals for memory accesses.
39	O	DT/$\overline{\text{R}}$	DATA TRANSMIT/RECEIVE determines the data direction to and from the local data bus. A HIGH indicates a write bus cycle and a LOW indicates a READ bus cycle. DEN output is always inactive when DT/$\overline{\text{R}}$ changes state. DT/R is HIGH when no bus cycle is active.
51	O	DEN	DATA ENABLE is an active HIGH output. When active it enables the data transceivers connected to the local bus.
41	O	$\overline{\text{DSDEN0}}$	DATA STROBE DATA ENABLE 0 is an active LOW output. When active it enables the data transceivers connected to the low byte (D0-D7) data bus. This signal is active when DEN is high. Also an active Numerical Processor Chip Select will disable this output.
40	O	$\overline{\text{DSDEN1}}$	DATA STROBE DATA ENABLE 1 is an active LOW output. When active it enables the data transceivers connected to the high byte (D8-D15) data bus. This signal is active when DEN is high. Also an active Numerical Processor Chip Select will disable this output.
61	I/O	$\overline{\text{XBHE}}$	BUS HIGH ENABLE is an active LOW signal which enables the high byte data bus signals to pass through the data bus transceivers.
62	I/O	XA0	ADDRESS 0 when active decodes the cascaded Interrupt Controller's command words issued by the CPU. The XA0 works in conjunction with the read, write and chip select inputs of the interrupt controller and determines whether the CPU wishes to issue a command or read the status of the controller.
72	I	XA3	ADDRESS 3 is used for generating the chip select and reset signals for the 80287.
71	I	$\overline{\text{CS287}}$	CHIP SELECT 287 is an active LOW input used to generate the Numerical Processor Select NPCS for the 80287.

82C201 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
65	O	$\overline{\text{NPCS}}$	NUMERICAL PROCESSOR CHIP SELECT is active LOW output and is used as the Numerical Processor Select NPS1 for the 80287.
70	I	$\overline{\text{BUSY}}$	BUSY is an active LOW input from the 80287 to indicate that it is currently executing a command. It is used to generate the Busy signal for the processor.
67	O	$\overline{\text{BUSY287}}$	BUSY 287 is an active LOW output for the processor. It indicates to the processor the operating condition of the Coprocessor.
69	I	$\overline{\text{ERROR}}$	ERROR is an active LOW input from the Numeric Processor indicating that an unmasked error condition exists.
66	O	CPINT	COPROCESSOR INTERRUPT is an active HIGH output. It is the Interrupt Request from the Numeric Coprocessor and is connected to the Interrupt Request 13 of the Interrupt Controller.
68	O	RES287	RES287 is an active HIGH output and is used to reset the Numeric Processor.
26	I	$\overline{\text{AF16}}$	AF16 is an active LOW input signal which should be asserted when 16 bit memory acceses are made. It is used to inhibit the command delays for memory accesses by the I/O devices.
25	I	$\overline{\text{MEMCS16}}$	MEMORY CHIP SELECT is an active low signal. It is active for a 16-bit, 1 wait-state memory cycle. It must be obtained by decoding LA17-LA23 address lines.
30	I	HRQ1	HOLD REQUEST 1 is an active HIGH signal from the DMA controller. It is used to generate the CPU Hold Request signal.
33	O	CPUHRQ	CPU HOLD REQUEST is an active HIGH output for the CPU for DMA transfers by the DMA controller. It is also active during refresh cycles.
28	I	HLDA	HOLD ACKNOWLEDGE is an active HIGH input generated by the CPU, granting a DMA cycle to the DMA controller. HLDA active forces all commands, IOR, IOW, MEMR, MEMW, and INTA, to be tri-stated provided the CNTLOFF output is low.
31	O	HLDA1	HOLD ACKNOWLEDGE 1 is an active HIGH ouput providing the Hold Acknowledge signal for the DMA controller.
74	I	$\overline{\text{IOCS16}}$	I/O CHIP SELECT is an active low signal. It is active for a 16-bit, 1 wait-state I/O cycle.

82C201 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
53	I	$\overline{AEN1}$	ADDRESS ENABLE 1 is an active LOW signal from one of the two DMA controllers to enable the address latches holding the address. It is active for 8-bit data transfers.
54	I	$\overline{AEN2}$	ADDRESS ENABLE 2 is an active LOW signal from one of the two DMA controllers to enable the address latches holding the address. It is active for 16 bit data transfers.
52	I	$\overline{EMODE}$	EARLY MODE is an input which selects between the Early generation of ALE and RAS signals or normal generation of the ALE and RAS signals. A LOW input will select the EARLY mode and a HIGH input will select the Normal mode.
76	I	WS2	TWO WAIT STATES option. When active the I/O acceses will have two wait states inserted. WS2 may be generated by I/O address decoders.
75	I	WS3	THREE WAIT STATES option. When active the I/O acceses will have three wait states inserted. WS3 may be generated by I/O address decoders.
59	O	DIRHLB	DIRECTION FOR HIGH TO LOW BYTE and low to high byte conversion during data transfers to and from the 8 bit peripherals. This signal is also referred to as DIR245.
58	O	CNTLOFF	CONTROL OFF is an active HIGH output which is used to enable the low byte data bus latch during byte accesses. When CNTLOFF is low, HLDA active tri-states all command outputs.
60	O	$\overline{ENHLB}$	ENABLE HIGH TO LOW byte performs the high to low byte conversion with the DIR HLB signal. Conversion does not take place if A0 = 0 which indicates word transfers. This signal is also referred to as as Gate 245.
55	O	$\overline{DMAEN}$	DMA ADDRESS ENABLE is an active LOW signal and is active when any I/O device is making a DMA access to the system memory.
34	I	IOCHRDY	I/O CHANNEL READY signal is generated by an I/O device. When LOW it indicates a 'not ready' condition and forces the insertion of wait states in I/O or Memory accesses by the I/O device. When HIGH it will allow the completion of a memory or an I/O access by the I/O device.

82C201 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
32	O	DMARDY	DMA READY signal for the DMA Controller used to extend memory read and write cycles from the DMA controller for slower memories or I/O devices. When low it inserts wait states.
35	I	REFREQ	REFRESH REQUEST INPUT is an input indicating that a refresh cycle be initiated for the dynamic RAMs. This signal is obtained from the Timer controller, 8254, and provides a refresh request every 15 microseconds.
36	O	REFDET	REFRESH DETECT is an output which changes state when a refresh cycle is being initiated. It may be used externally to monitor the state of the refresh cycle execution.
38	I/O	$\overline{\text{REF}}$	REFRESH is an open drain active LOW signal. It is used to initiate a refresh cycle for the dynamic RAMs. As an input it can used to force a REFRESH cycle from an I/O device. An external pull up is required on this pin.
37	O	$\overline{\text{REFEN}}$	REFRESH ENABLE is an active LOW output which is used to start a refresh counter which provides addresses for the dynamic RAM refresh cycle.
56	O	LSA0	ADDRESS 0 for system bus which is forced LOW for word accesses.
57	O	Q1WS	ONE WAIT STATE is an active high output which goes active during phase 2 (O2) of the CPU bus cycle following the Ts state. It can be used externally to extend the READ or WRITE cycles for slower I/O devices.
29	I	DRC	DMA READY CLOCK is an active HIGH input and is used to generate the DMA READY signal for the DMA controllers.
10	I	$\overline{\text{ARST}}$	ASYNCHRONOUS RESET is an active, LOW input. Under normal configurations, it should be tied to a 10K pull-up resistor. It resets the chip to a known state, and is used for testing purposes only.
23	I	$\overline{\text{NMICS}}$	NON-MASKABLE INTERRUPT CHIP SELECT input is active LOW. When active it enables the NMI to the CPU.
19	I	XD7	DATA BUS BIT 7 of the peripheral data bus, is used to generate the Non-Maskable Interrupt for the CPU.
16	O	NMI	NON-MASKABLE INTERRUPT is an active HIGH output and is connected to the NMI of the CPU.

82C201 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
22	I	$\overline{IOC}$	I/O CHECK is an active LOW input. It is used to signal an Error condition from an I/O device. When active it generates the IOCK output if Enable I/O Check input was active.
17	O	IOCK	I/O CHECK output is activated when an I/O Check ($\overline{IOC}$) input is activated. Enable I/O Check must be active for IOCK to be generated. The IOCK is used to generate the Non-Maskable Interrupt for the CPU, and is also stored in PORT B as one of the status bits.
20	I	ENIOC	ENABLE I/O CHECK is the enable input for the I/O Check logic. It enables the generation of the IOCK output when $\overline{IOC}$ is active.
24	I	$\overline{PAR}$	PARITY error is Active LOW input and generates the Parity Check PCHK output.
21	I	ERMPCK	ENABLE RAM PARITY CHECK is an active HIGH input used to enable the parity check logic.
18	O	PCHK	PARITY CHECK is an active HIGH output active when a parity check is detected. It is used to generate the Non-Maskable Interrupt for the CPU.
42,63,84	—	V_{DD}	Power Supply.
1,43,64	—	V_{SS}	Ground.

82C202 Pin Description

Pin No.	Pin Type	Symbol	Pin Description
40-34	I	A17-A23	ADDRESS BUS inputs from the processor address bus.
12	I	REF	REFRESH is an active HIGH input and initiates a refresh cycle for the dynamic RAMs.
10,11	I	RAMSEL0 RAMSEL1	RAM SELECT 0 and 1 select the 256K, 512K or 1024K RAM option. The select logic works as follows: RAMSEL0 RAMSEL1 RAM MEMORY 0 0 256K 0 1 640K 1 0 512K 1 1 1024K
13	I	HLDA	HOLD ACKNOWLEDGE is an active HIGH input from the processor. When active it indicates that the processor has relinquished the system bus in favour of another bus master in the system. It is used to latch the internally generated RAS/CAS signals into appropriate outputs.
14	I	ALE	ADDRESS LATCH ENABLE is an active HIGH input and latches the low order address signals from a multiplexed bus into the address registers. It is used to latch the internally generated RAS/CAS signals into appropriate outputs.
33	I	$\overline{\text{XMEMR}}$	MEMORY READ is an active LOW input from a peripheral device instructing the memory to place its data on the data bus. It is used to generate the direction signal for the data bus buffers holding the data bus signals.
42	I	$\overline{\text{UCAS}}$	USER CAS is an active LOW input and is used to enable parity generation logic when addressing memory which is selected by logic external to the 82C202. It is usually connected to the CAS generated externally for memory beyond what is addressable by the 82C202. When active it enables parity generation/ check for the externally selected memory.
41	O	PAREN	PARITY ENABLE is an active HIGH output. It is active during the parity check cycle.
29	I	XA0	ADDRESS 0 is the address 0 signal on the address bus. It is used to detect the parity error on low or high memory data byte.
32	I	$\overline{\text{XBHE}}$	BUS HIGH ENABLE signal is used in the same way as XA0 to generate the parity error for the low or high memory data byte.
47, 46	O	RAS0, RAS1	ROW ADDRESS SELECT 0 and 1 are used for selecting RAM banks. The RAS0 selects the lower memory bank,and RAS1 selects the high memory bank.

82C202 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
45, 44	O	CAS0, CAS1	COLUMN ADDRESS SELECT 0 and 1 are used to select the low and high byte access signals for the RAM access cycles.
4	O	$\overline{AF16}$	AF16 is an active LOW output indicating a word memory access. It is used to generate Command Delay control signal for delaying READ or WRITE commands for slower peripherals or I/O devices.
3	O	$\overline{LMEGCS}$	LOW MEG CHIP SELECT is an active LOW output which is active when low memory address space, 0-1.024 Megabyte, is accessed. It can be used to disable certain read or write signals on the I/O connector if accesses are made beyond one mega-byte address space.
2	O	$\overline{LCSROM}$	ROM CHIP SELECT is an active LOW output which is active when the ROM/PROM/EPROM space is accessed. It can be used to generate the chip select inputs for the non-volatile devices in the system.
5	O	$\overline{MDBEN}$	MEMORY DATA BUS ENABLE is an active LOW output. It is used to set the direction on the data bus buffers which drive the data bus between the system and the memory devices.
30	I	$\overline{PPICS}$	PROGRAMMABLE PERIPHERAL INTERFACE CHIP SELECT is an active LOW input. It is active when the Peripheral Interface Device 8042 is selected. It is used to generate the Chip Select signal for the 8042.
20	O	$\overline{8042CS}$	8042 CHIP SELECT is an active LOW signal for the 8042 device. It is selected when $\overline{PPICS}$ is active.
28	I	XA4	ADDRESS 4 is the address 4 of the CPU address bus. It is used to generate the chip selects and data strobes for other peripherals in the system.
17,18	I	$\overline{XIOR}$, $\overline{XIOW}$	I/O READ AND WRITE are active LOW inputs and are active whenever a read or write cycle is performed with an I/O device. They are used to generate the read and write signals for the peripherals or other I/O ports on the system.
22,21	O	$\overline{PORTBRD}$, $\overline{PORTBWR}$	READ and WRITE signals for the I/O port are active LOW outputs. They are generated when an Port B is either 'read' or 'written' to.
15	I	$\overline{ENAS}$	ENABLE ADDRESS STROBE is an active LOW input and is used to generate the address strobe signal for the real time clock device MC146818.
27,25	O	RTCAS, SRTDS	REAL TIME CLOCK ADDRESS STROBE and DATA STROBE outputs for the real time clock MC146818.

82C202 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
26	O	SRTRW	REAL TIME CLOCK READ/WRITE output for the real time clock device MC146818. A HIGH state indicates a 'read' operation and a LOW state means a 'write' operation.
16	I	Q1WS	Q1 WAIT STATE is an active HIGH input and is used to extend the Real Time Clock Address strobe by one wait state.
23	O	$\overline{\text{NMICS}}$	NMI CHIP SELECT is an active LOW output. It may be used to enable the Non-Maskable Interrupt to the processor.
9,8	I	MDPIN0, MDPIN1	MEMORY DATA PARITY INPUT 0,1 for parity on LOW and HIGH bytes of memory.
6	O	$\overline{\text{PAR}}$	PARITY is an active LOW output. This latched output is active when an even parity error is detected on either the LOW or HIGH byte memory access.
48	—	V_{DD}	Power Supply.
1,24	—	V_{SS}	Ground.
7,19,31,43		N.C.	Not Connected.

82A203 Pin Description

Pin No.	Pin Type	Symbol	Pin Description
1	—	V_{SS}	Ground.
2	O	$\overline{\text{SMEMR}}$	Memory Read command for the expansion bus. It is active when low 1 Megabyte memory space is addressed.
3	O	$\overline{\text{SMEMW}}$	Memory Write command for the expansion bus. It is active when low 1 Megabyte memory space is addressed.
4	I/O	$\overline{\text{MEMR}}$	Memory Read command for the extended expansion bus. It is active on all memory read cycles.
5	I/O	$\overline{\text{MEMW}}$	Memory Write command for the extended expansion bus. It is active on all memory write cycles.
6	I/O	$\overline{\text{IOR}}$	Input/Output Read command for the expansion bus. The read cycle can be initiated by the CPU or DMA controller, or by a DMA controller resident on the I/O channel.
7	I/O	$\overline{\text{IOW}}$	Input/Output Write command for the expansion bus. The write cycle can be initiated by the CPU or DMA controller, or by a DMA controller resident on the I/O channel.
8	I/O	SA0	Address 0 of the CPU bus. The I/O pin outputs the A0 from the CPU during local CPU cycles. The expansion bus can force the A0 on this pin during the period when another master on the expansion bus has the control.
9	I/O	XA0	Address 0 from the local I/O bus. In DMA cycle the XA0 is forced by the DMA controller. During CPU read cycle the XA0 is forced by the CPU.
10	I/O	$\overline{\text{SBHE}}$	Bus High Enable signal from or to the Expansion Bus is active when the high byte transfer is taking place.
11	I/O	$\overline{\text{XBHE}}$	Bus High Enable to or from the peripheral bus is active when high byte transfer is taking place.
12	I/O	$\overline{\text{MRDC}}$	Memory Read is the read signal generated by the CPU through the 82C201 to indicate a memory read cycle by the CPU.
13	I/O	$\overline{\text{MWTC}}$	Memory Write is the write signal generated by the CPU through the 82C201 to indicate a memory write cycle by the CPU.
14	I/O	$\overline{\text{IORC}}$	Input Output Read signal generated by the CPU through the 82C201 to indicate an I/O Read cycle.
15	I/O	$\overline{\text{IOWC}}$	Input Output Write signal generated by the CPU through the 82C201 to indicate an I/O Write cycle.

82A203 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
16	I/O	$\overline{\text{XMEMR}}$	Memory Read signal from and to the peripheral bus. The Read is forced (as an output) by the CPU during read of the peripheral devices. The DMA controller forces this pin as input to read data from a memory location or memory to memory transfer.
17	I/O	$\overline{\text{XMEMW}}$	Memory Write signal from and to the peripheral bus. The Write is forced (as an output) by the CPU during write to the peripheral devices. The DMA controller forces this pin as input to write data to a memory location or memory to memory transfer.
18	—	V_{CC}	5V Power Supply.
19	I/O	$\overline{\text{XIOR}}$	I/O Read signal for the peripheral bus. As an output it is used to Read the internal registers of the peripheral controllers. As an input it is forced by the DMA controllers to access data from a peripheral device.
20	I/O	$\overline{\text{XIOW}}$	I/O Write signal for the peripheral bus. As an output it is used to write to the internal registers of the peripheral controllers. As an input it is forced by the DMA controller to write data to a peripheral device.
21	I	$\overline{\text{BHE}}$	Bus high Enable signal is connected to $\overline{\text{BHE}}$ output of the CPU. It indicates the transfer of data on the upper half of the data bus. In conjunction with the A0 polarity it determines whether the access is on a word or byte boundary. The coding of BHE and A0 follows the 80286 coding scheme.
22	I	A20GATE	A20 Gate is used to force A20 LOW. When A20GATE is LOW A20 on the CPU address bus is forced LOW. When A20GATE is high, A20 is transmitted as generated by the CPU.
23	I	CPUA20	CPU A20 is the CPU address 20. It is transmitted as A20 after being conditioned by the A20GATE signal.
24-30	I/O	A23-A17	A23-A17 are the Address bits 17 through 23 of the CPU address bus. As input these pins are forced by the CPU address bus. As outputs the expansion bus address lines A17-A23 are output on these pins.
31	I	$\overline{\text{DMAEN}}$	DMA Address Enable is used to condition the transceivers for the peripheral control signals. When LOW it allows the DMA control signals (MEMR, MEMW, I/OR, I/OW, XA0) to be output on the system control bus.
32-34	O	SA17-19	System address bus addresses 17–19 are output to the expansion bus during a memory or an I/O cycle.
35	—	V_{SS}	Ground.

82A203 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
36-42	I/O	LA23-17	System address bus A17-23 is controlled by the MASTER signal. When MASTER is LOW the expansion I/O bus forces the A17-A23 addresses on the local system bus. When MASTER is HIGH the system board forces the addresses on the expansion bus. LA17-LA23 gives the system up to 16 Mbytes of addressability. LA17-LA19 are valid when bus ALE signal, BALE, is high. LA17-LA19 are not latched during CPU cycles and do not stay valid for the entire cycle. They are used to generate memory decodes for 1 wait-state memory cycles. The I/O add-on adapter boards must latch these signals on the falling edge of BALE signal.
43	O	AEN	Address Enable is an output signal for the expansion bus. When LOW it indicates that another MASTER on the expansion bus has made a request by activating MASTER.
44	O	BALE	Buffered Address Latch Enable is a buffered ALE signal for the devices on the expansion bus. SA0-SA19 are latched on the falling edge of BALE. During DMA cycles, BALE is forced high.
45	I	CPUHLDA	CPU Hold Acknowledge signal is used to control the direction of the address and control signal transceivers. A HIGH on the CPU HLDA is interpreted as a DMA cycle.
46	I	$\overline{\text{MASTER}}$	Master is generated by the devices on the expansion bus. A LOW indicates that another device on the expansion bus is active. After MASTER is forced low by an I/O device, the I/O CPU must wait for one system clock period before forcing the address and data lines. The MASTER signal must not be held low for more than 15 microseconds, or else data in the system memory may be lost due to lack of a refresh cycle.
47	I	$\overline{\text{LMEGCS}}$	Low Megabyte Chip Select is generated by 82C202. When active, it indicates that low megabyte memory address space is being accessed.
48	I	ALE	Address Latch Enable is obtained from the 82C201. It is used to generate the buffered ALE signal for the expansion bus, and to latch the address bus signals.
49	I	$\overline{\text{RESET}}$	Reset is used to reset the Port B latch. Reset is active LOW.
50	I	$\overline{\text{PORTBRD}}$	Port B Read is active when the CPU reads PORT B latch, which stores the status conditions.

82A203 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Pin Description
51	I	$\overline{\text{PORTBWR}}$	Port B Write is active when the CPU outputs the data to the PORT B latch.
52	—	V_{CC}	5 Volt Power Supply.
53	I	PCHK	Parity Check is generated by the 82C201 and can be read on a PORT B Read command.
54	I	IOCK	I/O Channel Check is generated by the 82C201. It can be read by a read to the PORT B.
55	I	OUT2	OUT2 is the output from the Timer 8254. It can be read by a read to the PORT B.
56	I	REFDET	Refresh Detect is generated by the 82C201. It can be read by a read to the PORT B.
57	O	EIOCHK	Enable I/O Check is an output which is used to enable the I/O Check ($\overline{\text{IOC}}$) from the I/O expansion bus to be latched into the 82C201.
58	O	ERMPCK	Enable RAM Parity Check is generated for the 82C201. It allows the 82C201 to latch the parity error and output it as PCHK signal for the 82A203.
59	O	SPKRDATA	Speaker data is an output which is used to allow the 8254 tone signal to be output to the speaker.
60	O	TMR2GATE	Timer 2 Gate signal enables the timer on 8254 Timer to generate the tone signal for the speaker.
68–65 64–61	I/O O	XD0-XD3 XD4-XD7	Data Bus 0–7 for the peripheral bus. XD0-XD3 are used as inputs to PORT B Latch and outputs from PORT B status buffer. XD4-XD7 are outputs only from PORT B status buffer.

82A204 Pin Description

Pin No.	Pin Type	Symbol	Description
1	—	V_{SS}	Ground.
64-68 2-4	O O	MA0-MA4 MA5-MA7	Address signals 0-7 for addressing the memory.
5-17 19-21	I I	A1-A13 A14-A16	Address signals 1-16 from the CPU for addressing the memory.
18	—	V_{CC}	5 Volt Power Supply.
22	I	ALE	Address Latch Enable from the 82C201.
23	I	$\overline{REF}$	Refresh is generated by the 82C201 to initiate a refresh cycle for the DRAMs.
24	I	TEST (RESET)	Test, when HIGH, resets the refresh counter and tri-states the memory addresses MA0-7. This will allow another device to access the memory. In normal operation the TEST pin must be pulled LOW.
25	I	CPUHLDA	CPU Hold Acknowledge is generated by the CPU in response to a Hold Request from a DMA controller. The 82A204 uses it to tri-state the SA bus, allowing the XA bus to drive the address bus.
26	O	SA0	Address 0 for the refresh memory.
27-34 36-43	I/O I/O	SA1-8 SA9-16	System addresses 1-16 for the expansion bus.
35	—	V_{SS}	Ground.
44	I	$\overline{REFEN}$	Refresh Enable is generated by the 82C201 and allows a refresh cycle to be initiated.
45	I	$\overline{DMAEN}$	DMA Enable is generated by the 82C201 when a DMA cycle is underway. It is used by the 82A204 to condition the address transceiver in the proper direction.
46	I	ADDRSEL	Address Select is used to multiplex the memory address between the system addresses and the addresses generated by the refresh counter.
47-51 53-63	I/O I/O	XA1-5 XA6-16	Peripheral addresses 1-16 for the local I/O bus.
52	—	V_{CC}	5 Volt Power Supply.

82A205 Pin Description

Pin No.	Pin Type	Symbol	Description
1	—	V_{SS}	Ground.
61-68 2-9	I/O I/O	MD0-7 MD8-15	Memory data bus for the on board memory.
10-17 19-26	I/O I/O	D0-D7 D8-D15	CPU data bus signals from/to the CPU.
18	—	V_{CC}	5 Volt Power Supply.
27-34 36-43	I/O I/O	SD0-SD7 SD8-15	System Data bus for the expansion bus. Its direction is determined by DT/$\overline{R}$ signal from the 82C201.
35	—	V_{SS}	Ground.
44	I	DIRHLB	DIRHLB is generated by the 82C201 and controls the direction of low to high byte conversion during data transfers to and from 8 bit peripherals.
45	I	DT/$\overline{R}$	Data Transmit/Receive is generated by the 82C201. It determines direction of data to and from the memory. A HIGH on the pin indicates a write cycle and a LOW indicates a read cycle.
46, 47	I	$\overline{DSDEN0}$ $\overline{DSDEN1}$	Data Strobe Enable 0 and 1 are generated by the 82C201. These signals enable the data transceivers connected to the LOW and HIGH data bytes.
48	I	XA0	XA0 is address signal 0 for the peripheral bus. It is generated by the 82A203. It is used to condition the bus transceiver for the memory data bus.
49	I	$\overline{XBHE}$	XBHE is the Bus High Enable signal generated by the 82A203. It is used to condition the bus transceiver for the memory data bus, and is active during a high byte transfer.
50	I	CNTLOFF	Control Off is generated by the 82C201 and is used to enable low byte data bus latch during byte access.
51	I	$\overline{XMEMR}$	Memory Read is generated by the 82A203 and is used to enable the parity generation logic on the device, and to set the direction on the output transceiver for the memory data bus.
52	—	V_{CC}	5 V Power Supply.
53	I	PAREN	Parity Enable allows the parity check to be done on parity on the parity bit read from the memory.
54	I	$\overline{ENHLB}$	$\overline{ENHLB}$ enables the high to low byte conversion in conjunction with DIRHLB signal. It is generated by the 82C201.

82A205 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Description
55	I	$\overline{\text{MDBEN}}$	Memory Data Bus Enable is generated by the 82C202. It enables the data bus transceivers connected to the memory devices.
56	O	$\overline{\text{PAR}}$	Parity signal, when active, signifies a parity error on a memory read cycle.
59,57	I	MDPOUT0, MDPOUT1	Memory Data Parity Out 0 and 1 are the parity bits read from the memory banks 0 and 1. They are used to compute the parity during a ready cycle.
60, 58	O	MDPIN0, MDPIN1	Memory Data Parity In 0 and 1 are the parity bits written to the memory banks 0 and 1 during a memory write cycle.

Functional Description 82C201

The 82C201 block diagram is illustrated in Figure 2. The device consists of the following functional blocks:

- Clock Generation and Reset/Ready Synchronization
- Command and Control Signal Generation
- Conversion Logic
- Wait State Control
- DMA and Refresh Logic
- Numerical Processor Control
- NMI and Error Logic

Clock Generation and Reset/Ready Synchronization

The Clock Generation circuitry contains the two oscillators used to generate the system clock signals. Both oscillators are designed to use an external, parallel resonant fundamental mode crystal to generate the basic operating frequency. Crystal connections for the CPU Clock oscillator are made to pins X1 and X2. The X11 and X12 pins are used for generating the Video Clock. The CPU Clock oscillator crystal frequency should be twice the CPU operating frequency (e.g. 12Mhz crystal for a 6 Mhz CPU). For the IBM PC AT, a 14.31818 Mhz crystal should be used with the Video Clock oscillator to maintain compatibility. The 14.31818 Mhz crystal may require a trimmer capacitor in series with the crystal. The trimmer capacitor can then be adjusted to eliminate unwanted color shifts in video signals. Recommended circuits and crystal specifications for both oscillators are shown in Figure 3.

Two clock signals are derived from the Video Clock oscillator, the 14.31818 Mhz clock (14MHz) to the expansion connectors for the system bus and the OSC/12 clock for the counter timer. The OSC/12 clock is generated internally by dividing the 14.31818 Mhz signal from the oscillator by twelve. Due to the possibility of heavy loading, the 14 Mhz clock should be externally buffered before being routed to the expansion connectors.

The remaining 82C201 clocks are derived from the CPU Clock oscillator. These clocks are used throughout the system board and determine the speed at which the computer operates.

PROCCLK is a clock output which is intended to drive both the CPU and the Numerical Processor. The PROCCLK output has a frequency equal to that of the CPU Clock oscillator crystal. The PROCCLK output buffer has sufficient drive capability to meet the 3.8 volt minimum V_{IH} requirement of the 80286/80287 clock inputs, and may be used to drive them directly.

SYSCLK and DMACLK are system clock signals whose output frequencies are ½ and ¼ the PROCCLK oscillator, respectively. Immediately after Reset, the SYSCLK and DMACLK signals are held in a LOW state and will not begin operating until after the CPU asserts Status (S1=0) at the beginning of the first bus cycle. SYSCLK will then make its first low to high transition on the falling edge of PROCCLK in Phase 1 of the next CPU bus cycle following T_S. SYSCLK and DMACLK are now synchronized to the CPU's internal clock, and SYSCLK will provide a low to high transition at the beginning of each Phase 1 while DMACLK makes this same transition on alternate Phase 1 cycles. An illustration of the DMACLK/SYSCLK start-up from Reset is shown in 82C201 reset timing diagrams.

The remaining clock signal, PCLK, also has a frequency equal to ½ of the frequency of PROCCLK. The difference between this signal and SYSCLK is that PCLK has no phase relationship to the CPU's internal clock. PCLK becomes active immediately after $\overline{ARST}$ is deasserted. $\overline{ARST}$ is a seperate reset line which clears both the PCLK and OSC/12 dividers and should, for normal operation, be tied to the same signal as the $\overline{RESET1}$ input. Alternately, $\overline{ARST}$ can be used to synchronize PCLK to any desired event using additional external circuitry. Since PCLK is not used internally in the 82C201 for timing purposes, this will have no effect on the proper operation of the CPU. It does, however, effect the operation of OSC/12, which is normally used as the Counter/Timer clock.

Two reset output signals are provided on the 82C201 for resetting the system. RESET4 is a synchronized reset signal for general system reset. RESET3, which is similar to RESET4, is the CPU reset signal and, additionally provides

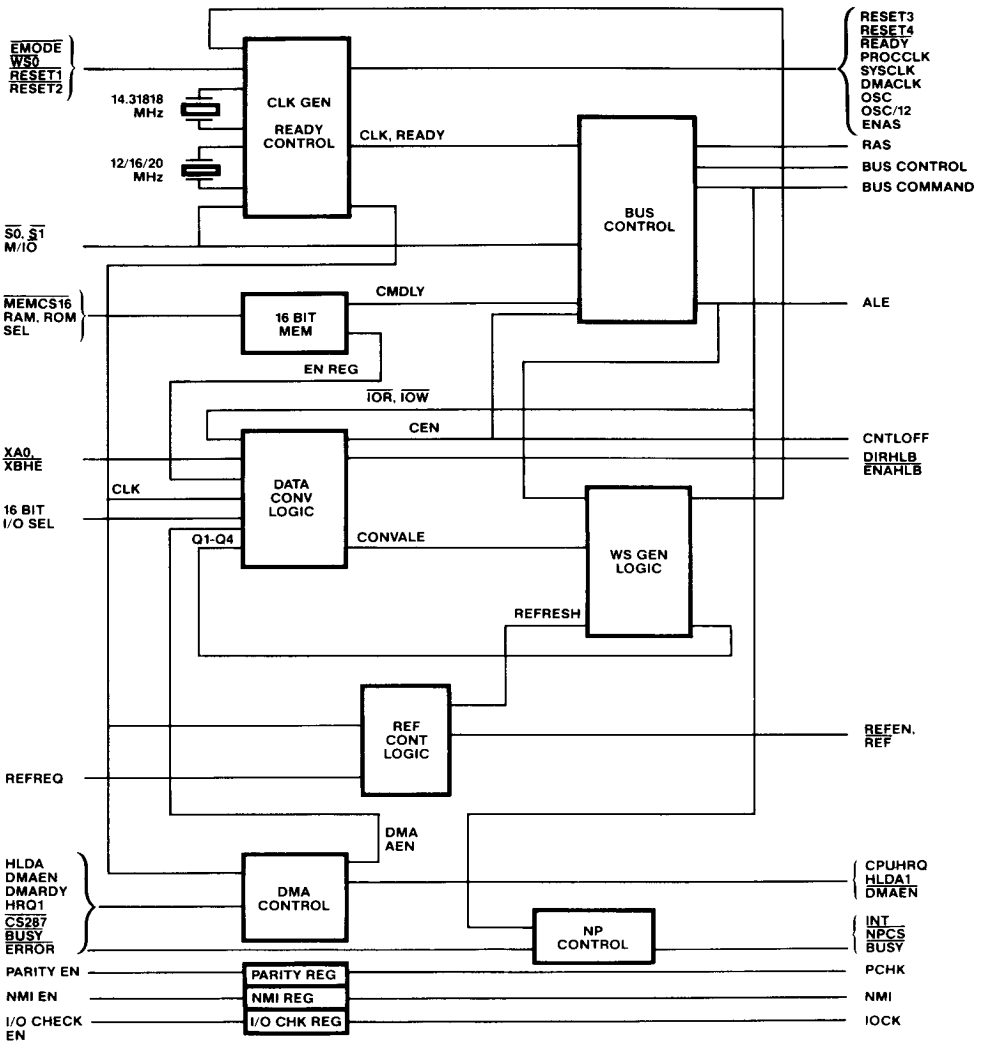


Figure 2. 82C201 Functional Block Diagram

a reset when a Shutdown condition in the CPU is detected. Both signals, RESET4 and RESET3, are active high signals derived from the RESET1 input. Both RESET4 and RESET3 meet the set-up and hold time requirements of the 80286. After a Shutdown condition is detected, RESET3 is asserted for 16 PROCCLK times and then deasserted. A RESET3 resulting from shutdown detection is also synchronous with PROCCLK, ensuring proper CPU operation.

A ready signal (READY) is provided on the 82C201 to allow the CPU to run with slower memories and peripherals. This signal is an open drain output requiring an external pull-up resistor to V_{CC}. The value of this resistor should not be less than 900 ohms nor greater than 1K ohms to ensure adequate rise and fall times. READY is synchronized in this section of the 82C201 to the PROCCLK output. Most of the control for READY, however, is provided for in other sections of the device. A detailed description of READY control can be found in the section entitled "Wait State and Conversion Logic." READY can also be asserted by applying a LOW to the WS0 input. In this case, WS0 must be externally synchronized for proper operation.

In order to prevent inadvertent writes to the Clock/Calendar device from occuring during power-up and power-down situations, ENAS (address strobe enable) is generated in the 82C201. ENAS is deasserted whenever RESET1 is active, and is only asserted after the CPU has started its first status cycle.

The RESET1 input is buffered internally in the 82C201 with a Schmitt trigger, and is intended to be used as the Power Normal input for the system. This signal should be LOW when power is applied to the system and remain LOW for at least 5 msec after all voltages have reached their proper operating range and the PROCCLK has reached the specified AC and DC parameters. The RESET1 input has a typical input hysteresis of 1 volt and may be directly connected to an RC network to generate the necessary power-on reset. (See Figure 9 for typical DC characteristics.)

Reset of the CPU can also be accomplished by asserting the RESET2 input. This input is controlled by the keyboard processor and can be used to reset the CPU by means of specific key combinations. When RESET2 is activated, the CPU reset signal (RESET3) is then asserted and will not be deasserted for 16 PROCCLK cycles after RESET2 is deasserted.

Command and Control Signal Generation

This section of the 82C201 generates various I/O and Memory control signals for an 80286 based system. The Command and Control Signal Generation Logic has two types of output signals. The first type, the Command signals, are decoded from the CPU status information available during the T_S cycle. These signals (MEMR, MEMW, IOR, IOW, INTA) indicate which type of cycle is to be performed. The second type (ALE, DT/R, DEN, DSDEN0, DSDEN1, RAS) are the Control signals. These signals latch the address, determine the direction and enabling of the data bus buffers and start a memory cycle. Both sets of signals are derived from the CPU status information (M/IO, S0 S1) and are controlled by an internal state machine. Table 1 contains a list of the command and control outputs for each type of bus cycle.

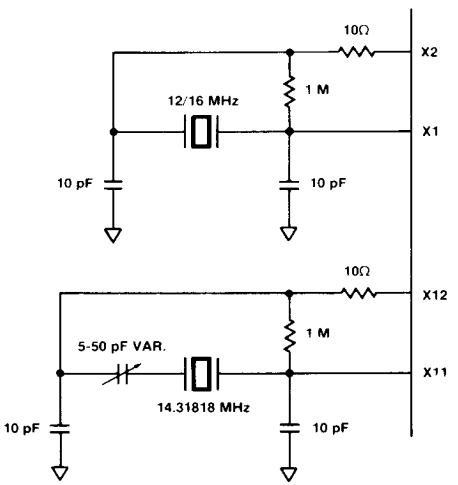


Figure 3. Recommended Oscillator Circuit

Table 1 Bus Cycle Status Definition

M/IO	S1	S0	Type of Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	None; idle
1	0	0	Halt or shutdown
1	0	1	Memory read
1	1	0	Memory write
1	1	1	None; idle

The state machine in the 82C201 has three bus states: Idle (T_I), Status (T_S), and Command (T_C). A T_I state exists when the CPU is not attempting a bus cycle. During this time, all command and control signals are in an inactive state. The start of a bus cycle is signaled by the S0 and S1 inputs. Whenever either signal is asserted, a bus cycle is started. The state machine then transitions into the T_S state. At this time, ALE becomes active and is returned to the inactive or LOW state at the end of T_S. Following a T_S state, the state machine then enters the T_C state. At this point, the decoded Command is issued unless an internal Command Delay condition exists. If a Command Delay is necessary, the appropriate command will be asserted one PROCCLK cycle later than normal. A Command Delay condition will exist on all I/O cycles (including INTA) and any memory cycle in which both AF16 and MEMCS16 are HIGH.

For Data Bus buffer control, four signals are provided. These signals are DT/R, DEN, DSDEN0, and DSDEN1. DT/R, is used to determine the data direction. The remaining three signals are Enables for the Data Bus Buffers. DEN is a general purpose timing signal for tri-state control of the transceivers. DSDEN0 is a similar signal to DEN, but has been further qualified with A0 to control the lower 8 bits of the Data Bus. Similarly, DSDEN1, has been qualified with BHE, and is used to control the upper 8 bits. In an IBM PC AT compatible design, independent control of the bus transceivers is necessary to accomplish the 8-bit to 16-bit data conversions.

In order to optimize system performance, the ALE and RAS signals have been enhanced. The additional input strapping signal EMODE has been incorporated into the 82C201. This signal will alter the timing of both ALE and RAS to provide either the standard signals or, if EMODE is LOW, the enhanced Early ALE and Early RAS signals. ALE is a control signal intended to be used to gate the address latches in the user's system. RAS is a timing signal used for controlling the start of a memory access. With EMODE asserted, ALE will become active asynchronously in response to the status signals S0 and S1 from the CPU. This allows the address latches to be enabled at the earliest possible moment. Early RAS also becomes active much earlier than the RAS signal generated in the IBM PC AT design. By utilizing the Early RAS signal, the Memory Cycle is lengthened. This allows the use of lower speed memories, while maintaining the same CPU clock rate.

Conversion Logic

This section of the 82C201 provides a means for the system to perform 16 bit data transfers to and from 8 bit peripheral devices. The Conversion Logic will detect when a conversion is necessary, signal the Wait State Control Logic to hold the CPU, and perform the conversion by manipulating the LSA0 and Cross-over Buffer Control output pins, DIRHLB and ENHLB. During a conversion, the CPU is held in a wait condition with READY inactive. Once the first byte has been transfered, the currently active control signal is interrupted while the state of LSA0 and the Cross-over Buffer Control signals are changed. Control is then re-enabled.

Conversion will take place when either of two conditions occurs:

A 16-bit transfer to an 8-bit memory device

A 16-bit transfer to an 8-bit I/O device

Wait State Control

The function of the Wait State Control logic is to match the speed of the various devices in the user's system to the speed of the CPU. Wait States are inserted in a CPU Bus Cycle by turning off the 82C201 open-drain READY output pin. This allows an external pull-up resistor to raise the 80286 input READY to a

HIGH (Not Ready) state. Termination of a CPU Bus Cycle will now occur only when the 82C201 READY is reasserted to a LOW. (See Figure 4 for a diagram of both an 8 bit I/O cycle and an 8/16 bit I/O cycle.)

In the design of the 82C201, several defaults have been established. During a memory cycle, which is signaled by the assertion of AF16 or MEMCS16, one wait state is inserted unless the user activates the WS0 input pin, in which case no wait states are inserted. The default for an 8-bit I/O cycle is four wait states. During an I/O cycle this can be shortened to either two or three wait states by the assertion of WS2 or WS3. Both WS2 and WS3 must be externally decoded by the user. If the user has 16 bit I/O devices in his system, the assertion of IOCS16 will result in the insertion of one wait state. On accesses to the I/O channel of the expansion bus, a maximum of four wait states will be inserted. This can be overridden by driving IOCHRDY LOW. Wait states will then continue to be inserted indefinitely. Note that IOCHRDY should not be held LOW for more than 2.5 usec.

DMA and Refresh Logic

Refresh in the IBM PC AT is handled by placing the CPU in a Hold condition, executing the refresh, and then releasing the processor from the Hold. Since this is the same method the DMA Controller uses to perform it's function, contention for the CPU Hold cycle must be resolved. In order to prevent contention problems, REFREQ is clocked into the Arbiter on the falling edge of DMACLK and HRQ1 is clocked in on the rising edge. Arbitration is then performed each SYSCLK cycle. This method of arbitration provides equal weighting of the two signals so neither has priority over the other.

The REFREQ input to the 82C201 is positive edge triggered, and if the minimum high and low times are met, the request will be internally latched. This allows the user to generate a refresh request from the relatively short duration Carry signal generated by a counter. Once REFREQ has been pulsed, the internal logic of the 82C201 will take over. Arbitration for the CPUHRQ output takes place and a Hold signal is generated. Upon completion of the current bus cycle, the CPU will enter a Hold state and issue HLDA. When the CPU asserts HLDA, the Command Signals (MEMR, MEMW, IOR, IOW, INTA) from the 82C201 will tri-state. (In order to maintain the command signals in an inactive state, external pull-up resistors to V_{CC} are required.) The open drain output REF is asserted and REFDET will make a state transition (low to high or high to low). After the next rising edge of SYSCLK, REFEN is asserted. REFEN is an output signal intended to enable the refresh counter outputs to the RAM during a refresh cycle. One SYSCLK cycle after REFEN is asserted, both MEMR and RAS are asserted. MEMR and RAS will remain active for two SYSCLK cycles, and then be deasserted. At this time CPUHRQ is also released. If the CPU has not regained control of the system, MEMR will return to the tri-state condition after the next SYSCLK cycle.

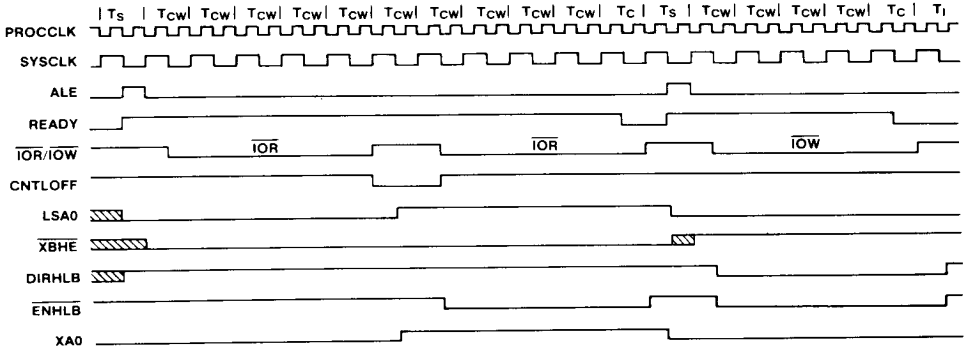


Figure 4. I/O Cycle Sequence

A DMA cycle is handled by the 82C201 in much the same manner as a REFREQ. (See diagram in Figure 5). When HRQ1 is asserted, an internal arbitration takes place and CPUHRQ is asserted. Once the CPU has suspended operation and asserted HLDA, the 82C201 will generate a HLDA1 signal and tri-state the Command outputs, allowing the DMA Device control of the system. The DMA Controller can then begin a bus cycle. In some cases the system will require a wait state to be inserted in a DMA cycle. This can be accomplished by providing a LOW to HIGH transition on the DRC input pin of the 82C201 early in the cycle. (This is most easily done by ORing $\overline{\text{MEMR}}$ and $\overline{\text{IOR}}$ from the DMA Controller.) The DMA Cycle will then be extended by one DMACLK period. Once initiated, the DMA cycle can be extended by an I/O device signaling a not ready condition. This is accomplished by applying a LOW to the IOCHRDY input of the 82C201. The DMA Controller will then be held in a wait state until IOCHRDY is returned HIGH.

In order to guarantee the integrity of an INTA cycle, which requires two bus cycles to complete, an inhibit function has been included in the 82C201. Once an INTA cycle has started, CPUHRQ is inhibited and will not be re-enabled until the CPU performs a memory write cycle. The memory write cycle will normally be executed due to the Stack operations required to handle the interrupt, and will be transparent to the software. This inhibit will then ensure that no DMA device can accidently corrupt an INTA cycle.

Numerical Processor Control

Incorporated in the 82C201 is the circuitry to interface an 80287 Numerical Processor to the 80286. This circuitry handles the decoding required for selecting and resetting the Numerical Processor, handling $\overline{\text{BUSY}}$/$\overline{\text{ERROR}}$ signals from the 80287 to the CPU, and generating interrupt signals for error handling.

The input signal $\overline{\text{CS287}}$ is used as a select by the internal logic of the 82C201 for the Numerical Processor chip select ($\overline{\text{NPCS}}$) and for generating a reset signal (RES287) to the 80287. The CS287 input should be a user-generated I/O decode, which is active for I/O addresses 0F0h through 0FFh. Further internal decode is provided by the 82C201 to generate RES287, $\overline{\text{NPCS}}$, and clear the latched BUSY287 signal, which results from an error condition. Refer to Table 2 for a definition of the internal decode addresses.

Table 2

Hex Address	Description
070	NMI Mask
0F0	Clear Numerical Processor Busy
0F1	Reset Numerical Processor Busy
0F8-0FF	Numerical Processor Chip Select

When the 80287 is given the command to perform a task, it will issue a $\overline{\text{BUSY}}$ signal to the 82C201. This signal will be passed to the CPU by assertion of the $\overline{\text{BUSY287}}$ output. In normal operation the $\overline{\text{BUSY}}$ input is passed through to

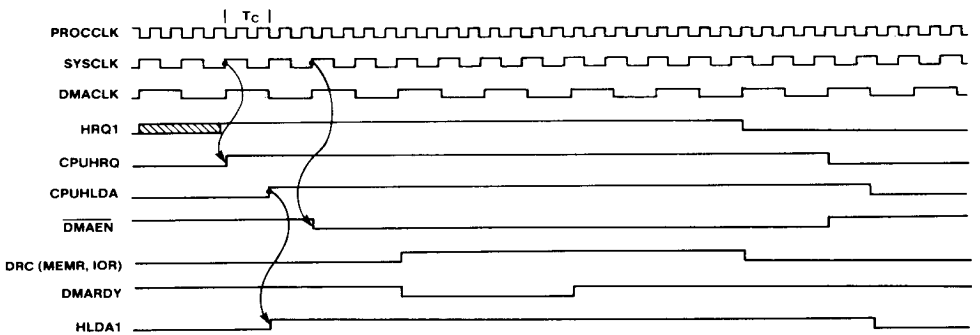


Figure 5. DMA Cycle Sequence

the BUSY287 output and is deasserted as a result of BUSY being deasserted. If, during this busy period, the ERROR input becomes active (signaling a Numerical Processor error), the BUSY287 output is then latched and the CPINT output pin is forced to a HIGH. Both signals will then remain active until cleared by an I/O write cycle to address 0F0h or 0F1h. After a system reset, both the interrupt latch for CPINT and the busy latch for BUSY287 are cleared.

Resetting the 80287 is handled by the RES287 output pin from the 82C201 and can be activated by a system reset or an I/O write to address 0F1h. This signal is not latched internally and will only be active for the period of time that the source signal is active.

NMI and Error Logic

This section of the 82C201 performs the latching and enabling of I/O and parity error conditions which, if NMI is enabled, will generate a Non-maskable Interrupt to the CPU. Both enable inputs ERMPCK and ENIOC are active HIGH level enables to their respective latches. Once latches have been enabled, an error condition can be detected and latched internally by placing a LOW on either of the error input pins—IOC or PAR. If either IOC or PAR indicate an error condition, that input latch is set and the appropriate output status pin becomes active. The status outputs, IOCK and PCHK, may then be used to determine the source of the error. An error condition will only result in the generation of an interrupt if NMI has been enabled by the user. Enabling and disabling of the NMI interrupt is accomplished by externally generating an active LOW decode, which is applied to the NMICS input of the 82C201. The trailing edge of NMICS is used to latch the state of input XD7, which will determine whether NMI is enabled or disabled. If XD7 is HIGH when NMICS makes a LOW to HIGH transition, NMI will be enabled.

82C201 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C201 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C201 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=8mA (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH} (Note 1)	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 8 MHz Clock	I_{CC}		20	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA
PROCCLK Output Low Voltage @ I_{OL} = 5 mA	V_{OLC}		0.45	V
PROCCLK Output High Voltage @ I_{OH} = -1 mA	V_{OHC}	4.0		V

NOTE 1: Pins 44, 83 only. Pins 3, 5, 8, 38, 45-50, 55, 61, 62, 65, 78, 79 and 81 have I_{OL} = 4mA. All other outputs and I/O pins have I_{OL} = 2mA. In all cases I_{OL} = I_{OH} = for the pin.

82C201, 82C201-10 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

		82C201		82C201-10		
Sym	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t1	PROCCLK period (Note 2)	62	250	50	250	ns
t2	PROCCLK low time	15	225	11	225	ns
t3	PROCCLK high time	25	235	18	235	ns
t4	M/$\overline{IO}$, $\overline{S0}$, $\overline{S1}$ hold time (PROCCLK Load = 50pf)	1		1		ns
t5	M/$\overline{IO}$, $\overline{S0}$, $\overline{S1}$ set-up time	24		20		ns
t6	ALE active delay ($\overline{EMODE}$ = 1) (Note 1)	3	21	3	16	ns
t7	ALE inactive delay (Note 1)	4	26	4	19	ns
t8	ALE delay from Status ($\overline{EMODE}$ = 0) (Note 1)	5	31	5	24	ns
t9	RAS active delay ($\overline{EMODE}$ = 1) (Note 1)	9	40	0	40	ns
t10	RAS inactive delay ($\overline{EMODE}$ = 1) (Note 1)	10	40	10	40	ns
t11	RAS active delay ($\overline{EMODE}$ = 0) (Note 1)	5	38	3	25	ns
t12	RAS inactive delay ($\overline{EMODE}$ = 0) (Note 1)	9	37	5	25	ns
t13	$\overline{WS0}$ set-up time (PROCCLK Load = 50pf)	22		15		ns
t14	$\overline{WS0}$ hold time (PROCCLK Load = 50pf)	1		0		ns
t15	Command active delay (Note 1)	4	26	3	21	ns
t16	Command inactive delay (Note 1)	7	25	3	20	ns
t17	DT/$\overline{R}$ active delay (Note 1)	7	35	7	23	ns
t18	DT/$\overline{R}$ inactive delay (Note 1)	1	9	1	9	ns
t19	DEN active delay from DT/$\overline{R}$ low (Read) (Note 1)	1	7	0	7	ns
t20	DEN inactive delay (Note 1)		42		35	ns
t21	$\overline{DSDEN0}$, $\overline{DSDEN1}$ active delay from DEN active (Note 1)	2	10	2	10	ns
t22	$\overline{DSDEN0}$, $\overline{DSDEN1}$ inactive from DEN inactive (Note 1)	-2	-6	-2	-6	ns
t23	XA0, $\overline{XBHE}$ set-up from DEN active	9		5		ns
t24	XA0, $\overline{XBHE}$ set-up from DEN inactive	0		0		ns
t25	DEN active delay (Write) (Note 1)	8	33	8	23	ns

82C201, 82C201-10 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)
(Continued)

		82C201		82C201-10		
Sym	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t26	DEN inactive delay (Write) (Note 1)		41		30	ns
t27	$\overline{AF16}$, $\overline{MEMCS16}$ set-up time	37		20		ns
t28	$\overline{AF16}$, $\overline{MEMCS16}$ hold time	1		0		ns
t29	$\overline{RESET1}$ hold time (PROCCLK Load = 50pf)	10		10		ns
t30	$\overline{RESET1}$ set-up time (PROCCLK Load = 50pf)	28		28		ns
t31	RESET4 delay (Note 1)		37		37	ns
t32	$\overline{ENAS}$ delay (Note 1)		36		36	ns
t33	SYSCLK delay (Note 1)		26		26	ns
t34	DMACLK delay from SYSCLK (Note 1)		16		16	ns
t35	RESET3 delay (Note 1)	5	50	5	27	ns
t36	RESET3 delay (Shut-down detected) (Note 1)	5	21	5	21	ns
t37	PCLK delay (Note 1)		22		22	ns
t38	OSC/12 delay from OSC (Note 1)		14		14	ns
t39	$\overline{DSDEN0}$, $\overline{DSDEN1}$ active delay from DT/$\overline{R}$ (Note 1)	3		3		ns
t40	DT/$\overline{R}$ inactive delay from $\overline{DSDEN0}$, $\overline{DSDEN1}$ (Note 1)	3		3		ns
t41	CPUHRQ active delay (due to REFREQ) from DMACLK (DMACLK Load = 50pf)		25		25	ns
t42	CPUHRQ inactive delay from SYSCLK		25		25	ns
t43	$\overline{REF}$ active delay from HLDA (Note 3)		25		25	ns
t44	$\overline{REF}$ inactive delay from SYSCLK (Note 3)		25		25	ns
t45	HLDA1, $\overline{REF}$ active delay from SYSCLK		25		25	ns
t46	REFDET delay from $\overline{REF}$		10		10	ns
t47	$\overline{REFEN}$ active delay from SYSCLK		25		25	ns
t48	$\overline{REFEN}$ inactive delay from SYSCLK		18		18	ns
t49	$\overline{MEMR}$ tri-state delay from HLDA		30		30	ns
t50	$\overline{MEMR}$ tri-state delay from SYSCLK		22		22	ns
t51	$\overline{MEMR}$ (Refresh) active delay from SYSCLK		21		21	ns

82C201, 82C201-10 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)
(Continued)

		82C201		82C201-10		
Sym	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t52	$\overline{\text{MEMR}}$ (Refresh) inactive delay from SYSCLK		21		21	ns
t53	REFREQ set-up to DMACLK	24		24		ns
t54	REFREQ width	25		25		ns
t55	IOCHRDY Set-up to PROCCLK	26		26		ns
t60	HRQ1 set-up to DMACLK (DMACLK load =50pf)	15		15		ns
t61	HLDA1 active, inactive delay from HLDA		30		30	ns
t62	HLDA1 inactive delay from SYSCLK		32		32	ns
t63	AEN1, AEN2 set-up from DRC	26		26		ns
t64	DRC set-up time from DMACLK	26		26		ns
t65	DMARDY delay from DRC		35		35	ns
t66	DMARDY delay from DMACLK		30		30	ns
t67	HRQ1 hold time from DMACLK	1		1		ns
t68	DRC hold time from DMACLK	1		1		ns
t69	AEN1, AEN2 hold time from DMARDY	1		1		ns
t70	$\overline{\text{READY}}$ inactive delay (Note 3)		15		15	ns
t71	$\overline{\text{READY}}$ active delay (Note 3)		20		20	ns
t72	A0 set-up time from PROCCLK	0		0		ns
t73	A0 hold time from PROCCLK	5		5		ns
t74	LSA0 delay		52		35	ns
t75	Q1WS delay		20		20	ns
t76	WS2, WS3 set-up time	43		43		ns
t77	WS2, WS3 hold time	0		0		ns
t78	CTLOFF active delay		36		36	ns
t79	CTLOFF inactive delay		41		41	ns
t80	$\overline{\text{ENAHLB}}$, DIRHLB inactive delay from $\overline{\text{IOR}}$, $\overline{\text{IOW}}$		30		30	ns
t81	DIRHLB delay from PPROCLK (high byte $\overline{\text{IOW}}$)		25		25	ns
t82	XA0, $\overline{\text{XBHE}}$ set-up from ALE trailing edge	0		0		ns
t83	$\overline{\text{IOCS16}}$ inactive set-up to $\overline{\text{IOR}}$/$\overline{\text{IOW}}$ active	5		5		ns

82C201, 82C201-10 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)
(Continued)

		82C201		82C201-10		
Sym	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t84	$\overline{IOCS16}$ hold time from $\overline{IOR}$/$\overline{IOW}$ inactive	2		2		ns
t85	XD7 set-up time with respect to NMICS	10		10		ns
t86	XD7 hold time with respect to NMICS	1		1		ns
t87	$\overline{NPCS}$ active delay from XA3, $\overline{INTA}$, $\overline{CS287}$		36		36	ns
t88	$\overline{NPCS}$ inactive delay from XA3, $\overline{INTA}$, $\overline{CS287}$		29		29	ns
t89	CPINT delay from $\overline{BUSY}$, $\overline{ERROR}$ low (Note 4)		30		30	ns
t90	CPINT inactive delay from $\overline{ERROR}$ high (Note 5)		31		31	ns
t91	Overlap of $\overline{BUSY}$ and $\overline{ERROR}$ (both low)	10		10		ns
t92	$\overline{BUSY287}$ active delay from $\overline{BUSY}$		32		32	ns
t93	$\overline{BUSY287}$ inactive delay from $\overline{BUSY}$		32		32	ns
t94	$\overline{IOCS16}$ active setup to PROCCLK		26		26	ns
t95	$\overline{ERROR}$ hold-time with respect to $\overline{BUSY}$	0		0		ns
t96	$\overline{BUSY}$ active pulse width	15		15		ns
t97	$\overline{ERROR}$ setup with respect to $\overline{BUSY}$	5		5		ns
t98	$\overline{ERROR}$ min low pulse width	10		10		ns
t99	$\overline{BUSY287}$ delay from $\overline{IOW}$		30		30	ns
t100	XA0, XA3, $\overline{CS287}$ set-up time with respect to $\overline{IOW}$	10		10		ns
t101	XA0, XA3, $\overline{CS287}$ hold-time with respect to $\overline{IOW}$	1		1		ns
t102	RES287 active delay from $\overline{IOW}$		33		33	ns
t103	RES287 inactive delay from $\overline{IOW}$		37		37	ns
t104	CPUHRQ inactive delay from $\overline{INTA}$		25		25	ns

82C201, 82C201-10 AC Characteristics

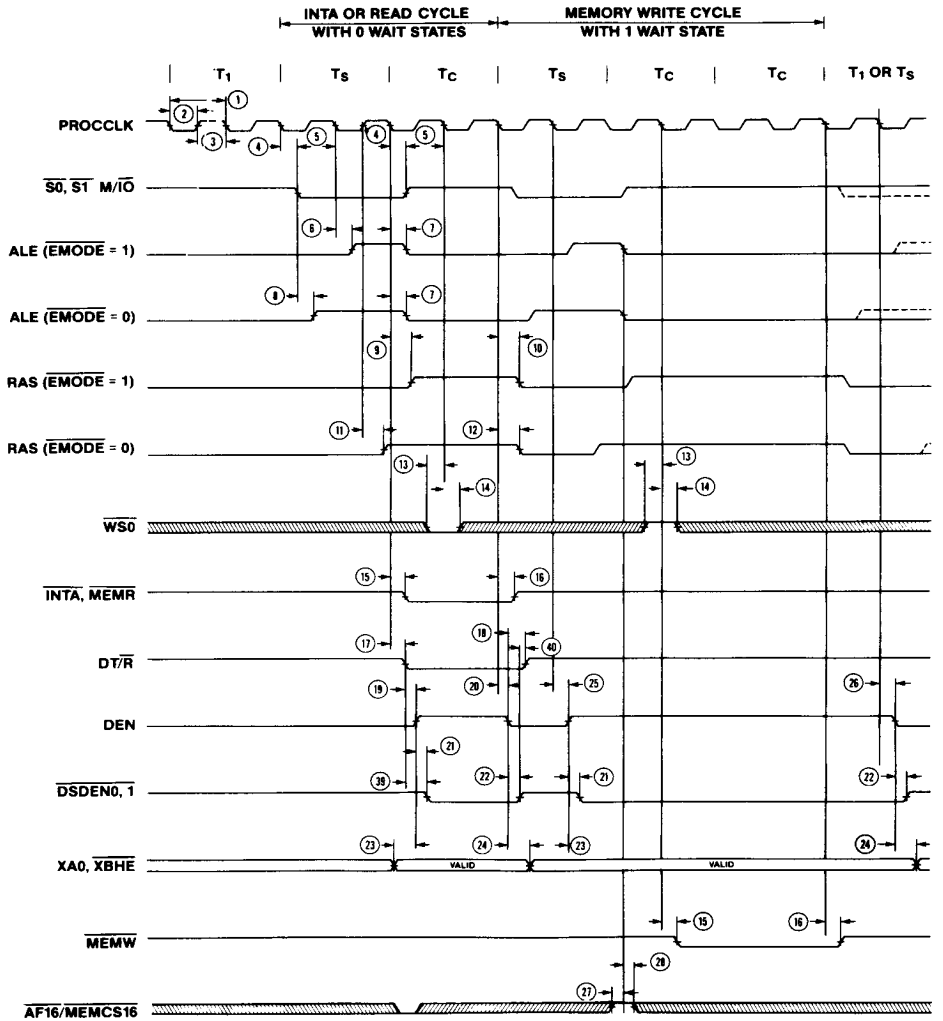
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)
(Continued)

		82C201		82C201-10		
Sym	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t105	CPUHRQ active delay from $\overline{IOW}$		25		25	ns
t106	$\overline{PAR}$, $\overline{IOC}$ low pulse width	10		10		ns
t107	IOCK, PCK NMI delay		30		30	ns
t108	IOCK, PCK, NMI delay from ENIOC, ENPCHK low		30		30	ns
t109	ENIOC, ENPCHK min low width	10		10		ns

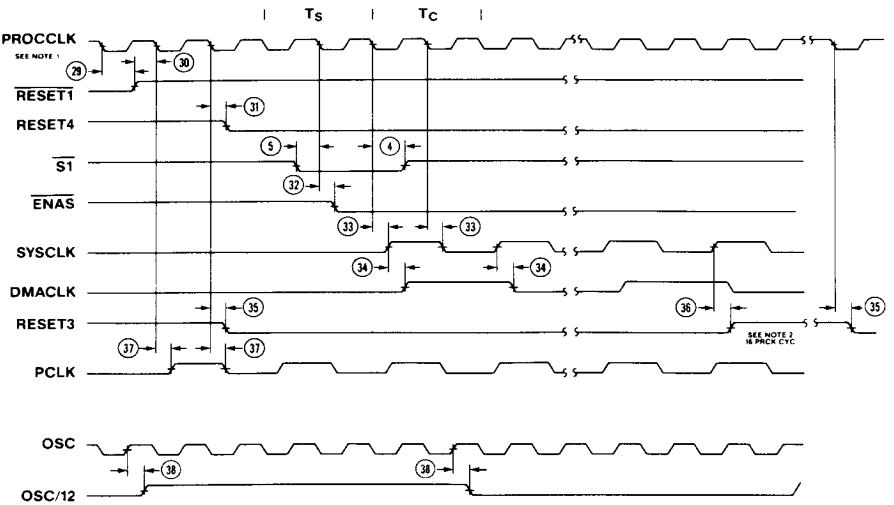
NOTES:

1. Pin capacitive load = 50pf; TTL levels
2. Measured from V_{ol} = 0.6V V_{oh} = 3.6V
3. $\overline{READY}$ and $\overline{REF}$ are open drain outputs; times specified are from high impedance to active and active to high impedance. Actual times will depend on value of external resistor used.
4. $\overline{BUSY}$ and $\overline{ERROR}$ have to be both low for CPINT active transition.
5. Load capacitance = 85 pf on *all outputs* except stated otherwise.

82C201 TIMING DIAGRAMS



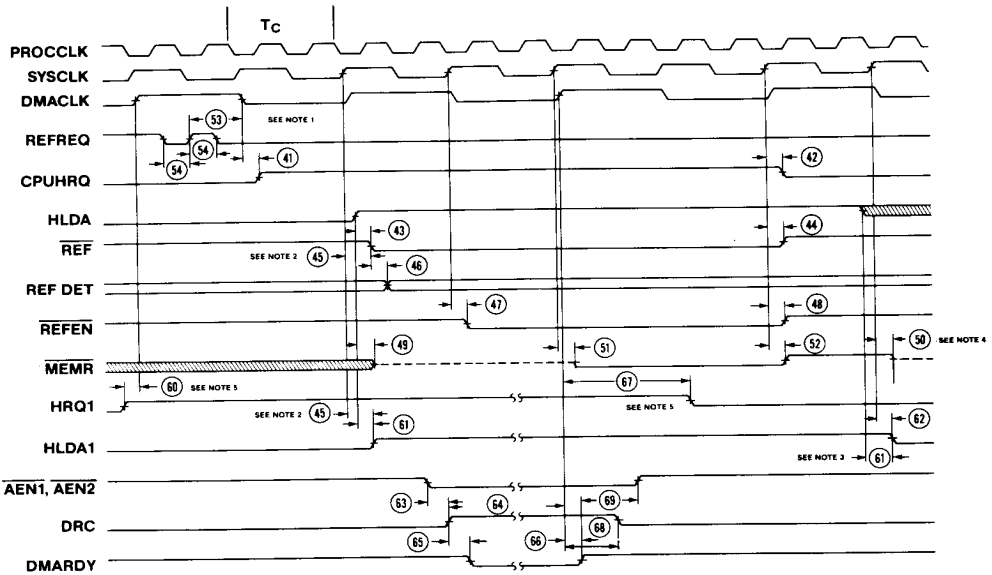
82C201 TIMING DIAGRAMS



NOTE

1. RESET is an asynchronous input and the timings shown are only to guarantee signal recognition on that clock cycle instead of the next one.
2. RESET3 is shown going high due to an internally detected shut down condition and will return low 16 PRCK cycles later.

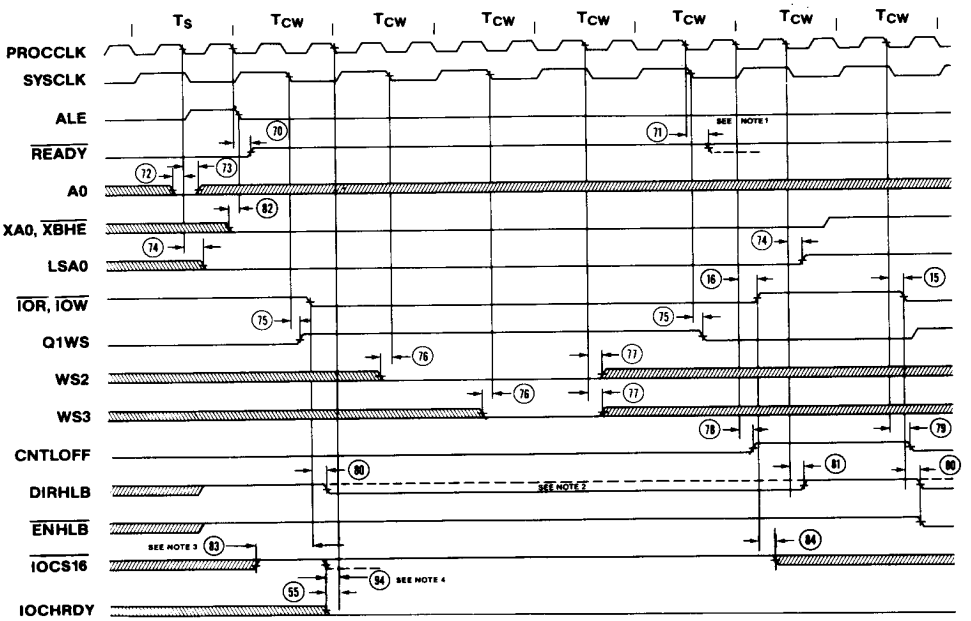
82C201 TIMING DIAGRAMS



NOTE

1. REFREQ is an asynchronous input and the timing from the high going edge of REFREQ to the low going edge of DMACLK is only to guarantee starting a refresh cycle on that clock cycle instead of the next one.
2. This timing parameter is shown because REF & HLDA1 are inhibited until this time. After this point CPU HLDA will enable REF or HLDA1.
3. HLDA1 will be deasserted at this time by SYSCLK if HLDA is still active.
4. MEMR will tri-state at this time if HLDA is still active.
5. Set-up and hold times are shown only to guarantee signal recognition on this clock edge.

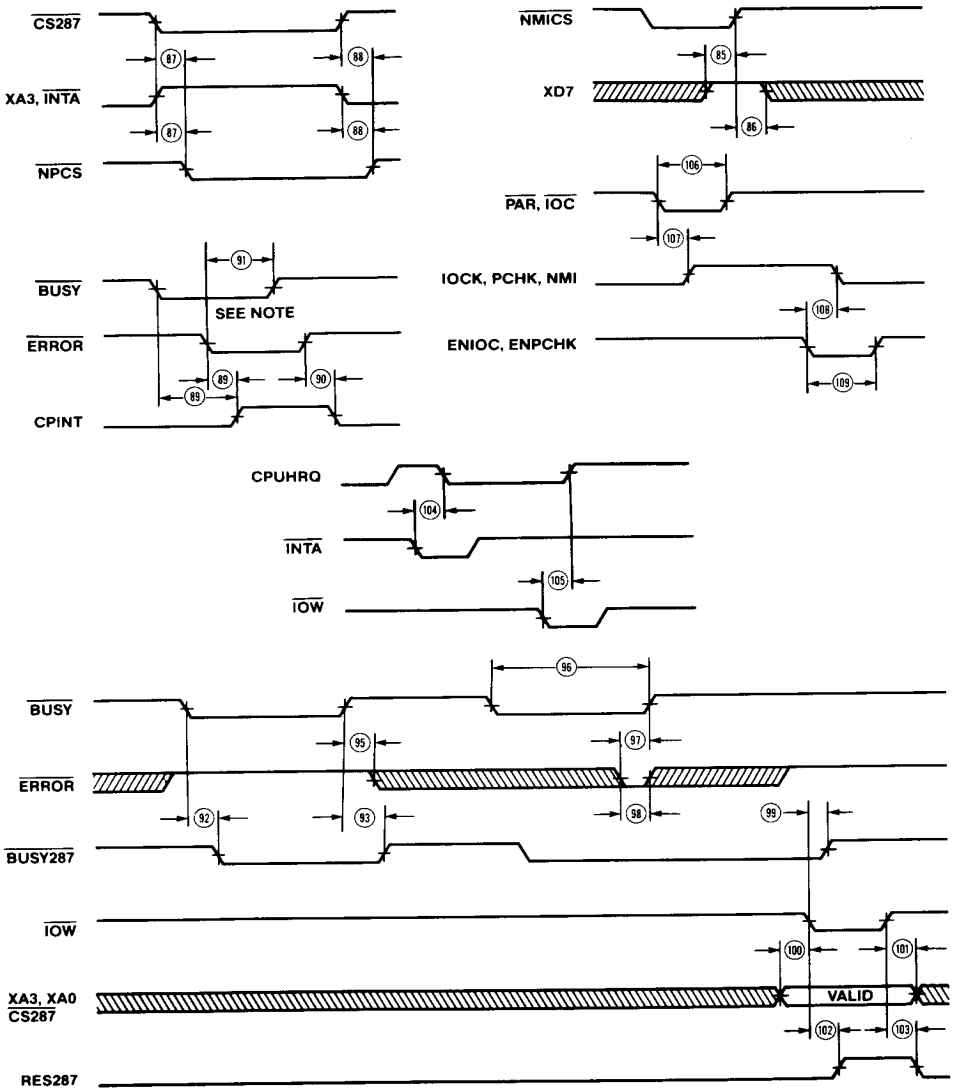
82C201 TIMING DIAGRAMS



NOTE

1. READY asserted here on 8-bit transfer to 8-bit peripheral.
2. DIRHLB shown for I/O write cycle: dotted line for I/O read cycle.
3. IOCS16 inactive setup to IOR/IOW is to prevent one wait state operation.
4. IOCS16 active setup to PROCCLK is to ensure that no conversion will take place.

82C201 TIMING DIAGRAMS



NOTE:
$\overline{\text{BUSY}}$ and $\overline{\text{ERROR}}$ both have to be low for CPINT to be active.

Functional Description 82C202

The 82C202 consists of the following functional blocks:

- ROM/RAM Decode and Latch
- Parity Error Detection Logic
- I/O Decode Logic

ROM/RAM Decode and Latch

The 82C202 contains the circuitry to decode the CPU's Address bus and provide the necessary latched signals for controlling both ROMS and RAMS on the user's system board. In order to make the 82C202 more flexible, a user-configurable decode is incorporated into the device. Decode configuration is accomplished by strapping the SEL0 and SEL1 input pins. Table 3 shows the different strapping options available. Strapping allows the user to configure the system for either 64K RAMs, 256K RAMs, or both 64K and 256K devices. Memory configurations ranging from 128K bytes to 1M bytes are now possible using the decode selects.

Additional support for Memory Refresh is also provided in the 82C202. During a Refresh Cycle, the assertion of the REF input will cause the 82C202 to ignore the current Address inputs. Instead, it will activate both the RAS0 and RAS1 outputs while inhibiting CAS0, CAS1, and $\overline{\text{LCSROM}}$.

$\overline{\text{LCSROM}}$ is the decoded and latched ROM chip select from the 82C202. This output is asserted whenever either of two addresses ranges is detected and $\overline{\text{REF}}$ is inactive. The address ranges for $\overline{\text{LCSROM}}$ are also listed in Table 3.

The two outputs, $\overline{\text{LMEGCS}}$ and $\overline{\text{MDBEN}}$, are intended to be used as memory buffer enable signals. $\overline{\text{LMEGCS}}$ is active whenever any memory access is made to an address below 100000h or when $\overline{\text{REF}}$ is active. For memory data bus buffer control, the signal $\overline{\text{MDBEN}}$ should be used. This signal will become active whenever either CAS0, CAS1, or $\overline{\text{LCSROM}}$ is active. The $\overline{\text{MDBEN}}$ signal may also be externally ANDed with $\overline{\text{MEMR}}$ to create the necessary directional control signal for the memory data buffer.

The 82C202 internal latch is controlled by two input signals —HLDA and ALE. During a CPU Memory Cycle, ALE will enable the RAM Decode Latch and allow the output from the decoder to be transferred to the output pins. When ALE is deasserted, the decoder output is latched for the remainder of the cycle. HLDA also enables the RAM Decode Latches. Asserting HLDA will enable the decoder outputs to the output pins and force $\overline{\text{LCSROM}}$ inactive. Forcing $\overline{\text{LCSROM}}$ inactive occurs regardless of the state of the input addresses.

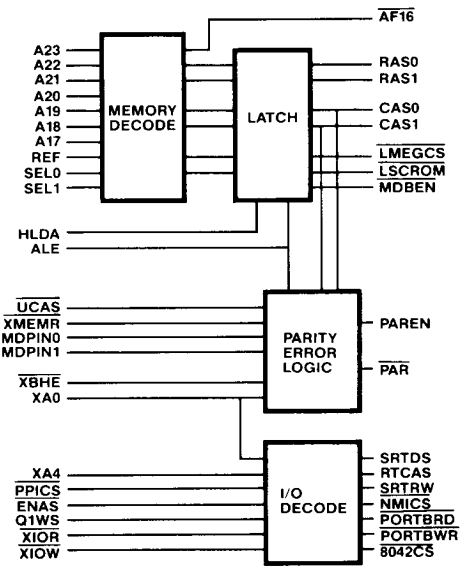


Figure 6. 82C202 Functional Block Diagram

Table 3

Select Input		RAM Address Range		RAM Type		ROM Address Range	
SEL0	SEL1	RAS0/CAS0	RAS1/CAS1	BANK0	BANK1	Low Addr. Range	High Addr. Range
0	0	000000h-01FFFFh	020000h-03FFFFh	64K	64K	0E0000h-0FFFFFh	FE0000h-FFFFFFh
1	0	000000h-07FFFFh		256K	NONE	0E0000h-0FFFFFh	FE0000h-FFFFFFh
0	1	000000h-07FFFFh	080000h-09FFFFh	256K	64K	0E0000h-0FFFFFh	FE0000h-FFFFFFh
1	1	000000h-07FFFFh	100000h-17FFFFh	256K	256K	0E0000h-0FFFFFh	FE0000h-FFFFFFh

The 82C202 has only one Decoder output that is unlatched. This output, AF16, is intended to be used by external circuitry as an indication that a 16-bit memory transfer is taking place. This signal may be used, if required, to generate wait states.

Parity Error Detection Logic

During a memory read cycle, this section of the 82C202 will detect a parity error condition and generate the error signal PAR. For proper operation of the circuitry, the input signals, MDPIN0 and MDPIN1, from the Parity Generator/Checker must correspond to the correct byte of data. MDPIN0 is derived from the low byte of data (D0-D7), and MDPIN1 from the high byte (D8-D15).

A parity error condition for the 82C202 can exist for either of two cases. Both cases occur during a decoded memory cycle, on the rising edge of XMEMR. The two cases are:

MDPIN0—HIGH and XA0—LOW
MDPIN1—HIGH and XBHE—LOW

If either of these conditions exist during the rising edge of XMEMR, the error signal PAR is asserted.

In order to provide for memory expansion beyond what is decoded in the 82C202, a separate input (UCAS) is provided to enable the Parity Error Detection Logic. UCAS will cause the PAREN output to become active. If an error condition is detected on the rising edge of XMEMR, PAR will be asserted. A similar sequence occurs during memory reads in which a decode is generated by the 82C202, but in this case, UCAS need not be asserted.

I/O Decode Logic

The I/O Decode Logic portion of the 82C202 provides the signals necessary for controlling the Clock/Calendar, Status/Control Port, NMI Enable Latch and the Keyboard Controller.

NMICS controls the enabling and disabling of the NMI Enable Latch, and 8042CS selects the Keyboard Controller. IBM PC AT compatibility is maintained for all of the decoded control signals in this section. A decoded listing of the outputs is provided in Table 4.

Three signals are generated in the 82C202 for controlling the Clock/Calendar device. These signals are used for latching the address (SRTAS), latching the data (SRTDS), and determining the direction of a data transfer (SRTRW). Gating of the SRTAS decode with Q1WS and ENAS (which originate from the 82C201) is performed to ensure proper latching of the register address by the Clock/Calendar device. Reading from and writing to the Clock/Calendar can be performed using these three signals.

PORTBRD and PORTBWR are provided in the 82C202 either to latch the contents of the data bus into a latch, in the case of PORTBWR, or to enable status information onto the data bus using PORTBRD.

Table 4

Inputs					Outputs						
PPICS	XA0	XA4	XIOR	XIOW	NMICS	PORTBRD	PORTBWR	8042CS	SRTDS	SRTAS (See Note)	SRTRW
1	X	X	X	X	1	1	1	1	1	0	1
0	0	0	X	X	1	1	1	0	1	0	1
0	1	0	0	1	1	0	1	1	1	0	1
0	1	0	1	0	1	1	0	1	1	0	1
0	0	1	1	0	0	1	1	1	1	1	1
0	1	1	1	0	1	1	1	1	1	0	0
0	1	1	0	1	1	1	1	1	0	0	1

X = Don't Care 0 = TTL Low 1 = TTL High
Note: This condition assumes Q1WS and ENAS are true.

82C202 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C202 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C202 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL} (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH} (Note 1)	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 8 MHz Clock	I_{CC}		20	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA

NOTE 1: See Page 43 for details.

82C202 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Max.	Units
t1	Address, Ramsel & REF setup to ALE going inactive	25		ns
t2	Address & Ramsel hold time from ALE inactive	0		ns
t3	REF hold time from ALE inactive	0		ns
t4	REF hold time from HLDA inactive	0		ns
t5	RAS valid from Address, Ramsel & REF valid		35	ns
t6	Address setup to ALE going active for ALE to control RAS	25		ns
t7	RAS delay from ALE active		20	ns
t8	CAS valid from Address, Ramsel & REF valid		35	ns
t9	Address setup to ALE going active for ALE to control CAS	25		ns
t10	CAS delay from ALE active		30	ns
t11	RAS active delay from HLDA active during REF cycle		30	ns
t12	CAS inactive delay from HLDA active during REF cycle		30	ns
t13	$\overline{AF16}$ valid from Address valid		35	ns
t14	$\overline{LCSROM}$ valid from Address & REF valid		40	ns
t15	Address setup to ALE going active for ALE to control $\overline{LCSROM}$	25		ns
t16	$\overline{LCSROM}$ delay from ALE active		35	ns
t17	$\overline{MDBEN}$ valid from ALE inactive		30	ns
t18	$\overline{MDBEN}$ hold time from ALE going active	5		ns
t19	$\overline{LCSROM}$ inactive from HLDA active		30	ns
t20	$\overline{LCSROM}$ active from HLDA inactive		30	ns
t21	$\overline{PAR}$ inactive from ALE active		25	ns
t22	$\overline{PAR}$ active from $\overline{XMEMR}$ inactive		15	ns
t23	REF setup to HLDA going active	15		ns
t24	MDPIN0, MDPIN1, $\overline{XBHE}$ & XA0 hold time from $\overline{XMEMR}$ inactive	0		ns
t25	MDPIN0, MDPIN1, $\overline{XBHE}$ & XA0 setup time to $\overline{XMEMR}$ going inactive	10		ns
t26	$\overline{LMEGCS}$ valid from Address & REF valid		40	ns
t27	Address setup to ALE going active for ALE to control $\overline{LMEGCS}$	25		ns
t28	$\overline{LMEGCS}$ valid from ALE active		30	ns
t29	$\overline{LMEGCS}$ active from HLDA active during REF cycle		30	ns

82C202 AC Characteristics

(T_A = 0° C to 70° C, V_{CC} = 5V ± 5%)
(Continued)

Sym	Description	Min.	Max.	Units
t30	PAREN valid from ALE inactive		20	ns
t31	PAREN inactive from ALE active	5	20	ns
t32	PAREN active from $\overline{UCAS}$ active		25	ns
t33	PAREN inactive from $\overline{UCAS}$ inactive	5	25	ns
t34	$\overline{PORTBRD}$, $\overline{PORTBWR}$, SRTDS or SRTDW active (low) from XA0 and XA4 valid		35	ns
t35	$\overline{PORTBRD}$, $\overline{PORTBWR}$, SRTDS or SRTDW inactive (high) from XA0 and XA4 invalid	5		ns
t36	$\overline{PORTBRD}$, $\overline{PORTBWR}$, SRTDS or SRTDW active (low) from $\overline{XIOR}$ or $\overline{XIOW}$ active		35	ns
t37	$\overline{PORTBRD}$, $\overline{PORTBWR}$, SRTDS or SRTDW inactive (high) from $\overline{XIOR}$ or $\overline{XIOW}$ inactive	5		ns
t38	$\overline{PORTBRD}$, $\overline{PORTBWR}$, SRTDS or SRTRW active from $\overline{PPICS}$ active		35	ns
t39	$\overline{PORTBRD}$, $\overline{PORTBWR}$, SRTDS or SRTRW inactive from $\overline{PPICS}$ inactive		5	ns
t40	$\overline{8042CS}$ active from $\overline{PPICS}$ active		35	ns
t41	$\overline{8042CS}$ inactive from $\overline{PPICS}$ inactive	5		ns
t42	$\overline{8042CS}$ active from XA0 & XA4 valid		35	ns
t43	$\overline{8042CS}$ inactive from XA0 & XA4 invalid	5		ns
t44	SRTAS active from XA0 & XA4 valid		35	ns
t45	SRTAS inactive from XA0 & XA4 invalid	5	35	ns
t46	SRTAS active from $\overline{ENAS}$ active		35	ns
t47	SRTAS inactive from $\overline{ENAS}$ inactive	5	35	ns
t48	SRTAS active from Q1WS active		35	ns
t49	SRTAS inactive from Q1WS inactive	5	35	ns
t50	SRTAS active from $\overline{XIOW}$ active		35	ns
t51	SRTAS inactive from $\overline{XIOW}$ inactive	5	35	ns

Output test conditions:

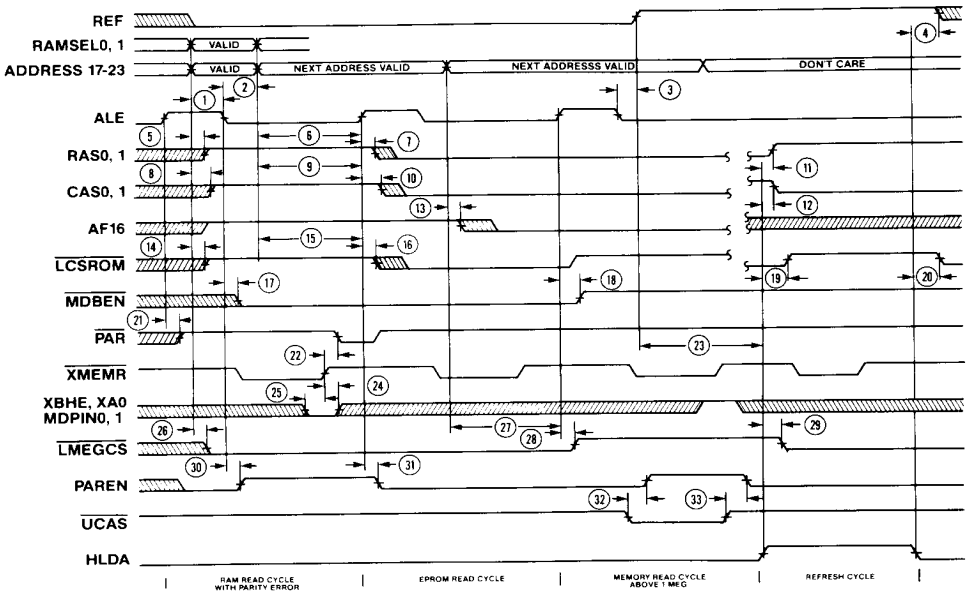
RAS0,1
$\overline{CAS0,1}$
$\overline{MDBEN}$
$\overline{AF16}$
$\overline{LCSROM}$
$\overline{LMEGCS}$

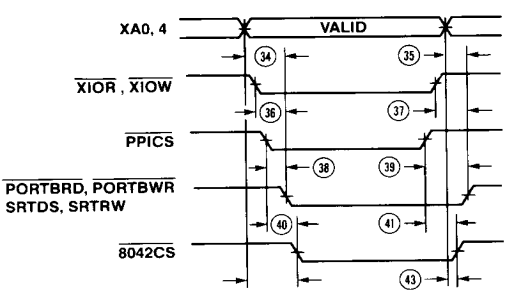
CL = 85pF
I_{ol} = 4ma
I_{oh} = 4ma

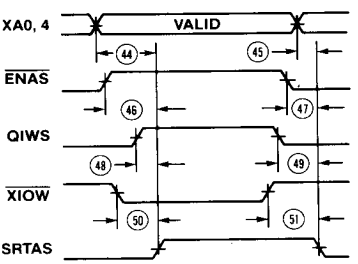
$\overline{PAR}$
$\overline{PAREN}$
$\overline{PORTBRD}$
$\overline{PORTBWR}$
SRTDS
$\overline{SRTRW}$
$\overline{8042CS}$
SRTAS

CL = 50pf
I_{ol} = 2ma
I_{oh} = 2ma

82C202 TIMING DIAGRAMS







Functional Description 82C203

Figure 7 illustrates a TTL equivalent of the logic implemented by the 82A203. As is shown in the figure, the 82A203 provides the drivers and buffers for the CPU, the System and Local I/O control buses. The memory read and write and the I/O read and write signals are bidirectional. The direction and control of the bus is determined by the DMAEN and the MASTER inputs. The chip also provides the drive and buffer capability for the high address bus signals, A17-A23. The direction and control is provided by the CPU Hold Acknowledge and ALE inputs, as shown in the figure. In addition to providing the drivers and buffers, the 82A203 also integrates the status latch (PORT B in the AT implementation). The latch can be written into and read through PORTWR and PORTRD signals.

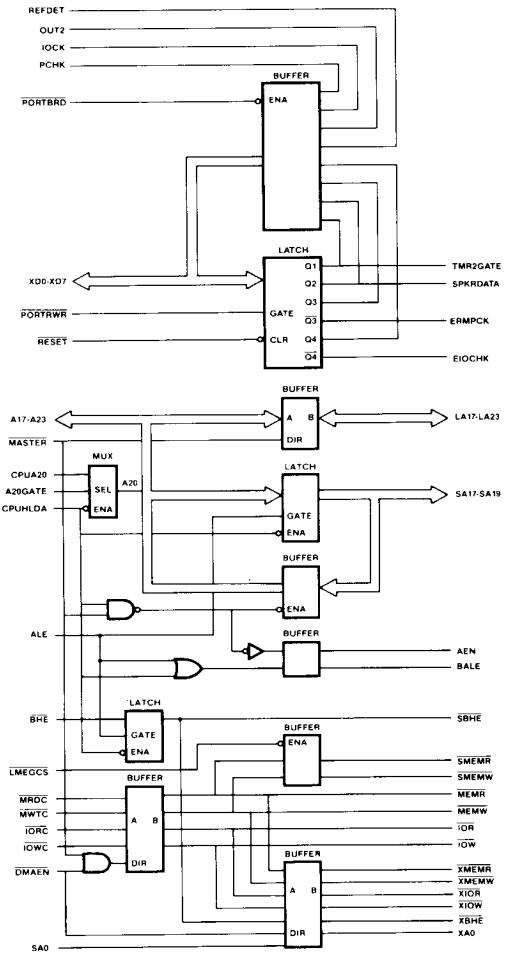


Figure 7. Functional Block Diagram

82A203 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A203 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A203 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH} = -3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All non-system and non-extended system bus outputs only.
2. All system bus and extended system bus outputs, LA17-19, SA17-19, BALE, $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$, SBHE, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, AEN AND SA0 have I_{OL} = 24mA @ V_{OL} = 0.5V.
3. All outputs and bidirectional pins.

82A203 AC Characteristics

(T_A = 0° C to 70° C, V_{CC} = 5V ± 5%)

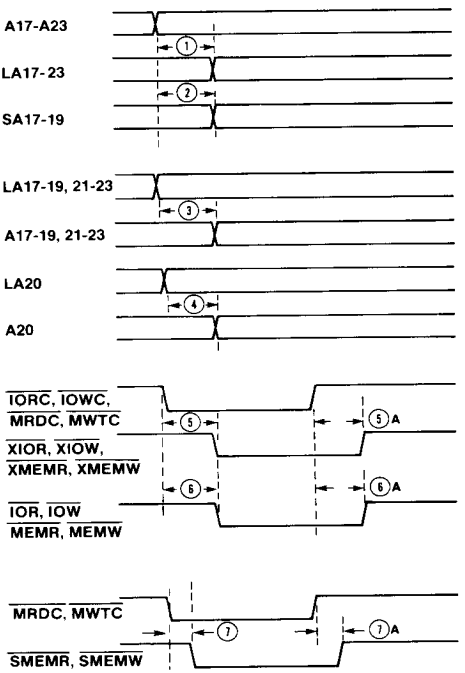
Sym	Description	Min.	Max.	Units
t1	A Bus to L Bus Address Delay	4	20	ns
t2	A Bus to S Bus Address Delay	4	20	ns
t3	L Bus to A Bus Address Delay	4	20	ns
t4	L Bus A20 to A Bus A20 Delay	4	23	ns
t5	CPU Control to Local I/O Control Delay↓	5	23	ns
t5A	CPU Control to Local I/O Control Delay↑	5	21	ns
t6	CPU Control to Extended System I/O Control Delay↓	5	25	ns
t6A	CPU Control to Extended System I/O Control Delay↑	5	21	ns
t7	CPU $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, to System $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$ Delay↓	5	23	ns
t7A	CPU $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, to System $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$ Delay↑	5	21	ns
t8	Local I/O CTRL to CPU, System I/O CTRL Delay↓	5	23	ns
t8A	Local I/O CTRL to CPU, System I/O CTRL Delay↑	5	23	ns
t9	Local I/O $\overline{\text{XMEMR}}$, $\overline{\text{XEMEW}}$, to $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$ Delay↓	5	23	ns
t9A	Local I/O $\overline{\text{XMEMR}}$, $\overline{\text{XEMEW}}$, to $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$ Delay↑	5	21	ns
t10	Expansion I/O CTRL to CPU, Local I/O CTRL Delay ↓	5	23	ns
t10A	Expansion I/O CTRL to CPU, Local I/O CTRL Delay ↑	5	21	ns
t11	Extended System $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ to $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$ Delay ↓	5	23	ns
t11A	Extended System $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ to $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$ Delay ↑	5	21	ns
t12	System SA0 to Local I/O A0 Delay ↓	3	16	ns
t12A	System SA0 to Local I/O A0 Delay ↑	4	20	ns
t13	Local I/O XA0 to System SA0 Delay ↓	3	16	ns
t13A	Local I/O XA0 to System SA0 Delay ↑	3	18	ns
t14	System SBHE to Local XBHE Delay ↓	5	22	ns
t14A	System SBHE to Local XBHE Delay ↑	5	25	ns
t15	Local I/O XBHE to System SBHE Delay ↓	5	22	ns
t15A	Local I/O XBHE to System SBHE Delay ↑	5	22	ns
t16	CPU Address A20, A20GATE to A20 Delay ↓	5	20	ns
t16A	CPU Address A20, A20GATE to A20 Delay ↑	5	20	ns
t17	ALE to System Address SA17-SA19 Valid Delay	7	30	ns
t18	CPU HLDA to AEN Delay ↑	5	22	ns
t18A	CPU HLDA to AEN Delay ↓	5	24	ns
t19	CPU HLDA to BALE Delay ↑	4	20	ns
t19A	CPU HLDA to BALE Delay ↓	4	20	ns

82A203 AC Characteristics

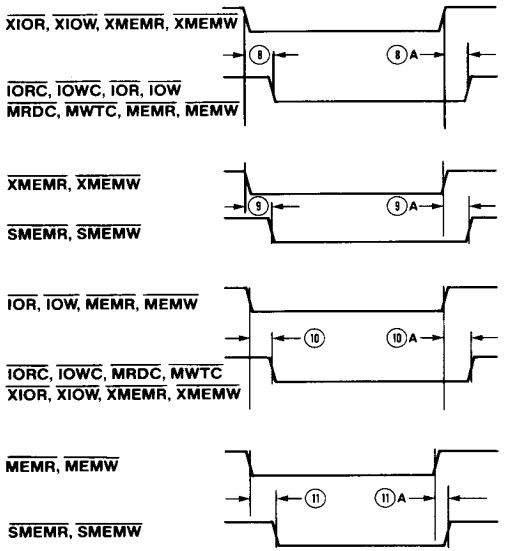
(T_A = 0° C to 70° C, V_{CC} = 5V ± 5%)
(Continued)

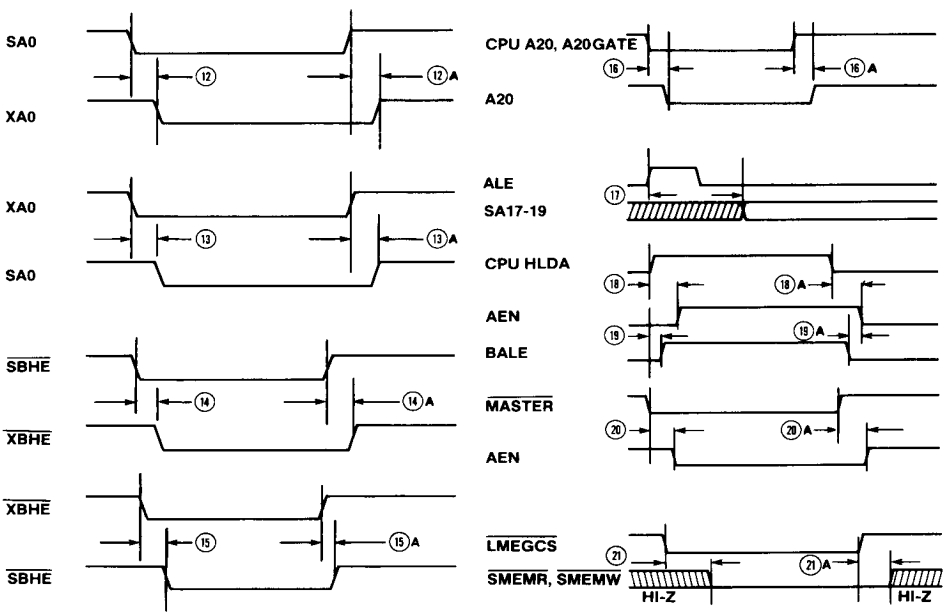
Sym	Description	Min.	Max.	Units
t20	System $\overline{\text{MASTER}}$ to AEN Delay ↓	5	24	ns
t20A	System $\overline{\text{MASTER}}$ to AEN Delay ↑	5	22	ns
t21	Low Memory $\overline{\text{LMEGCS}}$ Active to $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$ Valid	5	23	ns
t21A	Low Memory $\overline{\text{LMEGCS}}$ In-Active to $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$ HI-Z	5	20	ns

82A203 TIMING DIAGRAMS



82A203 TIMING DIAGRAMS





Functional Description 82A204

Figure 8 illustrates a TTL equivalent of the logic implemented by the 82A204. The chip provides the drive and buffering for the address signals A1-A16. Additionally, it provides the drivers for the memory address bus MA0-MA7. The direction and control for the Address buffers for A1-A16 are provided by the CPU Hold Acknowledge and $\overline{\text{DMAEN}}$ inputs, as shown in the figure. The refresh addresses are provided by a refresh counter, which is enabled by the $\overline{\text{REFEN}}$ input. The addresses for the memory are multiplexed as shown in the figure. The SA0 is an output which is active only during the refresh cycle.

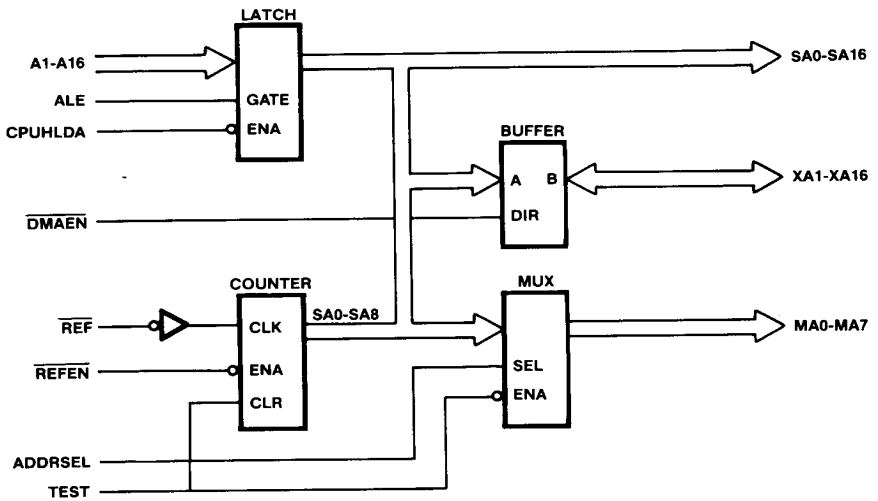


Figure 8. Functional Block Diagram

82A204 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A204 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A204 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH} = -3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	170	285	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

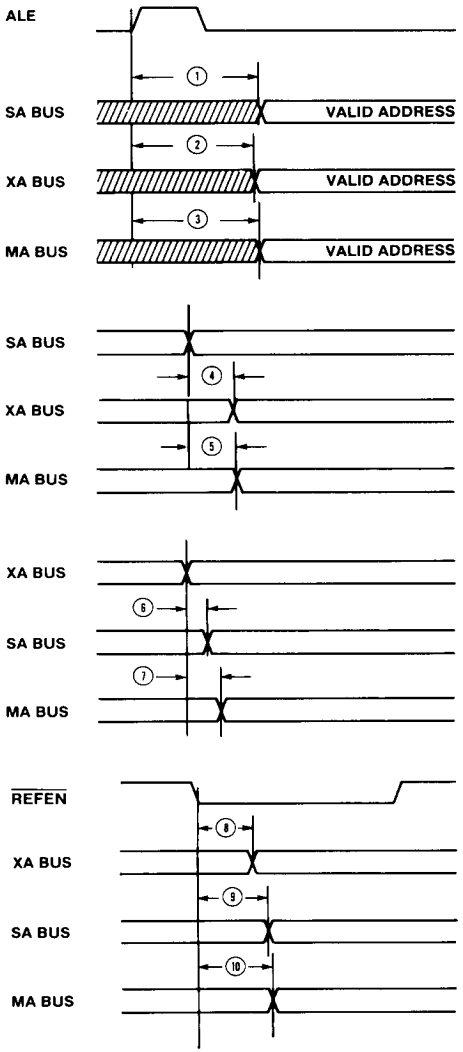
NOTES 1. All non-system and bus outputs only.
2. All system bus outputs, SA0-16, are specified at I_{OL} = 24mA @ V_{OL} = 0.5V.
3. All outputs and bidirectional pins.

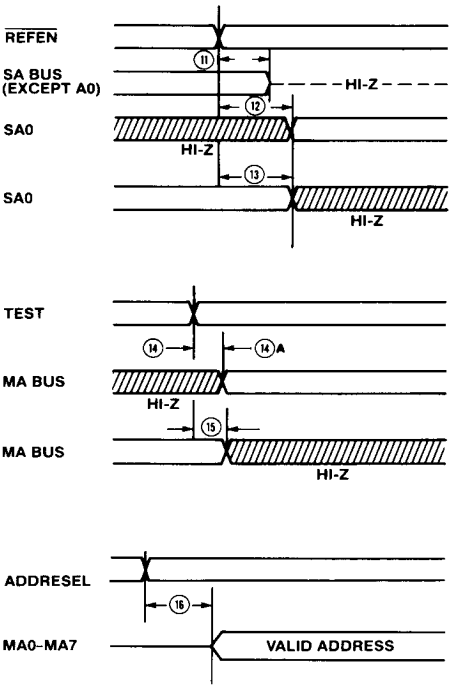
82A204 AC Characteristics

(T_A = 0° C to 70° C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Max.	Units
t1	ALE to System Address Bus Delay	8	35	ns
t2	ALE to Local I/O Address Bus Delay (XA Bus)	8	30	ns
t3	ALE to Memory Address Bus Delay	8	35	ns
t4	System Address Bus to Local I/O Address Bus Delay (XA Bus)	5	25	ns
t5	System Address Bus to Memory Address Bus Delay	5	30	ns
t6	Local /O Bus to System Address Bus Delay	6	30	ns
t7	Local I/O Bus to System Address Bus Delay	6	30	ns
t8	$\overline{\text{REFEN}}$ Active to Local I/O Address Bus Valid Delay	8	35	ns
t9	$\overline{\text{REFEN}}$ Active to System Address Bus Delay	10	40	ns
t10	$\overline{\text{REFEN}}$ Active to Memory Address Bus Delay	10	40	ns
t11	$\overline{\text{REFEN}}$ In-Active to System Address Bus HI-Z Delay	5	23	ns
t12	$\overline{\text{REFEN}}$ to SA0 Valid Delay	7	28	ns
t13	$\overline{\text{REFEN}}$ to SA0 HI-Z Delay	5	23	ns
t14	Test Enable to Memory Address Bus Valid Delay	7	29	ns
t15	Test Enable to Memory Address Bus HI-Z Delay	6	25	ns
t16	ADDRSEL to Address Valid	5	28	ns

82A204 TIMING DIAGRAMS





Functional Description 82A205

Figure 9 illustrates a TTL equivalent of logic implemented by the 82A205. The chip provides the data bus buffers and drivers for D0-D15. The three data buses controlled are the CPU bus (D0-D15), the System bus (SD0-SD15), and the Memory Data bus (MD0-MD15). The direction and control for these drivers are provided by the DT/$\overline{R}$, $\overline{DSDEN0}$, $\overline{DSDEN1}$, $\overline{XBHE}$, and XA0 inputs, as shown in the figure. The low byte to high byte conversion logic is also implemented on the chip. The conversion logic is controlled by the $\overline{ENHLB}$ and DIRHLB inputs. The chip also integrates the parity generation and check logic. The parity is computed on the memory data bus signals and output as MDPIN0 and MDPIN1. During a read cycle, the parity check is computed on the data read from the memory and the parity bits MDPOUT 0 and MDPOUT 1. On a parity error, the $\overline{PAR}$ output is activated.

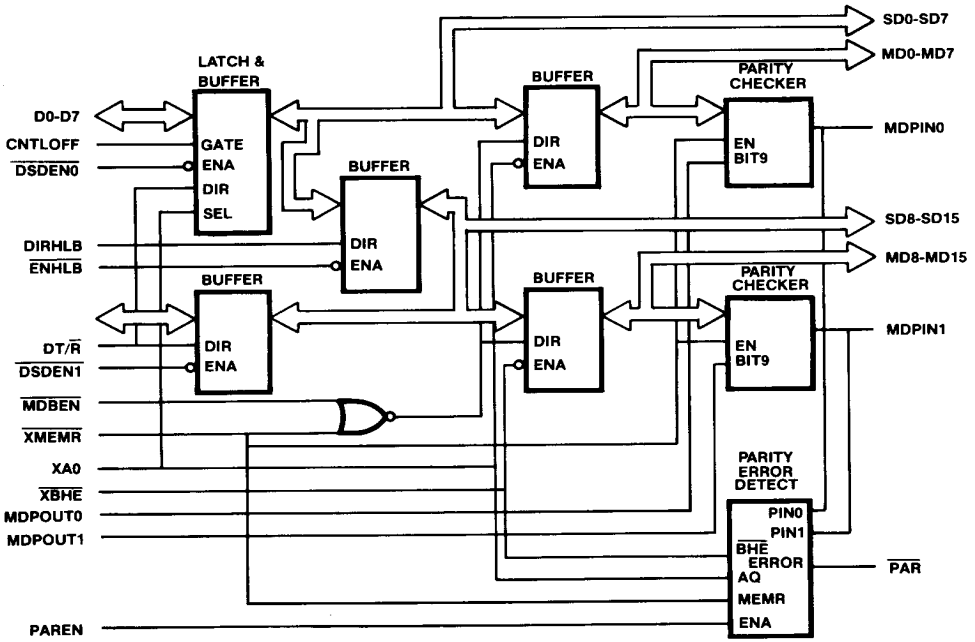


Figure 9: 82A205 Functional Block Diagram

82A205 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A205 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A205 DC Characteristics

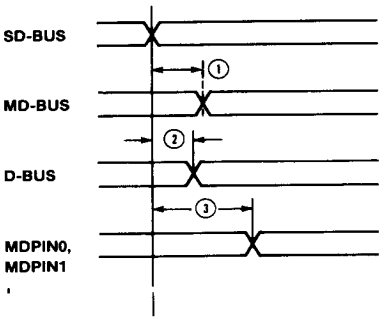
Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH} = -3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	180	300	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

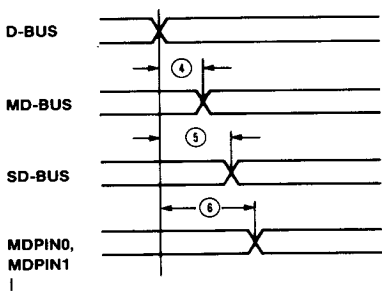
NOTES 1. All non-system and bus outputs only.
2. All system bus outputs, SD0-15, are specified at I_{OL} = 24mA @ V_{OL} = 0.5V.
3. All outputs and bidirectional pins.

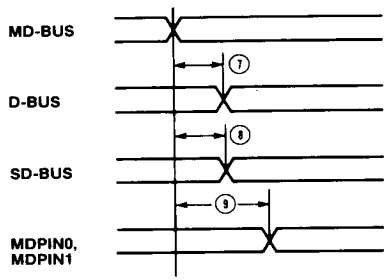
82A205 AC Characteristics

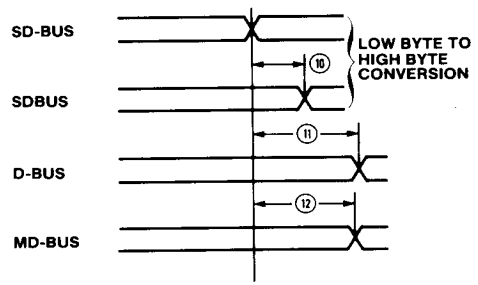
(T_A + 0° C to 70° C, V_{CC} + 5V ± 5%)

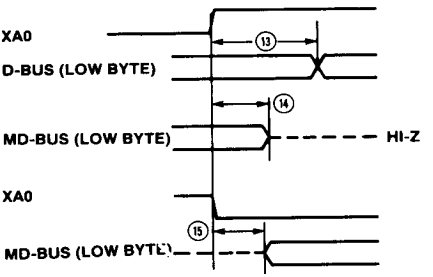
Sym	Description	Min.	Max.	Units
t1	System Data Bus to Memory Bus Delay	8	32	ns
t2	System Data Bus to CPU Data Bus Delay	8	32	ns
t3	System Data Bus to Parity Bits MDPIN0, 1 Output	12	42	ns
t4	CPU Data Bus to Memory Data Bus Delay	8	30	ns
t5	CPU Data Bus to System Data Bus Delay	5	25	ns
t6	CPU Data Bus to Parity Bits MDPIN0, MDPIN1 Output	12	42	ns
t7	Memory Data Bus to CPU Data Bus Delay	8	30	ns
t8	Memory Data Bus to System Data Bus Delay	6	27	ns
t9	Memory Data Bus to Parity Bits MDPIN0, 1 Output	10	38	ns
t10	System Data Bus Low Byte to High Byte Conversion	8	32	ns
t11	System Bus to CPU Data Bus Hi-Lo Byte Conversion	10	33	ns
t12	System Bus to Mem Data Bus Hi-Lo Byte Conversion	10	35	ns
t13	XA0 to CPU Data Bus Low Byte Delay	8	30	ns
t14	XA0 to Memory Data Bus HI-Z	6	26	ns
t15	XA0 to Memory Data Bus Address Valid	8	30	ns
t16	$\overline{\text{XMEMR}}$ Going High to Parity Delay	7	28	ns
t17	$\overline{\text{PAREN}}$ to Parity Delay	4	20	ns
t18	Parity Input Bits to Parity Output Bits Delay	12	40	ns
t19	$\overline{\text{ENHLB}}$ to SD8-SD15 delay	—	30	ns
t20	SD BUS to CNTLOFF set-up time	10		ns

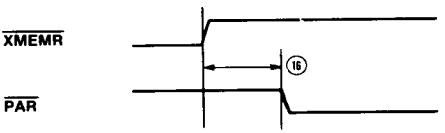


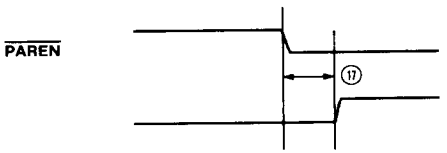


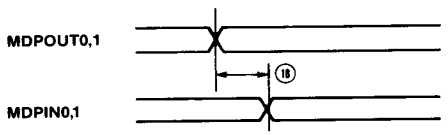


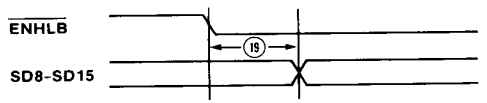


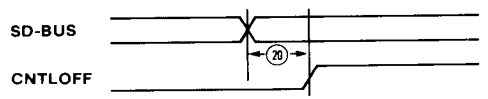






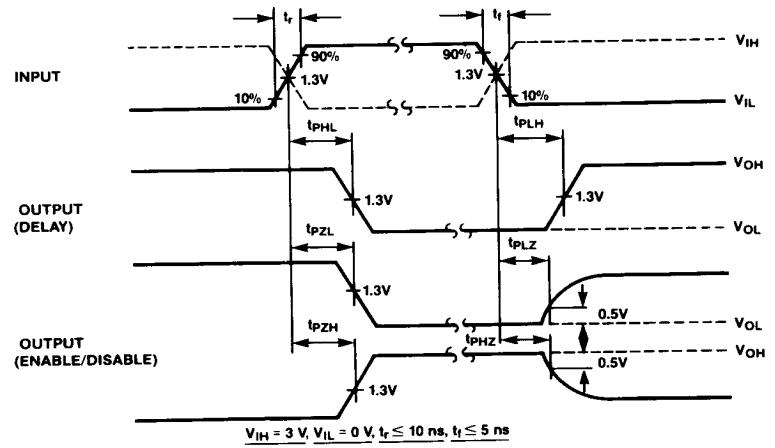


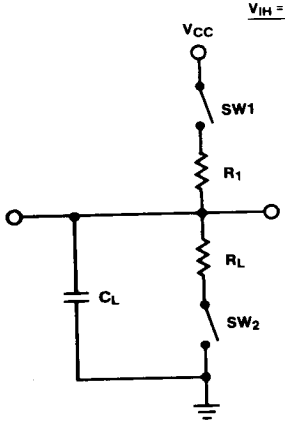




Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L(pF)	R_1 (Ω)	R_L (Ω)	SW_1	SW_2
Propagation Delay Time	Totem pole 3-state Bidirectional	t_{PLH} t_{PHL}	50	—	1.0K	OFF	ON
Propagation Delay Time	Open drain or Open Collector	t_{PLH} t_{PHL}	50	0.5K	—	ON	OFF
Disable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	5	0.5K	1.0K	ON OFF	ON
Enable Time	3-state Bidirectional	t_{PZL} t_{PZH}	50	0.5K	1.0K	ON OFF	ON ON





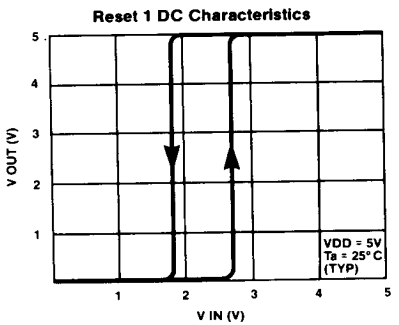
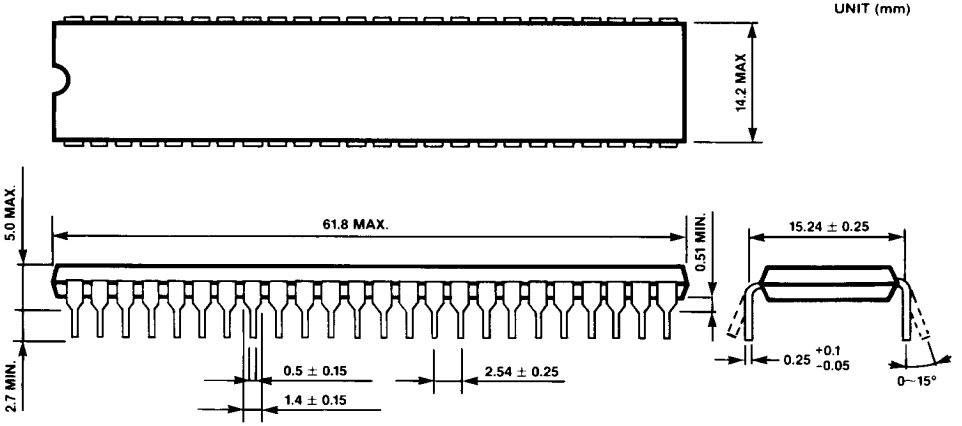


Figure 10. Load Circuit and AC Characteristics Measurement Waveform

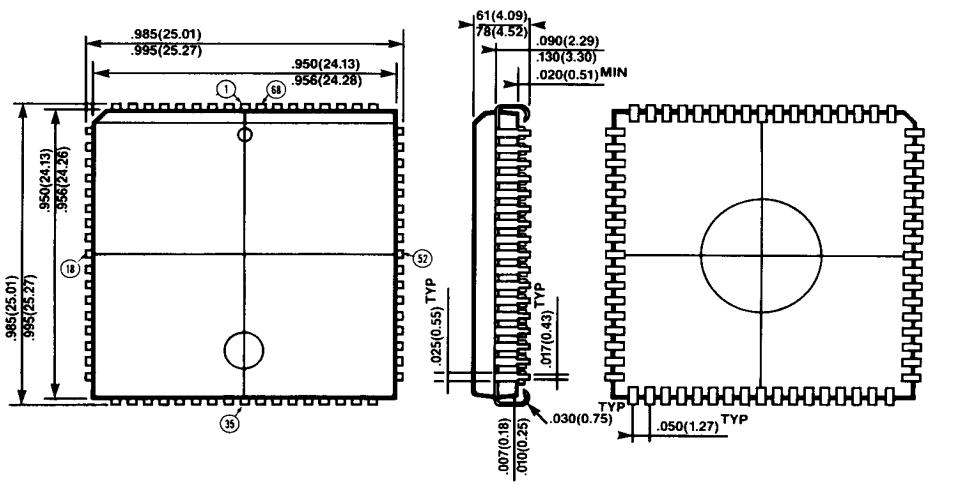
48-PIN PLASTIC DUAL-IN-LINE PACKAGE

UNIT (mm)



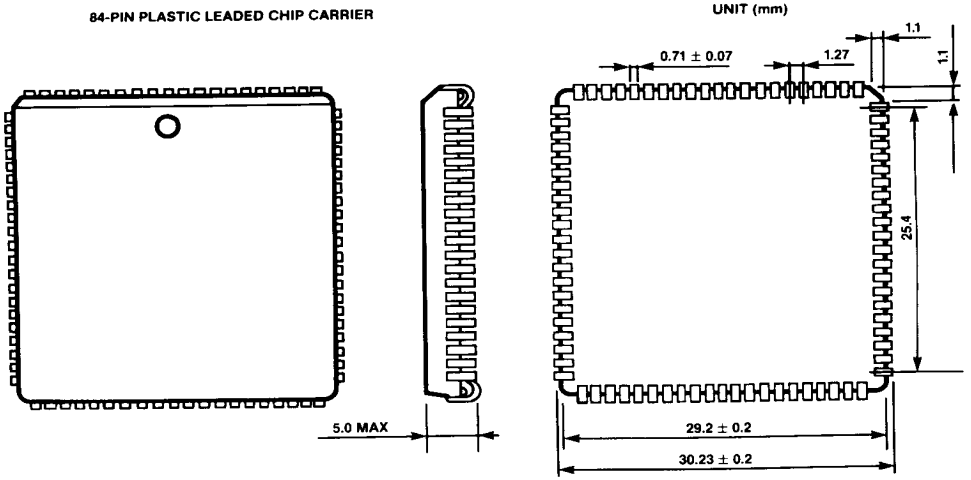
68-LEAD PLASTIC CHIP CARRIER

DIMENSIONS IN INCHES (MILLIMETERS) S = 3.6/1



84-PIN PLASTIC LEADED CHIP CARRIER

UNIT (mm)



Ordering Information

Order Number	Package Type Note 1	Remarks
P82C201, P82C201-10	PLCC-84	C (Note 2)
P82C202	PDIP-48	C
P82A203	PLCC-68	C
P82A204	PLCC-68	C
P82A205	PLCC-68	C
CS8220	—	Standard CHIPSet (Note 3)
CS8220-10	—	10MHz CHIPSet (Note 4)

NOTES
1. PLCC = Plastic Leaded Chip Carrier 84 Pins
   PDIP = Plastic Dual-In-Line Package 48 Pins
2. C = Commercial Range, 0 to 70°C, V_{DD} = 4.75 to 5.25 V
3. CS8220 consists of P82C201, P82C202, P82A203, P82A204, P82A205
4. CS8220-10 consists of P82C201-10, P82C202, P82A203, P82A204, P82A205

RECEIVED 7-13-88

PAGE REF

RESEARCHED

Chips and Technologies, Incorporated
521 Cottonwood Drive, Milpitas, CA 95035 408-434-0600 Telex 272929 CHIPS UR