P54/74PCT521, 521A, 521B
ULTRA-HIGH SPEED
CMOS 8-BIT IDENTITY COMPARATORS

FEATURES

- **Ultra-Fast Compare Time—5.5 ns**
- **Function, Pinout Compatible with the Fastest 54/74 Bipolar Logic 521**
- **CMOS for Low Power Operation**
- **Designed for Easy Expansion to Wider Word Widths**
- **Inputs and Output Interface Directly with TTL, NMOS and CMOS Devices**
- **Operational over the Full Commercial and Military Temperature Ranges**
- **Input Clamp Diode to Limit Bus Reflections**
- **Produced with PACE Technology™**
- **Standard Pinout**
  —20-Pin 300 mil DIP
  —20-Pin 350 x 350 mil LCC

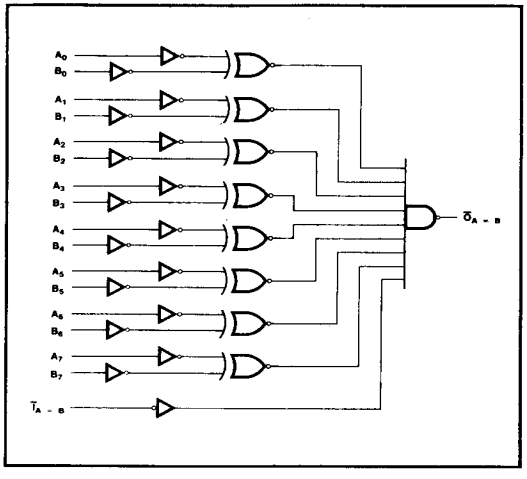
DESCRIPTION

The 'PCT521, 'PCT521A and 'PCT521B are ultra-fast expandable eight- (8-) bit comparators. Each device compares two words of up to 8 bits each. The output goes to a low level when the two words being compared match bitwise. The word width may be expanded by cascading (i.e., connecting the output of the comparator to the expansion input $\overline{I}_{A=B}$ of another 'PCT521 type device) or by logically ORing the outputs of several 'PCT521 devices. If not used for expansion, $\overline{I}_{A=B}$ must be set at CMOS low voltage. The CMOS comparator typically dissipates one-third the power of its slower bipolar equivalents. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without requiring additional components.

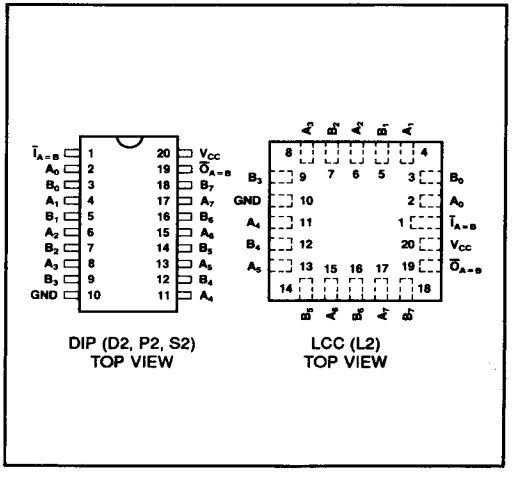
The 'PCT521s are members of the PACE LOGIC™ Family which includes byte-wide bus interface and memory related components. PACE LOGIC is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single-event-upset protection, and is supported by a Class 1 environment facility for volume production.

*For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature and 5.0V supply.

LOGIC DIAGRAM



PIN CONFIGURATIONS



DIP (D2, P2, S2)
TOP VIEW

LCC (L2)
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage				–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2			V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2			V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.7			V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V			0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)			0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)			0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)			0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF		All outputs

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CCQC}	Quiescent Power Supply Current (CMOS inputs) Com'l Mil	.003 .003	0.3 0.5	mA mA	V_{CC} = MAX, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, f = 0, Outputs Open
I_{CCQT}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, Outputs Open
I_{CC}	Total Power Supply Current[5]		4.0[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, f_1 = 10MHz, and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			4.8[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, f_1 = 10MHz, and V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQC} + I_{CCQT}D_HN_T + I_{CCD}(f_0/2 + f_1N_1)$
   I_{CCQC} = Quiescent Current with CMOS input levels
   I_{CCQ} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

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AC CHARACTERISTICS

Sym.	Parameter	54PCT521		74PCT521		54PCT521A		74PCT521A		54PCT521B		74PCT521B		Unit	Fig. No.
		T_A, V_{cc} = Comm. C_L = 50 pF		T_A, V_{cc} = Comm. C_L = 50 pF		T_A, V_{cc} = Comm. C_L = 50 pF		T_A, V_{cc} = Comm. C_L = 50 pF		T_A, V_{cc} = Comm. C_L = 50 pF		T_A, V_{cc} = Comm. C_L = 50 pF			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH}	Propagation Delay	1.5	15.0	1.5	11	1.5	9.5	1.5	7.2	1.5	7.3	1.5	5.5	ns	1,
t_{PHL}	A_N or B_N to $\overline{O}_{A=B}$	1.5	12.0	1.5	10.5	1.5	9.5	1.5	7.2	1.5	7.3	1.5	5.5		2, 3
t_{PLH}	Propagation Delay	1.5	8.5	1.5	7.5	1.5	7.8	1.5	6.0	1.5	6.0	1.5	4.6	ns	1, 3
t_{PHL}	$\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	1.5	9.0	1.5	8.0	1.5	7.8	1.5	6.0	1.5	6.0	1.5	4.6		

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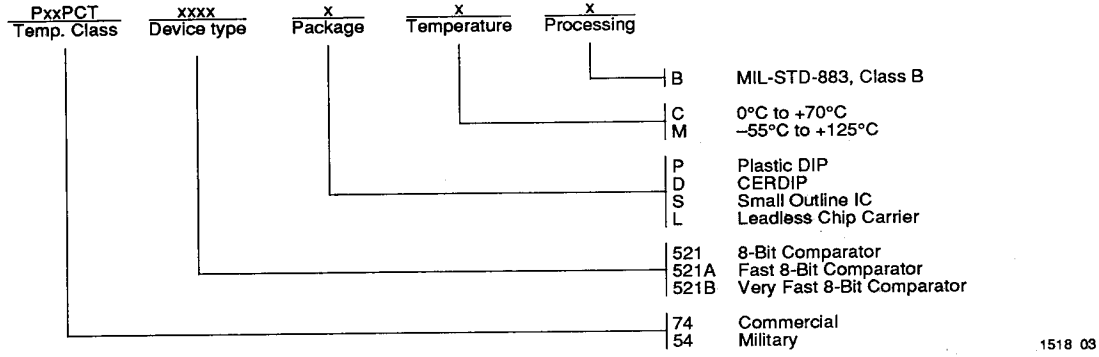
Note:
1. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION



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